

74LVC1GU04

Inverter

Rev. 08 — 12 June 2007

Product data sheet

1. General description

The 74LVC1GU04 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The input can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

The 74LVC1GU04 provides the inverting single state unbuffered function.

2. Features

- Wide supply voltage range from 1.65 V to 5.5 V
- High noise immunity
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Input accepts voltages up to 5 V
- Multiple package options
- ESD protection:
 - ◆ HBM JESD22-A114-D exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

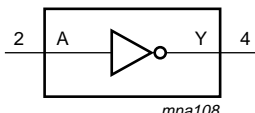
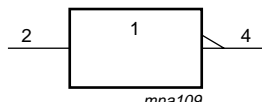
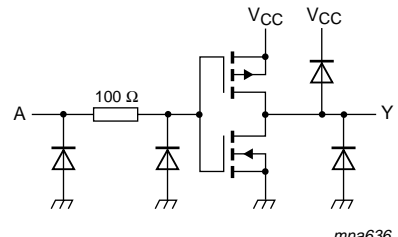
Type number	Package			
	Temperature range	Name	Description	Version
74LVC1GU04GW	-40 °C to $+125$ °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74LVC1GU04GV	-40 °C to $+125$ °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74LVC1GU04GM	-40 °C to $+125$ °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body $1 \times 1.45 \times 0.5$ mm	SOT886
74LVC1GU04GF	-40 °C to $+125$ °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body $1 \times 1 \times 0.5$ mm	SOT891

4. Marking

Table 2. Marking codes

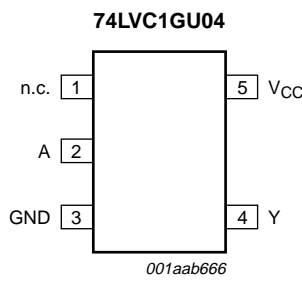
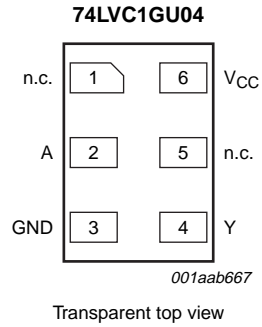
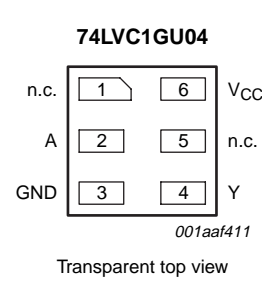
Type number	Marking
74LVC1GU04GW	VD
74LVC1GU04GV	VU4
74LVC1GU04GM	VD
74LVC1GU04GF	VD

5. Functional diagram

 <p>Fig 1. Logic symbol</p>	 <p>Fig 2. IEC logic symbol</p>	 <p>Fig 3. Logic diagram</p>
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6. Pinning information

6.1 Pinning

 <p>Fig 4. Pin configuration SOT353-1 and SOT753</p>	 <p>Fig 5. Pin configuration SOT886</p>	 <p>Fig 6. Pin configuration SOT891</p>
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6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT353-1/SOT753	SOT886/SOT891	
n.c.	1	1	not connected
A	2	2	data input A
GND	3	3	ground (0 V)
Y	4	4	data output Y
n.c.	-	5	not connected
V _{CC}	5	6	supply voltage

7. Functional description

Table 4. Function table^[1]

Input (A)	Output (Y)
L	H
H	L

- [1] H = HIGH voltage level;
L = LOW voltage level.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-	-50	mA
V _I	input voltage		^[1] -0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
V _O	output voltage	Active mode	^{[1][2]} -0.5	V _{CC} + 0.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	+100	mA
I _{GND}	ground current		-	-100	mA
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	^[3] -	250	mW
T _{stg}	storage temperature		-65	+150	°C

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 [2] When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.
 [3] For TSSOP5 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.
 For XSON6 packages: above 45 °C the value of P_{tot} derates linearly with 2.4 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$	0	-	20	ns/V
		$V_{CC} = 2.7\text{ V to }5.5\text{ V}$	0	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$T_{amb} = -40\text{ °C to }+85\text{ °C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65\text{ V to }5.5\text{ V}$	$0.75 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65\text{ V to }5.5\text{ V}$	-	-	$0.25 \times V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100\ \mu\text{A};$ $V_{CC} = 1.65\text{ V to }5.5\text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -4\text{ mA}; V_{CC} = 1.65\text{ V}$	1.2	-	-	V
		$I_O = -8\text{ mA}; V_{CC} = 2.3\text{ V}$	1.9	-	-	V
		$I_O = -12\text{ mA}; V_{CC} = 2.7\text{ V}$	2.2	-	-	V
		$I_O = -24\text{ mA}; V_{CC} = 3.0\text{ V}$	2.3	-	-	V
		$I_O = -32\text{ mA}; V_{CC} = 4.5\text{ V}$	3.8	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100\ \mu\text{A};$ $V_{CC} = 1.65\text{ V to }5.5\text{ V}$	-	-	0.1	V
		$I_O = 4\text{ mA}; V_{CC} = 1.65\text{ V}$	-	-	0.45	V
		$I_O = 8\text{ mA}; V_{CC} = 2.3\text{ V}$	-	-	0.3	V
		$I_O = 12\text{ mA}; V_{CC} = 2.7\text{ V}$	-	-	0.4	V
		$I_O = 24\text{ mA}; V_{CC} = 3.0\text{ V}$	-	-	0.55	V
		$I_O = 32\text{ mA}; V_{CC} = 4.5\text{ V}$	-	-	0.55	V
I_I	input leakage current	$V_I = 5.5\text{ V or GND}; V_{CC} = 0\text{ V to }5.5\text{ V}$	-	± 0.1	± 5	μA
I_{CC}	supply current	$V_I = 5.5\text{ V or GND}; I_O = 0\text{ A};$ $V_{CC} = 1.65\text{ V to }5.5\text{ V}$	-	0.1	10	μA
C_I	input capacitance	$V_{CC} = 3.3\text{ V}; V_I = \text{GND to }V_{CC}$	-	6	-	pF

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 5.5 V	0.8 × V _{CC}	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 5.5 V	-	-	0.2 × V _{CC}	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -100 μA; V _{CC} = 1.65 V to 5.5 V	V _{CC} - 0.1	-	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	0.95	-	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.7	-	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	1.9	-	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.0	-	-	V
		I _O = -32 mA; V _{CC} = 4.5 V	3.4	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 μA; V _{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.7	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.80	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	-	0.80	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	±0.1	±5	μA
I _{CC}	supply current	V _I = 5.5 V or GND; I _O = 0 A; V _{CC} = 1.65 V to 5.5 V	-	-	200	μA

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	A to Y; see Figure 7 ^[2]						
		V _{CC} = 1.65 V to 1.95 V	0.3	1.7	5.0	0.3	6.5	ns
		V _{CC} = 2.3 V to 2.7 V	0.3	1.3	4.0	0.3	5.5	ns
		V _{CC} = 2.7 V	0.5	1.7	5.0	0.5	6.5	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	1.6	3.7	0.5	5.0	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	1.3	3.0	0.5	4.0	ns

Table 8. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} ; V _{CC} = 3.3 V	-	14.9	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

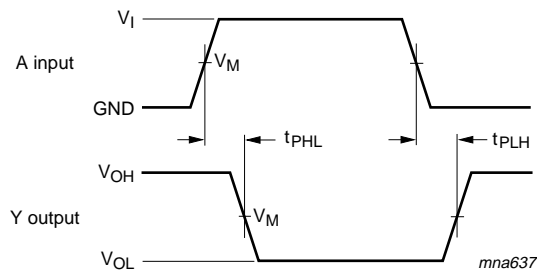
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

∑(C_L × V_{CC}² × f_o) = sum of outputs.

12. Waveforms



Measurement points are given in [Table 9](#).

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 7. The input A to output Y propagation delay times

Table 9. Measurement points

Supply voltage	Input	Output
V _{CC}	V _M	V _M
1.65 V to 1.95 V	0.5 × V _{CC}	0.5 × V _{CC}
2.3 V to 2.7 V	0.5 × V _{CC}	0.5 × V _{CC}
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	0.5 × V _{CC}	0.5 × V _{CC}

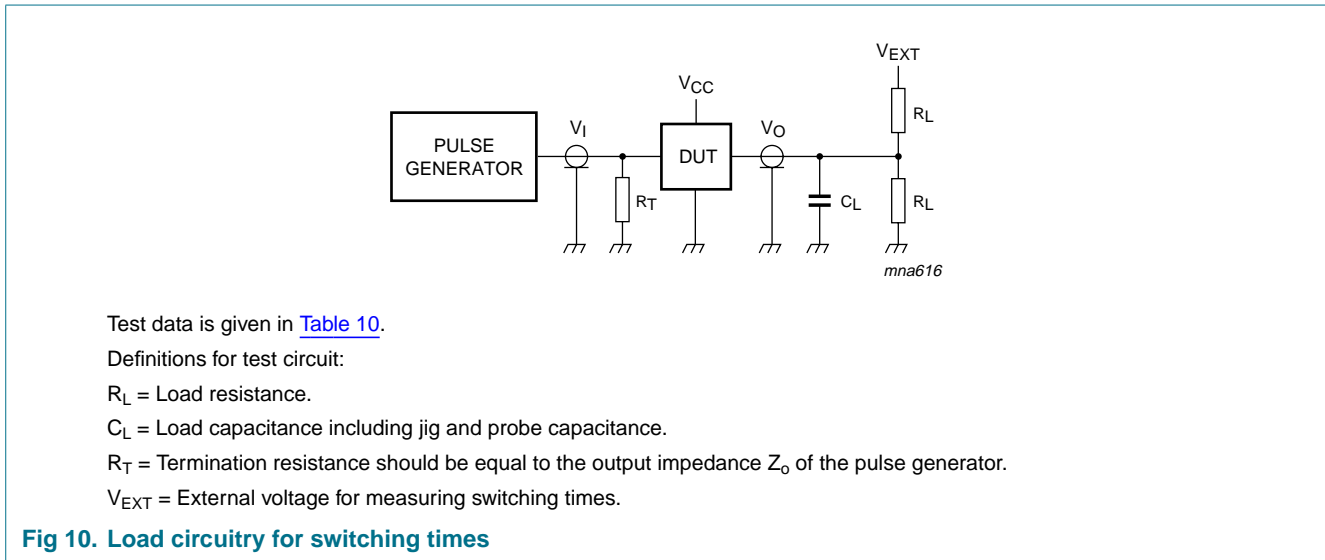
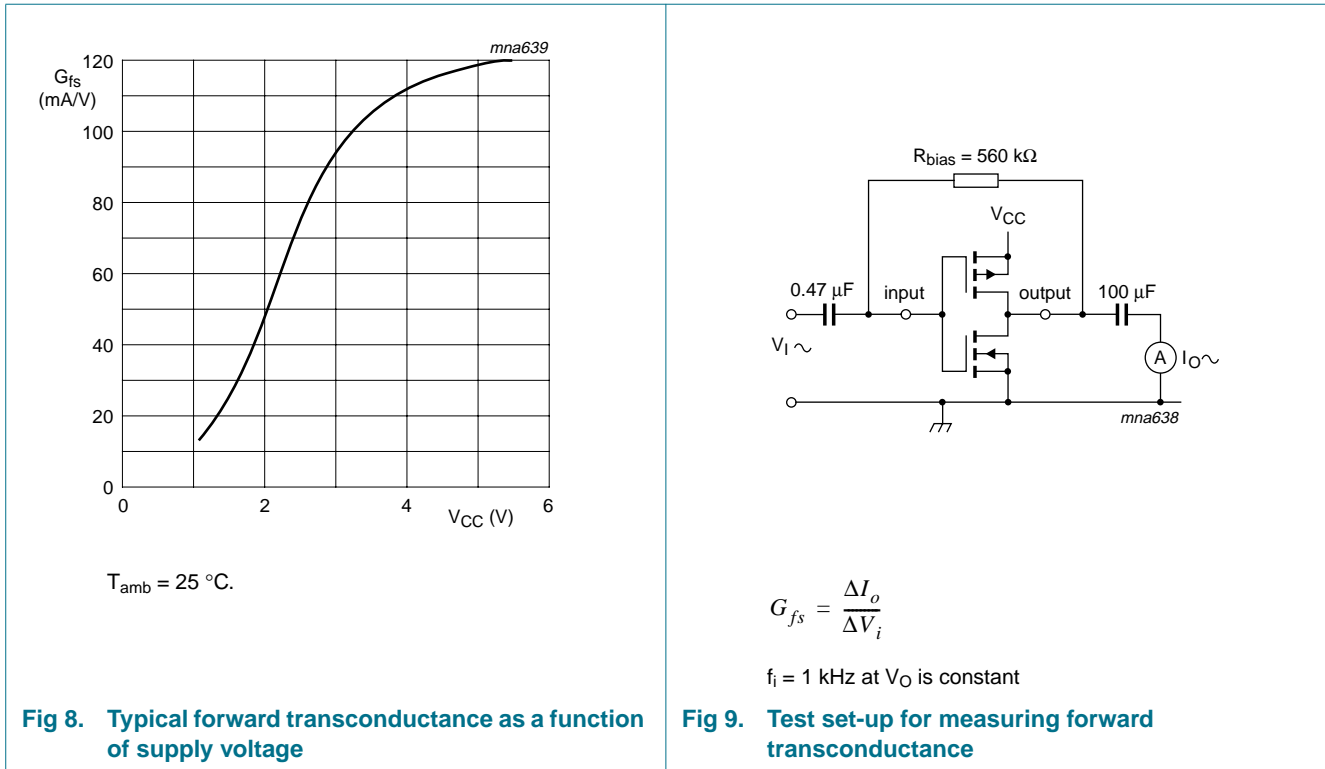


Table 10. Test data

Supply voltage	Input	Load	V_{EXT}
V_{CC}	V_I	C_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	$t_r = t_f$ 30 pF	1 kΩ open
2.3 V to 2.7 V	V_{CC}	$t_r = t_f$ 30 pF	500 Ω open

Table 10. Test data ...continued

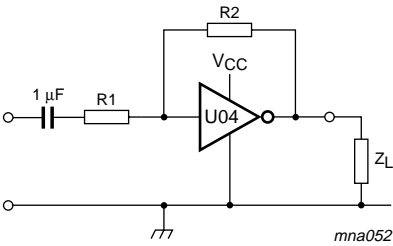
Supply voltage	Input		Load		V _{EXT}
V _{CC}	V _I	t _r = t _f	C _L	R _L	t _{PLH} , t _{PHL}
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V _{CC}	≤ 2.5 ns	50 pF	500 Ω	open

13. Application information

Some applications are:

- Linear amplifier (see [Figure 11](#))
- In crystal oscillator design (see [Figure 12](#))

Remark: All values given are typical unless otherwise specified.

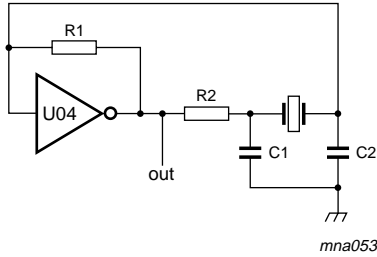


$V_{o(p-p)} = V_{CC} - 1.5 \text{ V}$ centered at $0.5V_{CC}$.

$$A_u = -\frac{A_{OL}}{1 + \frac{R1}{R2}(1 + A_{OL})}$$

A_{OL} = open loop amplification.
 A_u = voltage amplification.
 R1 ≥ 3 kΩ, R2 ≤ 1 MΩ
 Z_L > 10 kΩ; A_{OL} = 20 (typ.)
 Typical unity gain bandwidth product is 5 MHz.

Fig 11. Used as a linear amplifier



C1 = 47 pF (typ.)
 C2 = 22 pF (typ.)
 R1 = 1 MΩ to 10 MΩ (typ.)
 R2 optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} (I_{CC} is typically 2 mA at V_{CC} = 3.3 V and f = 10 MHz).

Fig 12. Crystal oscillator configuration

14. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1

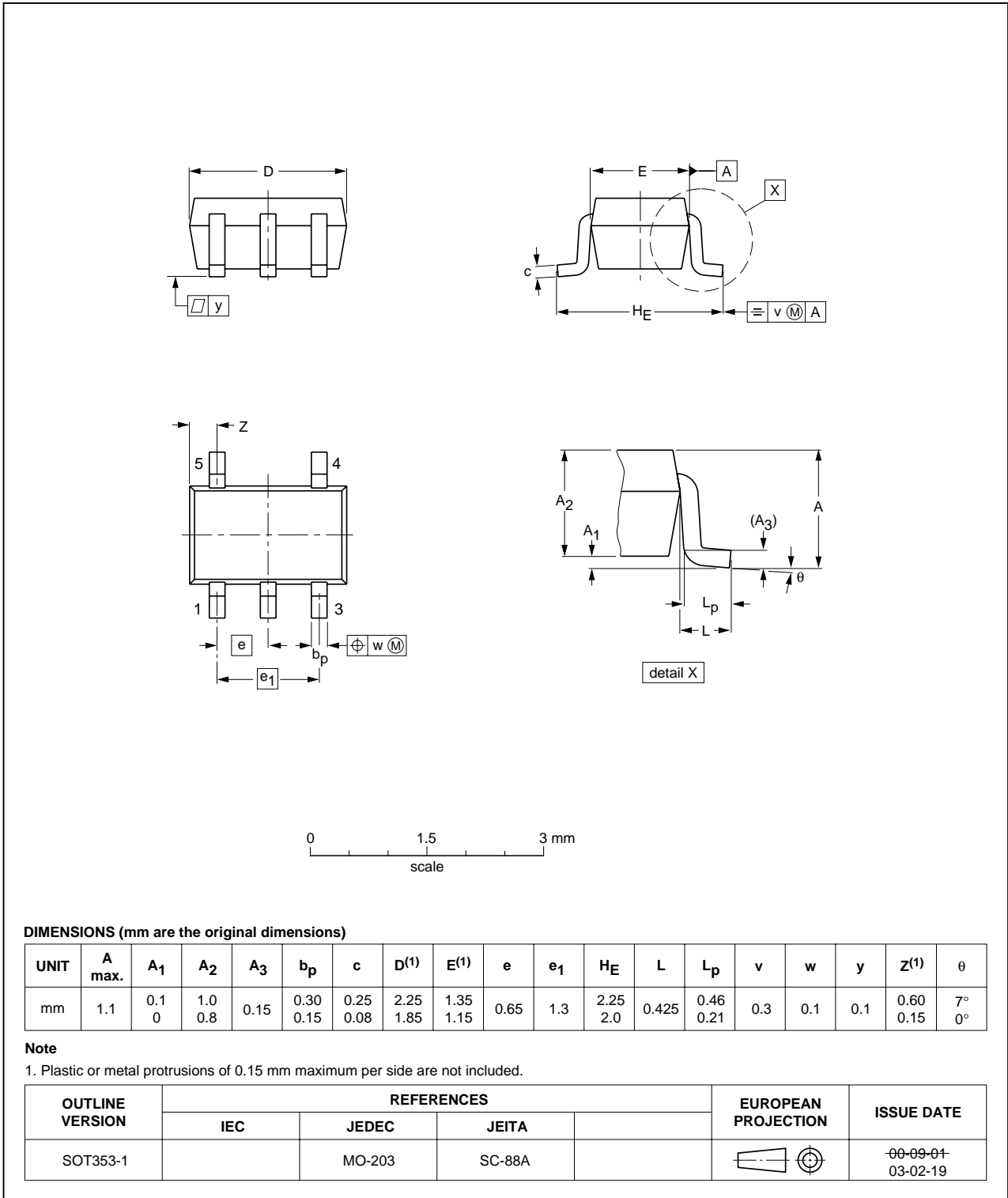


Fig 13. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

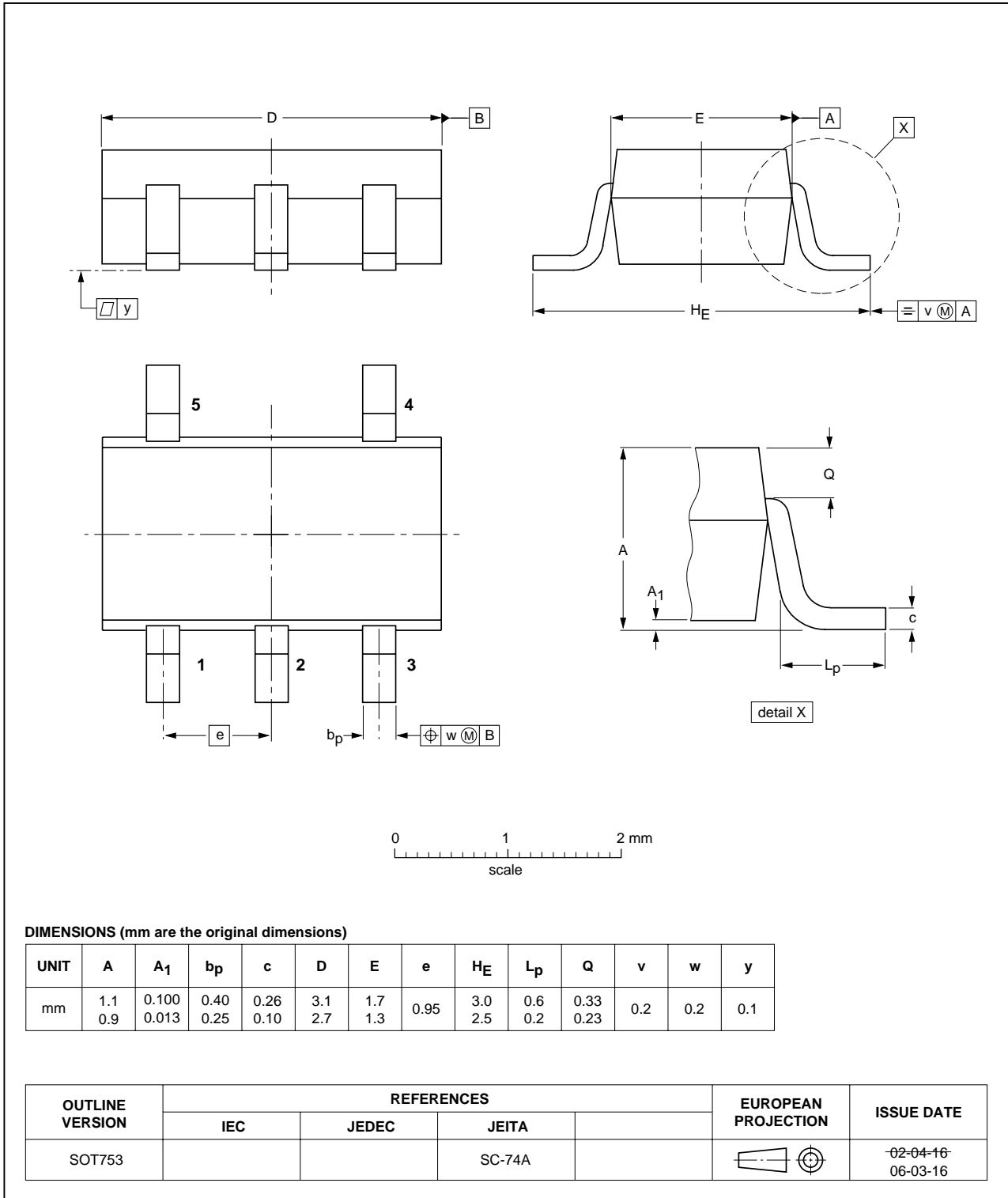


Fig 14. Package outline SOT753 (SC-74A)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886

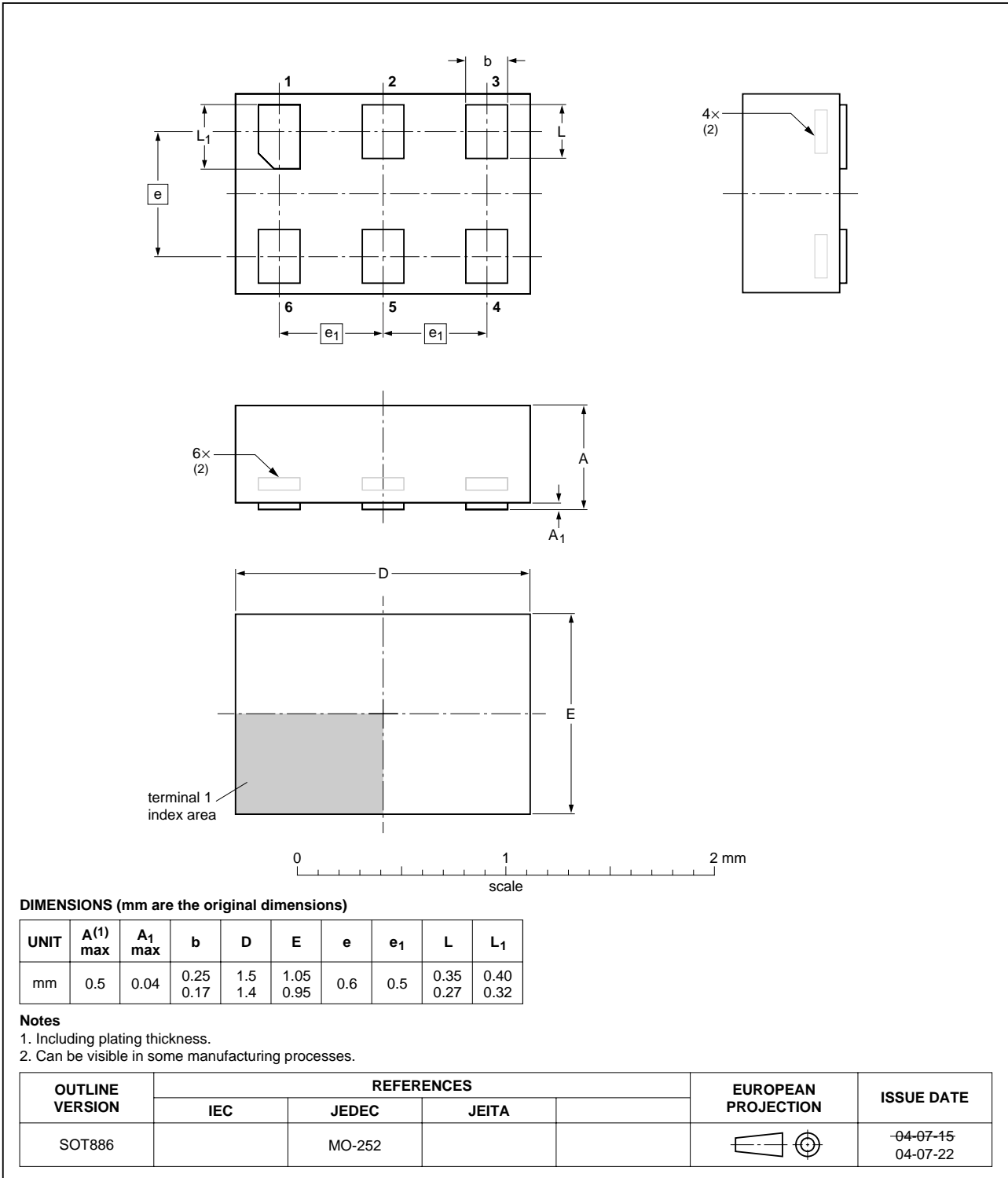


Fig 15. Package outline SOT886 (XSON6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm

SOT891

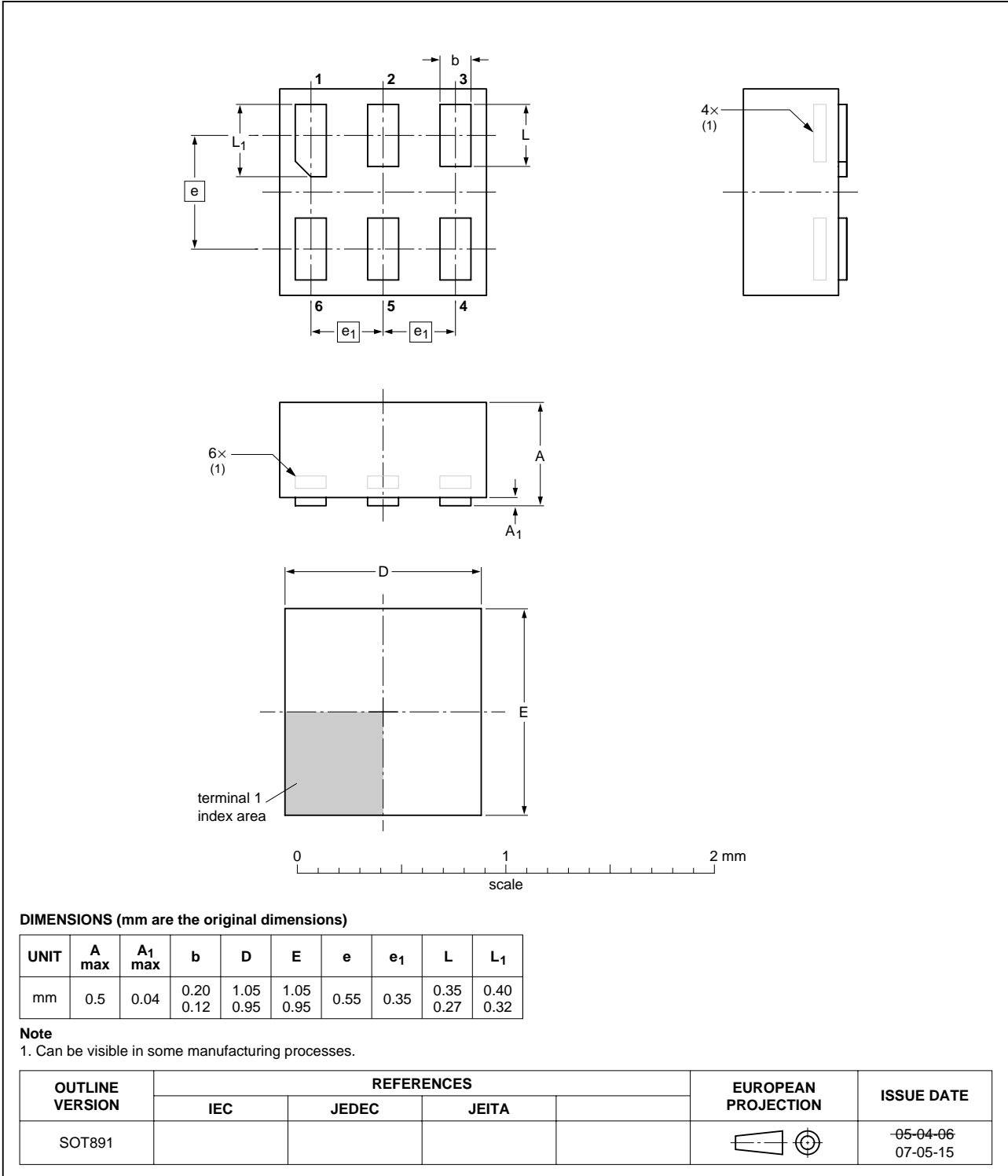


Fig 16. Package outline SOT891 (XSON6)

15. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

16. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1GU04_8	20070612	Product data sheet	-	74LVC1GU04_7
Modifications:	<ul style="list-style-type: none"> The general description has been changed. 			
74LVC1GU04_7	20061006	Product data sheet	-	74LVC1GU04_6
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Added type number 74LVC1GU04GF (XSON6/SOT891 package). 			
74LVC1GU04_6	20040921	Product specification	-	74LVC1GU04_5
74LVC1GU04_5	20040628	Product specification	-	74LVC1GU04_4
74LVC1GU04_4	20030630	Product specification	-	74LVC1GU04_3
74LVC1GU04_3	20030212	Product specification	-	74LVC1GU04_2
74LVC1GU04_2	20010406	Product specification	-	74LVC1GU04_1
74LVC1GU04_1	20001212	Product specification	-	-

17. Legal information

17.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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