Document Number: MC33800
Rev. 5.0, 10/2007

RoHS

Engine Control Integrated Circuit

33800

ENGINE CONTROL

EK SUFFIX (Pb-FREE)
98ASA99334D
54-PIN SOICW-EP

The 33800 is a combination output switch and driver Integrated Circuit (IC) which can be used in numerous powertrain applications. The IC contains two programmable constant current drivers (CCD), an octal, low side, serial switch (OSS), and six, external MOSFET gate pre-drivers (GD). The IC has over-voltage, under-voltage, and thermal protection. All drivers and switches, including the external MOSFETs, have over-current protection, off-state open load detection, on-state shorted load detection, and fault annunciation via the serial peripheral interface (SPI).

Additional features include: Low power Sleep Mode, Heated Exhaust Gas Oxygen (HEGO) sensor diagnostics, output control via serial and/or parallel inputs, PWM capability, and programmable current output with dithering. These features, along with cost effective packaging, make the 33800 ideal for Powertrain Engine Control applications.

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MCZ33800EK/R2	-40°C to 125°C	54 SOICW EP

Features

- Wide operating voltage range, 5 < VPWR < 36V
- Interfaces to 3.3V and 5V microprocessors via SPI protocol
- Low, Sleep Mode, standby current, typically 10uA.
- Internal or external voltage reference
- Internal oscillator with calibrate capability
- Measures resistance to monitor HEGO sensors
- CCDs have programmable current, dither frequency and amplitude
- OSSs can be paralleled to increase current capability
- GDs have programmable frequency and duty cycle PWM
- All outputs controllable via serial and/or parallel inputs
- Pb-free packaging designated by suffix code EK

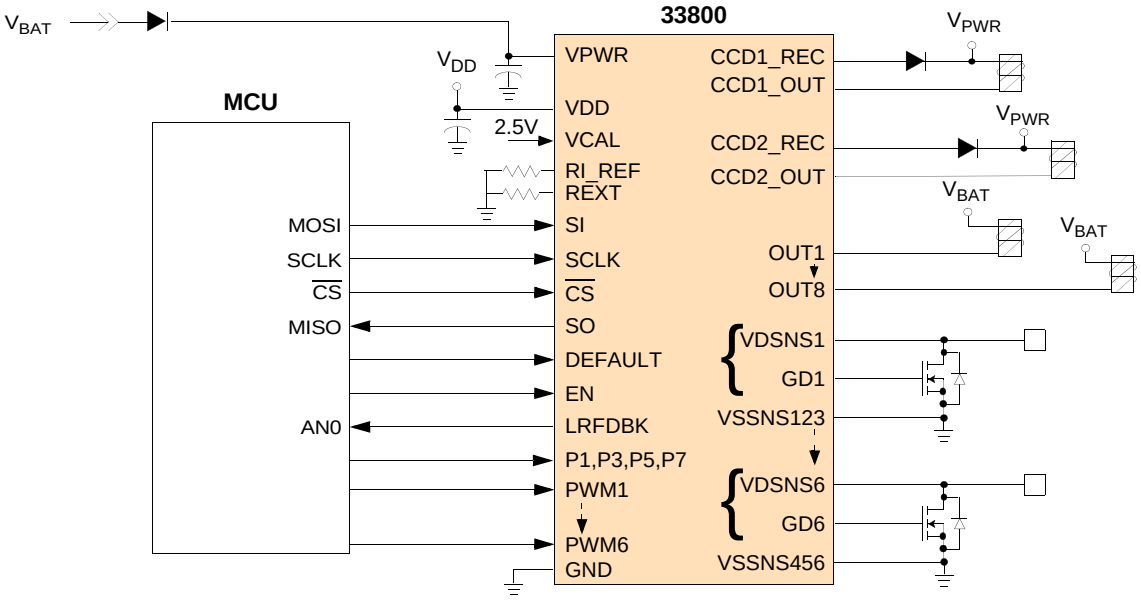

Figure 1. MC33800 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

freescale semiconductor

INTERNAL BLOCK DIAGRAM

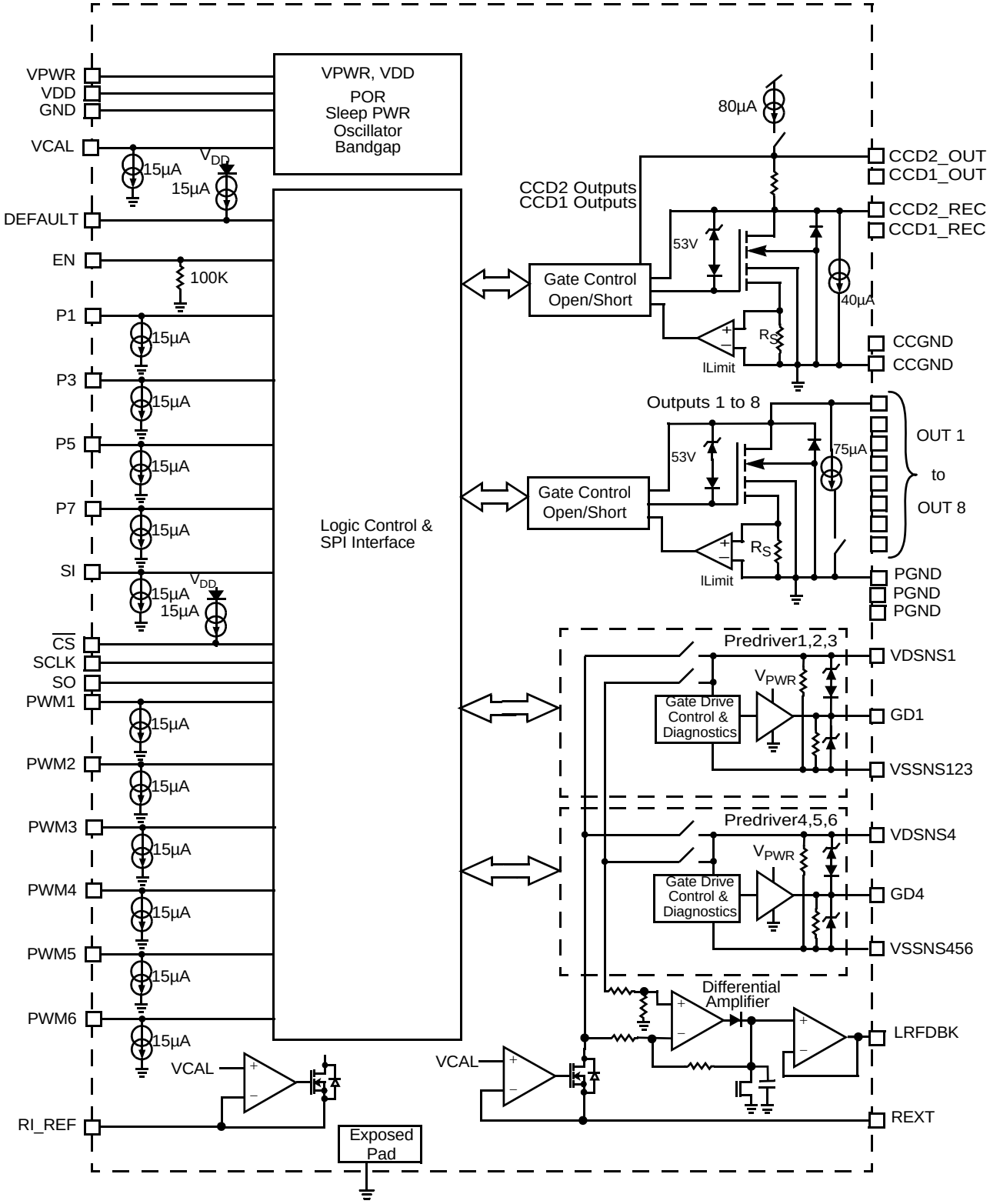

Figure 2. 33800 Simplified Internal Block Diagram

PIN CONNECTIONS

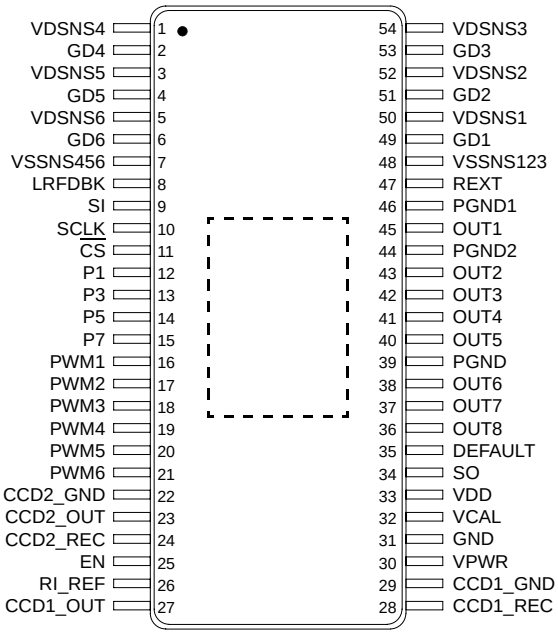

Figure 3. 33800 Pin Connections

Table 1. 33800 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 16.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1, 3, 5, 50, 52, 54	VDSNS1-VDSNS6	Input	Drain Voltage Sense	The VDSNS pin is used to monitor the drain voltage of the external MOSFET.
2, 4, 6, 49, 51, 53	GD1-GD6	Output	Gate Driver Output	The GD pin provides gate drive for an external MOSFET
7 48	VSSNS456 VSSNS123	Input	Source Voltage Sense	The VSSNS pins are used to monitor the source voltage of the external MOSFETS.
8	LRFDBK	Output	Load Resistance Feedback	The LRFDBK pin is an operational amplifier output.
9	SI	Input	Serial Input Data	The SI input pin is used to receive serial data from the MCU. The serial input data is latched on the rising edge of SCLK, and the input data transitions on the falling edge of SCLK.
10	SCLK	Input	Serial Clock Input	The SCLK input pin is used to clock in and out the serial data on the SI and SO Pins while being addressed by the $\overline{CS}$.
11	$\overline{CS}$	Input	Chip Select	The Chip Select input pin is an active low signal sent by the MCU to indicate that the device is being addressed. This input requires CMOS logic levels and has an internal active pull up current source.
12	P1	Input	Input One	Input control of OSS output 1. When configured via the SPI, P1 input may be used to control OSS output 1 and output 2 in parallel.
13	P3	Input	Input Three	Input control of OSS output 3. When configured via the SPI, P3 input may be used to control OSS output 3 and output 4 in parallel.
14	P5	Input	Input Five	Input control of OSS output 5. When configured via the SPI, P5 input may be used to control OSS output 5 and output 6 in parallel.

Table 1. 33800 Pin Definitions(continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 16.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
15	P7	Input	Input Seven	Input control of OSS output 7. When configured via the SPI, P7 input may be used to control OSS output 7 and output 8 in parallel.
16,17, 18, 19, 20, 21	PWMX	Input	Pulse Width Modulated Input	The PWMX input pin is used for direct parallel control of the GDX (Gate Drive Output X) predriver or as on/off control of the internal PWM controller. Control strategy is programmed via the SPI.
22	CCD2_GND	Ground	CCD2 Ground	The CCD2_GND pin provides a dedicated ground for the CCD2 constant current controller
23	CCD2_OUT	Output	Current Controlled Driver 2 Output	The CCD2_OUT pin is connected to a series internal sense resistor and power MOSFET driver. The CCD2_OUT has a pull up and pull down current source and is used for fault threshold monitoring.
24	CCD2_REC	Input	Current Controlled Driver 2 Recirculation Input	The CCD2_REC pin provides a recirculation path for the load current. The CCD2_REC pin is connected to the node between the internal sense resistor and power MOSFET driver. The device uses the differential voltage between CCD2_REC and CCD2_OUT to determine the load solenoid current.
25	EN	Input	ENABLE	The EN pin is an active high input.
26	RI_REF	Output	Resistor for Current Reference	The RI_REF pin is used to generate a reference current. The reference is used in the regulation of the constant current controller. The constant current controller regulation current is inversely proportional to the reference current through the external resistor. A 39.2kΩ 1% resistor to ground will set the 1FF programmed current value of the CCD1 to 1075mA and the CCD2 to be 232mA.
27	CCD1_OUT	Output	Current Controlled Driver 1 Output	The CCD1_OUT pin is connected to a series internal sense resistor and power MOSFET driver. The CCD1_OUT has a pull up and pull down current source and is used for fault threshold monitoring.
28	CCD1_REC	Input	Current Controlled Driver 1 Recirculation Input	The CCD1_REC pin provides a recirculation path for the load current. The CCD1_REC pin is connected to the node between the internal sense resistor and power MOSFET driver. The device uses the differential voltage between CCD1_REC and CCD1_OUT to determine the load solenoid current.
29	CCD1_GND	Ground	CCD1 Ground	The CCD1_GND pin provides a dedicated ground for the CCD1 constant current controller
30	VPWR	Power Input	Analog Voltage Supply	The VPWR pin provides power to all pre-driver, driver and output circuits and other internal functions such as the oscillator and SPI circuits.
31	GND	Ground	Ground	Analog ground for the internal control circuits of the IC. This ground should be used for decoupling of VDD and VPWR supply.
32	VCAL	Input	Voltage Calibrated Input	VCAL input is a precision (2.5V, +8.0mV, -20mV over temperature) reference input, used in several internal circuits. A 1.0nF to 10nF decoupling capacitor is required on the VCAL input pin to ground.
33	VDD	Power Input	Digital Voltage Supply	The VDD pin supplies power to the Serial Output (SO) buffer along with the pull up current sources for the chip select ($\overline{CS}$) and DEFAULT inputs.
34	SO	Output	Serial Output Data	The SO output pin is used to transmit serial data from the device to the MCU. The SO pin remains tri-stated until selected by the active low $\overline{CS}$. The serial output data is available to be latched by the MCU on the rising edge of SCLK. The SO data transitions on falling edge of the SCLK.
35	DEFAULT	Input	Default Mode Enable	The DEFAULT pin is an active high input.
36-38, 40, 41-43, 45	OUT1-OUT8	Output	OSS Output 1-8	Octal Serial Switch (OSS) low side driver output 1-8.

Table 1. 33800 Pin Definitions(continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 16.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
39	PGND3	Ground	OSS 3-8 Ground	This PGND pins provide a dedicated ground for the Octal Serial Switch (OSS) low side driver outputs 3 - 8.
44	PGND2	Ground	OSS 2 Ground	This PGND pin provides a dedicated ground for the Octal Serial Switch (OSS) low side driver output 2.
46	PGND1	Ground	OSS 1 Ground	This PGND pin provides a dedicated ground for the Octal Serial Switch (OSS) low side driver output 1.
47	REXT	Output	Resistor External Reference	The REXT pin is used to generate a reference current.
–	–	Ground	Exposed Pad Ground	The package exposed pad provides thermal conductivity for the die and should be grounded to system ground.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltage V_{PWR} V_{DD}	 V_{PWR} V_{DD}	 -1.5 to 45 -0.3 to 7.0	V_{DC}
$\overline{CS}$, SI, SO, SCLK, EN, DEFAULT, PWMx, P1, P3, P5, P7	–	-0.3 to V_{DD}	V_{DC}
Predriver Drain Voltage (VDSNS1 to VDSNS6)	V_{DSNS}	-0.3 to 60	V_{DC}
OSS Output Clamp Energy (OUT3 to OUT8)(Single Pulse) $T_{Junction}$ = 150°C, I_{OUT} = 0.45A	E_{CLAMP}	30	mJ
OSS Output Clamp Energy (OUT1 & OUT2)(Single Pulse) $T_{Junction}$ = 150°C, I_{OUT} = 0.45A	E_{CLAMP}	45	mJ
CCD1 Output Clamp Energy (Single Pulse) $T_{Junction}$ = 150°C, I_{OUT} = 0.45A	E_{CLAMP}	75	mJ
CCD2 Output Clamp Energy (Single Pulse) $T_{Junction}$ = 150°C, I_{OUT} = 0.45A	E_{CLAMP}	25	mJ
OSS Output Continuous Current (OUT1 to OUT8 Steady State) $T_{Junction}$ = 150°C	I_{OSS_SS}	350	mA
CCD1 Output Clamp Energy (CCD1_REC OUTPUT) $T_{Junction}$ = 150°C, I_{OUT} = 1.0 A	E_{CLAMP}	75	mJ
Frequency of SPI Operation (V_{DD} = 5.0V)[3]	–	4.0	MHz
ESD Voltage[1] Human Body Model Machine Model	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V
THERMAL RATINGS			
Storage Temperature	T_{STG}	-55 to 150	°C
Operating Case Temperature	T_C	-40 to 125	°C
Operating Junction Temperature	T_J	-40 to 150	°C
Power Dissipation (T_A = 25°C)[2]	P_D	1.7	W
THERMAL RESISTANCE			
Thermal Resistance Junction to Ambient Between the Die and the Exposed Die Pad	 $R_{\theta JA}$ $R_{\theta JC}$	 71 1.2	°C/W

Notes

1. ESD data available upon request. All pins tested individually. ESD1 testing is performed in accordance with the Human Body Model (AEC-Q100-002). and the Machine Model (AEC-Q100-003).
2. Maximum power dissipation at T_J =150°C junction temperature with no heat sink used.
3. This parameter is guaranteed by design but is not production tested.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 3.0V ≤ V_{DD} ≤ 5.5V, 9.0V ≤ V_{PWR} ≤ 18V, -40°C ≤ T_A ≤ 125°C, GND = 0V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT (VPWR, VDD)					
Supply Voltage Fully Operational	$V_{PWR(FO)}$	5.0	–	36	V
Supply Current All Outputs Disabled (Normal & Default Mode)	$I_{PWR(ON)}$	–	10.0	14.0	mA
Sleep State Supply Current V_{DD} ≤ 0.8 V, V_{PWR} = 18V EN ≤ 0.8 V, V_{DD} = 5.5V	 $I_{PWR(SS)}$ $I_{VDD(SS)}$	 – –	 10 2.0	 30 5.0	µA
V_{PWR} Over-voltage Shutdown Threshold Voltage[4]	$V_{PWR(OV)}$	36.5	39	44	V
V_{PWR} Over-voltage Shutdown Hysteresis Voltage	$V_{PWR(OVHYS)}$	0.5	1.5	3.0	V
V_{PWR} Under-voltage Shutdown Threshold Voltage[5]	$V_{PWR(UV)}$	3.0	4.0	4.4	V
V_{PWR} Under-voltage Shutdown Hysteresis Voltage	$V_{PWR(UVHYS)}$	100	200	650	mV
Logic Supply Voltage	V_{DD}	3.0	–	5.5	V
Logic Supply Current Static Condition	I_{DD}	180	300	525	µA
Logic Supply Under-voltage Shutdown Threshold Voltage [5]	$V_{DD(UV)}$	0.8	2.5	2.8	V
Logic Supply Under-voltage Hysteresis	$V_{DD(UVHYS)}$	100	–	650	mV
Internally Generated V_{CAL}[6]	V_{BIAS}	2.2	2.5	2.8	V
CONSTANT CURRENT SOLENOID DRIVER OUTPUT (CCD1_OUT)					
Drain-to-Source ON Resistance T_J = 125°C, V_{PWR} = 13V T_J = 25°C, V_{PWR} = 13V T_J = -40°C, V_{PWR} = 13V	$R_{DS(ON)}$	 – – –	 – 0.25 –	 0.60 – –	Ω
Internal Current Sense Resistor DAC Value = 000, $V_{CCD1REC}$ = 0.0V, $I_{CCD1OUT}$ = 100mA R_{SENSE} = $V_{CCD1OUT}$ / $I_{CCD1OUT}$	R_{SENSE}		0.7	1.2	Ω
Current Regulation DAC Value = 17C HEX +/- (3%) DAC Value = 05F HEX +/- (15%) Load Resistance = 5Ω, Load Inductance = 10mH, Dither Off	I_{CCD1}	 775 157	 800 200	 823 235	mA
Programmable Dither Frequency Programmable from 50Hz to 500Hz in 50Hz Increments after Calibration	f_{DITHER}	-10		10	%

Notes
4. Over-voltage thresholds minimum and maximum include hysteresis.
5. Under-voltage thresholds minimum and maximum include hysteresis.
6. Using the internally generated V_{CAL} increases all applicable parametric tables by +- 10%

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 3.0V ≤ V_{DD} ≤ 5.5V, 9.0V ≤ V_{PWR} ≤ 18V, -40°C ≤ T_A ≤ 125°C, GND = 0V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CONSTANT CURRENT SOLENOID DRIVER OUTPUT (CDD1_OUT) (CONTINUED)					
Programmable Dither Amplitude Peak to Peak Programmable from 0.0mA to 350mA in 50mA increments	I_{DITHER}	 -10		 10	%
CCD1 Fault Detection Voltage Threshold Outputs Programmed OFF	$V_{OUT(FLTTH)}$	 2.0	 2.5	 3.0	V
CCD1 Output Clamp Voltage Outputs Programmed OFF	V_{OC}	 50	 55	 60	V
CCD1 Output Self Limiting Current	$I_{OUT(LIM)}$	1.5	–	2.8	A
CCD1 Output Leakage Current Pull-up enabled, Dither Off, CCD1OUT = V_{OC} - 1.0V Pull-up enabled, Dither Off, CCD1OUT = V_{PWR} = 24V	$I_{CCD1(LKG)}$	 – –	 –	 8000 20	µA
CCD1 Pull Up Current Pull-up enabled, DAC = 000, CCD1OUT = CCD1REC = 2.0V	$I_{CCD1(PULLUP)}$	-60	-40	-20	µA
CCD1 Pull Down Current Pull-up disabled, DAC = 000, CCD1OUT = CCD1REC = 2.0V	$I_{CCD1(PULLDOWN)}$	20	40	60	µA
CONSTANT CURRENT SOLENOID DRIVER OUTPUT (CCD2_OUT)					
Drain-to-Source ON Resistance T_J = 125°C, V_{PWR} = 13V T_J = 25°C, V_{PWR} = 13V T_J = -40°C, V_{PWR} = 13V	RDSON	 – – –	 – 1.0 –	 2.0 – –	Ω
Internal Current Sense Resistor DAC Value = 000, $V_{CCD2REC}$ = 0V, $I_{CCD2OUT}$ = 100mA R_{SENSE} = $V_{CCD2OUT}$ / $I_{CCD2OUT}$	R_{SENSE}		3.5	5.0	Ω
Current Regulation DAC Value = 17C HEX +/- (4%) DAC Value = 05F HEX +/- (10%) Load Resistance = 32Ω, Load Inductance = 130mH, Dither Off	I_{CCD2}	 166 38.9	 173 43.2	 180 47.5	mA
Programmable Dither Frequency Programmable from 50Hz to 500Hz in 50Hz Increments after Calibration	f_{DITHER}	 -10		 10	%
Programmable Dither Amplitude Peak to Peak Programmable from 0.0mA to 90mA in 10.9mA increments	I_{DITHER}	 -10		 10	%
CCD2 Fault Detection Voltage Threshold Outputs Programmed OFF	$V_{OUT(FLTTH)}$	 2.0	 2.5	 3.0	V
CCD2 Output Clamp Voltage Outputs Programmed OFF	V_{OC}	 50	 55	 60	V
CCD2 Output Leakage Current Pull-up enabled, Dither Off, CCD2OUT = V_{OC} - 1.0V Pull-up enabled, Dither Off, CCD2OUT = V_{PWR} = 24V	$I_{CCD2(LKG)}$	 – –	 –	 8000 20	µA
CCD2 Output Self Limiting Current	$I_{OUT(LIM)}$	0.5	–	1.0	A

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 3.0V ≤ V_{DD} ≤ 5.5V, 9.0V ≤ V_{PWR} ≤ 18V, -40°C ≤ T_A ≤ 125°C, GND = 0V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CONSTANT CURRENT SOLENOID DRIVER OUTPUT (CCD2_OUT) (CONTINUED)					
CCD2 Pull Up Current Pull-up enabled, DAC = 000, CCD1OUT = CCD1REC = 2.0V	$I_{CCD2(PULLUP)}$	-60	-40	-20	µA
CCD2 Pull Down Current Pull-up disabled, DAC = 000, CCD2OUT = CCD2REC = 2.0V	$I_{CCD2(PULLDOWN)}$	20	40	60	µA
OCTAL SERIAL DRIVERS (OUT1 - 8)					
Drain-to-Source ON Resistance **(OUT1 - 2)** I_{OUT} = 0.350A, T_J = 125°C, V_{PWR} = 13V I_{OUT} = 0.350A, T_J = 25°C, V_{PWR} = 13V I_{OUT} = 0.350A, T_J = -40°C, V_{PWR} = 13V	$R_{DS(ON)}$	 – – –	 – 0.7 –	 1.4 – –	Ω
Drain-to-Source ON Resistance **(OUT3 - 8)** I_{OUT} = 0.350A, T_J = 125°C, V_{PWR} = 13V I_{OUT} = 0.350A, T_J = 25°C, V_{PWR} = 13V I_{OUT} = 0.350A, T_J = -40°C, V_{PWR} = 13V	$R_{DS(ON)}$	 – – –	 – 1.0 –	 1.7 – –	Ω
Output Self Limiting Current Output 3 to Output 8 Output 1, Output 2	$I_{OUT(LIM)}$	 1.0 4.0	 – –	 2.0 6.0	A
Output Fault Detection Voltage Threshold.[7] Outputs Programmed OFF	$V_{OUT(FLTTH)}$	 2.0	 2.5	 3.0	V
Output OFF Open Load Detection Current V_{Drain} = 18V, Outputs Programmed OFF	I_{OCO}	 40	 75	 100	µA
Output Clamp Voltage Low Side Drive I_D = 20mA	V_{OC}	 50	 55	 60	V
Output Leakage Current V_{DD} = 5.0V, V_{Drain} = 24V, Open Load Detection Current Disabled V_{DD} = 5.0V, V_{Drain} = V_{OC} - 1.0V, Open Load Detection Current Disabled V_{DD} = 0V, V_{Drain} = 24V, Device Disabled	$I_{OUT(LKG)}$	 – – –	 – – –	 20 3000 10	µA
Over-temperature Shutdown[8]	TLim	155	–	185	°C
Over-temperature Shutdown Hysteresis[8]	$TLim_{(HYS)}$	5.0	10	15	°C
SPI DIGITAL INTERFACE (SO, SI, $\overline{CS}$, SCLK)					
Input Logic High-voltage Thresholds[8]	V_{IH}	0.7 x V_{DD}	–	V_{DD} + 0.3	V
Input Logic Low-voltage Thresholds[8]	V_{IL}	GND - 0.3	–	0.2 x V_{DD}	V
Input Logic Voltage Hysteresis[8]	V_{HYS}	100	–	300	mV
Input Logic Capacitance[8]	C_{IN}	–	–	20	pF
Sleep Mode Input Logic Current[8] V_{DD} = 0.0V	$I_{LOGICSS}$	 -10	 –	 10	µA

Notes

7. Output fault detection thresholds with outputs programmed OFF. Output fault detect thresholds are the same for output open and shorts.
8. This parameter is guaranteed by design, however is not production tested.

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 3.0V ≤ V_{DD} ≤ 5.5V, 9.0V ≤ V_{PWR} ≤ 18V, -40°C ≤ T_A ≤ 125°C, GND = 0V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI DIGITAL INTERFACE (SO, SI, $\overline{CS}$, SCLK) (CONTINUED)					
Sleep Mode EN and DEFAULT Input Current V_{DD} = 0.0V, V_{EN} = 5.0V, $V_{DEFAULT}$ = 5.0V	$I_{LOGICSS}$	-10	–	10	µA
Normal Mode Input Logic Pull-down Current[9] 0.8V to 5.0V	$I_{LOGICPD}$	5.0	15	25	µA
Normal Mode DEFAULT Pull-up Current	$I_{DEFAULTPU}$	-5.0	–	-25	µA
SCLK, Tri-state SO Output 0.0V to 5.0V	I_{SCLK}, I_{TRISO}	-10	–	10	µA
$\overline{CS}$ Input Current $\overline{CS}$ = V_{DD}	I_{CS}	-10	–	10	µA
$\overline{CS}$ Pull-up Current $\overline{CS}$ = 0.0V	$I_{\overline{CS}PU}$	-5.0	–	-30	µA
$\overline{CS}$ Leakage Current to V_{DD} $\overline{CS}$ = 5.0V, V_{DD} = 0.0V	$I_{CS(LKG)}$	–	–	10	µA
SO High-state Output Voltage I_{SOHIGH} = -1.0mA	V_{SOHIGH}	V_{DD} - 0.4	–	–	V
SO Low-state Output Voltage I_{SOLOW} = 1.0mA	V_{SOLOW}	–	–	0.4	V
EN Input Pull-down Current EN = V_{DD}	I_{ENPD}	10	50	100	µA
PREDRIVER OUTPUT FUNCTION (GD1 - GD6)					
Gate Drive Output Voltage $I_{GATEDRIVE}$ = 100µA $I_{GATEDRIVE}$ = - 100µA	 $V_{GS(ON)}$ $V_{GS(OFF)}$	 5.0 –	 7.0 0.2	 9.0 0.5	V
Gate Drive Sink and Source Current	$I_{GATEDRIVE}$	–	2.0	5.0	mA
Sleep Mode Gate to Source Resistor	$R_{GS(PULLDOWN)}$	65	200	300	KΩ
Short Fault Detection Voltage Threshold V_{DD} = High, Outputs Programmed ON Programmable from 0.5V to 3.0V in 0.5V increments.	$V_{DS(FLTTH)}$	-20%		+20%	V
Open Fault Detection Voltage Threshold V_{DD} = High, Outputs Programmed OFF	$V_{DS(FLTTH)}$	2.0	2.5	3.0	V

Notes

9. Parameter applies to P1, P3, P5, P7, PWM1 to PWM6, SI and VCAL, and are guaranteed by design.

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 3.0V ≤ V_{DD} ≤ 5.5V, 9.0V ≤ V_{PWR} ≤ 18V, -40°C ≤ T_A ≤ 125°C, GND = 0V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
PREDRIVER OUTPUT FUNCTION (GD1 - GD6) (CONTINUED)					
Drain Sense Fault Detection Current Gate Drive Off, VDS = 18V	$I_{DSNS(flt\text{-}sns)}$	40	180	400	µA
Output Clamp Voltage Driver Command Off, V_{GATE} = 2.0V	V_{OC}	50	55	60	V
Sleep Mode Drain Sense Leakage Current V_{DD} = 0.0V, V_{DSNS} = 24V,	$I_{DSNS(LKG)}$	–	–	25	µA
Load Resistance Feedback Accuracy Sample and Hold After 150ms R_{EXT} = 24ohm, R_{LOAD} = 10ohm, LR_{FDBK} = VCAL*2.5*(R_{LOAD}/R_{EXT})	$LR_{FBCKACC}$	-10%	2.6	+10%	V
Load Resistance Feedback Output Voltage (V_{DSNS1} - V_{DSNS2}) ≥ 10V, PWM Diagnostics Select = 0001	$LR_{FBCKMax}$			6.0	V

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 3.0V ≤ V_{DD} ≤ 5.5V, 9.0V ≤ V_{PWR} ≤ 18V, -40°C ≤ T_A ≤ 125°C, GND = 0V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CONSTANT CURRENT SOLENOID DRIVER OUTPUT (CCD1_OUT)					
On State Open Load Detect Timer(10) Fault is detected with driver on, timer expired	$t_{ONOPENTIMER}$	6.0	12	24	ms
Off State Open Load Detect Timer(10) Fault detected with driver off & voltage threshold not achieved (Driver off timer)	$t_{OFFOPENTIMER}$	30	60	90	µs
On State Shorted Load Detect Timer(10) Fault is detected with driver switching and drain voltage remains greater than threshold for specified time.	$t_{ONSHORTTIMER}$	30	60	90	µs
Short Retry Time(10)	t_{RETRY}	10	14	24	ms
Output Slew Rate V_{BAT} = 14V, Measured from 4.0V to 10.0V V_{BAT} = 14V, Measured from 10.0V to 4.0V	 $t_{SR(RISE)}$ $t_{SR(FALL)}$	 2.0 -2.0	 3.0 -3.0	 4.0 -4.0	V/µs
Driver On Time Blanking Period(10)	$t_{BP(OFF)}$		7.0	10	µs
Driver Off Time Blanking Period(10)	$t_{BP(ON)}$		7.0	10	µs
CONSTANT CURRENT SOLENOID DRIVER OUTPUT (CCD2_OUT)					
On State Open Load Detect Timer(10) Fault is detected with driver on, timer expires (Driver on timer)	$t_{ONOPENTIMER}$	6.0	12	24	ms
Off State Open Load Detect Timer(10) Fault is detected with driver off and voltage threshold is not achieved. (Driver off timer)	$t_{OFFOPENTIMER}$	30	60	90	µs
On State Shorted Load Detect Timer(10) Fault is detected with driver switching and drain voltage remains greater than threshold for specified time.	$t_{ONSHORTTIMER}$	30	60	90	µs
Short Retry Time(10)	t_{RETRY}	10	14	24	ms
Output Slew Rate V_{BAT} = 14V, Measured from 4.0V to 10.0V V_{BAT} = 14V, Measured from 10.0V to 4.0V	 $t_{SR(RISE)}$ $t_{SR(FALL)}$	 1.5 -1.5	 – –	 4.0 -4.0	V/µs
CCD2 DAC Update Rate(10) Response time from present current level to new programmed level	$t_{RESPONSE}$	1.0			ms
Driver On Time Blanking Period(10)	$t_{BP(ON)}$		3.0	4.3	µs
Driver Off Time Blanking Period(10)	$t_{BP(OFF)}$		12	17.2	µs
OCTAL SERIAL DRIVERS (OUT1 - OUT8)					
Output On Current Limit Fault Filter Timer(10)	t_{CL}	30	50	90	µs
Output Refresh Timer(10)	t_{REF}	5.0	10	15	ms
Output On Short Circuit Fault Filter Timer(10)	t_{SC}	400	500	650	µs

Notes

10. Assumes oscillator has been calibrated using SPI Calibrate Command.

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 3.0V ≤ V_{DD} ≤ 5.5V, 9.0V ≤ V_{PWR} ≤ 18V, -40°C ≤ T_A ≤ 125°C, GND = 0V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OCTAL SERIAL DRIVERS (OUT1 - OUT8) (CONTINUED)					
Output Off Open Circuit Fault Filter Timer[11]	t_{OC}	400	500	650	µs
Output Slew Rate					V/µs
R_{LOAD} = 51Ω	$t_{SR(RISE)}$	1.0	5.0	10	
R_{LOAD} = 51Ω	$t_{SR(FALL)}$	1.0	5.0	10	
P1 Input Propagation Delay					µs
Input @ 50% V_{DD} to Output voltage 10% of final value	$t_{(RISEDELAY)}$			6.0	
Input @ 50% V_{DD} to Output voltage 90% of initial value	$t_{(FALLDELAY)}$			6.0	
P3, P5, P7 Input Propagation Delay					µs
Input @ 50% V_{DD} to Output voltage 10% of final value	$t_{(RISEDELAY)}$			5.0	
Input @ 50% V_{DD} to Output voltage 90% of initial value	$t_{(FALLDELAY)}$			5.0	
OSCILLATOR AND TIMER ACCURACY					
Calibrated Timer Accuracy[11]	t_{TIMER}	–	–	±10	%
Un-calibrated Timer Accuracy	t_{TIMER}	–	–	±80	%
SPI DIGITAL INTERFACE TIMING (SO, SI, $\overline{CS}$, SCLK)[12]					
Required Low State Duration on V_{PWR} for Reset[13]	t_{RESET}				µs
V_{PWR} ≤ 0.2V		1.0	–	–	
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK	t_{LEAD}				ns
Required Setup Time		100	–	–	
Falling Edge of SCLK to Rising Edge of $\overline{CS}$	t_{LAG}				ns
Required Setup Time		50	–	–	
SI to Rising Edge of SCLK	$t_{SI(SU)}$				ns
Required Setup Time		16	–	–	
Rising Edge of SCLK to SI	$t_{SI(HOLD)}$				ns
Required Hold Time		20	–	–	
SI, $\overline{CS}$, SCLK Signal Rise Time[14]	$t_{R(SI)}$	–	5.0	–	ns
SI, $\overline{CS}$, SCLK Signal Fall Time[14]	$t_{F(SI)}$	–	5.0	–	ns
Time from Falling Edge of $\overline{CS}$ to SO Low-impedance[15]	$t_{SO(EN)}$	–	–	150	ns
Time from Rising Edge of $\overline{CS}$ to SO High-impedance[16]	$t_{SO(DIS)}$	–	–	150	ns
Time from Falling Edge of SCLK to SO Data Valid[17]	t_{VALID}	–	25	150	ns
Sequential Transfer Rate	t_{STR}			1.0	µs
Time required between data transfers					

Notes
11. Assumes oscillator has been calibrated using SPI Calibrate Command
12. These parameters are guaranteed by design. Production test equipment uses 1MHz, 5.0V SPI interface.
13. This parameter is guaranteed by design, however it is not production tested.
14. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals for design consideration to prevent the occurrence of double pulsing.
15. Time required for valid output status data to be available on SO pin.
16. Time required for output states data to be terminated at SO pin.
17. Time required to obtain valid data out from SO following the fall of SCLK with 200pF load.

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 3.0V ≤ V_{DD} ≤ 5.5V, 9.0V ≤ V_{PWR} ≤ 18V, -40°C ≤ T_A ≤ 125°C, GND = 0V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
PREDRIVER OUTPUT FUNCTION (GD1 - GD6)					
Open Fault Detection Filter Timer[18] V_{DD} = High, Outputs Programmed OFF	$V_{DS(FLTTH)}$	100	128	400	µs
Short Fault Detection Filter Timer[18] V_{DD} = High, Outputs Programmed ON Programmable from 30µs to 960µs in replicating increments.	$t_{DS(FLTTMR)}$	-10%		+10%	µs
Gate Drive Rise Slew Rate Cload = 1.0nF, VGS from 0.5 to 5.0V	$t_{GDSR(RISE)}$	–	1.7	–	V/µs
Gate Drive Fall Slew Rate Cload = 1.0nF, VGS from 5.0 to 0.5V	$t_{GDSR(FALL)}$	–	1.7	–	V/µs
PWM1 to PWM6 Input Propagation Delay Measured from PWM input at 4.5V and GDx output at 0.5V.	$t_{PWMDELAY}$	20		300	ns
Load Resistance Feedback Output Rise Slew Rate C_{LOAD} = 40pF	$t_{LRSR(RISE)}$	0.5	–	2.0	V/µs
Load Resistance Feedback Output Fall Slew Rate C_{LOAD} = 40pF	$t_{LRSR(FALL)}$	0.5	–	2.0	V/µs
Load Resistance Sample Duration[18]	$t_{LOADSAMPLE}$			200	µs
Load Resistance Feedback Valid [18] Time from rising edge of $\overline{CS}$ to Load Resistance measurement valid	$t_{FDBKVALID}$			400	us

Notes

18. Assumes oscillator has been calibrated using SPI Calibrate Command.

TIMING DIAGRAMS

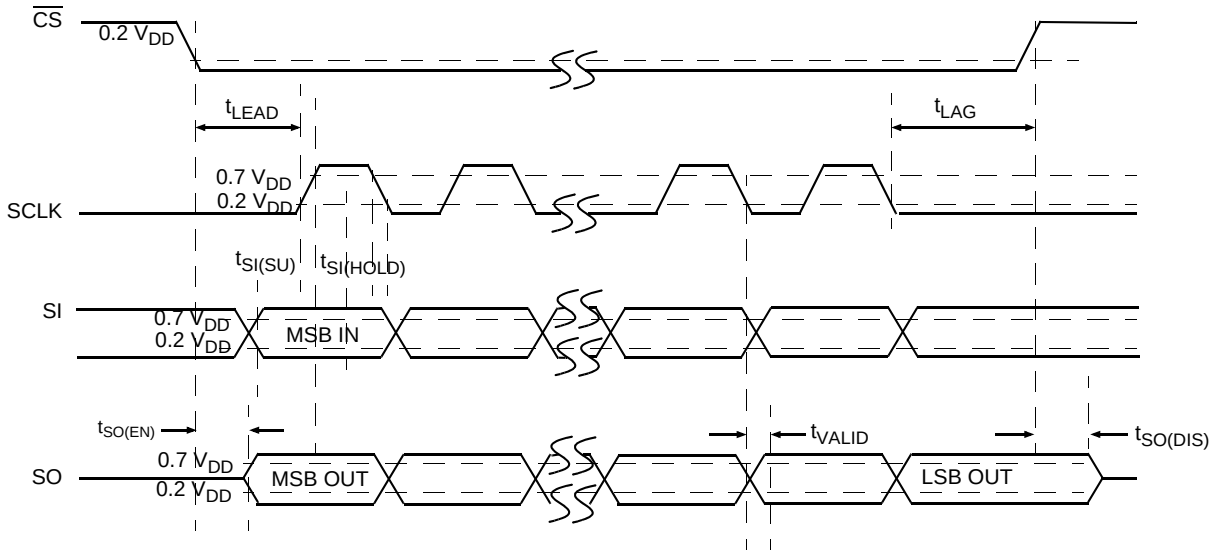

Figure 4. SPI Timing Characteristics

FUNCTIONAL DESCRIPTION

FUNCTIONAL PIN DESCRIPTION

ANALOG VOLTAGE SUPPLY (VPWR)

The VPWR pin is battery input to the 33800 IC. The VPWR pin requires external reverse battery and transient protection. Maximum input voltage on VPWR is 45V. All IC analog current and internal logic current is provided from the VPWR pin. With V_{DD} and EN applied to the IC, the application of V_{PWR} will perform a Power-ON Reset (**POR**).

DIGITAL VOLTAGE SUPPLY (VDD)

The VDD input pin is used to determine communication logic levels between the microprocessor and the 33800 device. Current from V_{DD} is used to drive SO output and pull-up current for $\overline{CS}$. V_{DD} must be applied for Normal Mode operation. Removing V_{DD} from the IC will place the device in Sleep Mode. Power-ON Reset will be performed with the application of V_{DD} supply.

GROUND (GND)

The GND pin provides a low current analog ground for the IC. The VPWR and VDD supplies are both referenced to the GND pin. GND pin should be used for decoupling both supplies.

CONSTANT CURRENT DRIVER GROUND (CCDX_GND)

The Constant Current Driver Ground (CCDX_GND) pins provide dedicated grounds for the Constant Current output drivers. Both CCDX_GND1 and CCDX_GND2 grounds are isolated from the other grounds of the IC.

GROUND (PGND1 - 3, CCD1_GND, CCD2_GND)

There are three PGND pins associated with the OSS drivers. OUT1 driver and OUT2 driver have dedicated PGND1 & PGND2 pins. Drivers OUT3 through Driver OUT8 share one PGND3 pin. In general all ground pins must be connected together and terminated to ground on the circuit board.

SOURCE VOLTAGE SENSE (VSSNS123, VSSNS456)

The Source Sense Ground pins (VSSNS123, VSSNS456) provide dedicated grounds for the hex MOSFET pre-drivers. The pins are used by the IC to monitor the drain to source voltage of the external MOSFET. This pin must be connected to the source of the external MOSFET and system ground. VSSNS123 and VSSNS456 ground pins are isolated from other internal IC grounds.

SERIAL CLOCK INPUT (SCLK)

The system clock (SCLK) pin clocks the internal shift register of the 33800. The SI data is latched into the input shift register on the rising edge of SCLK signal. The SO pin shifts status bits out on the falling edge of SCLK. The SO data is available for the MCU to read on the rising edge of SCLK. With $\overline{CS}$ in a logic high state, signals on the SCLK and SI pins will be ignored and the SO pin is tri-state.

CHIP SELECT ($\overline{CS}$)

The system MCU selects the 33800 to receive communication using the chip select ($\overline{CS}$) pin. With the $\overline{CS}$ in a logic low state, command words may be sent to the 33800 via the serial input (SI) pin, and status information is received by the MCU via the serial output (SO) pin. The falling edge of $\overline{CS}$ enables the SO output and transfers status information into the SO buffer.

Rising edge of the $\overline{CS}$ initiates the following operation:

1. Disables the SO driver (high-impedance)
2. Activates the received command word, allowing the 33800 to activate/deactivate output drivers.

To avoid any spurious data, it is essential the high-to-low and low-to-high transitions of the $\overline{CS}$ signal occur only when SCLK is in a logic low state. Internal to the 33800 device is an active pull-up to VDD on $\overline{CS}$. In cases were voltage exists on $\overline{CS}$ without the application of V_{DD}, no current will flow from $\overline{CS}$ to the VDD pin.

SERIAL INPUT DATA (SI)

The SI pin is used for serial instruction data input. SI information is latched into the input register on the rising edge of SCLK. A logic high state present on SI will program a *one* in the command word on the rising edge of the $\overline{CS}$ signal. To program a complete word, 16-bits of information must be entered into the device.

SERIAL OUTPUT DATA (SO)

The SO pin is the output from the shift register. The SO pin remains tri-stated until the $\overline{CS}$ pin transitions to a logic low state. All normal operating drivers are reported as zero, all faulted drivers are reported as one. The negative transition of $\overline{CS}$ enables the SO driver.

The SI/SO shifting of the data follows a first-in-first-out protocol, with both input and output words transferring the most significant bit (MSB) first.

ENABLE (EN)

The ENABLE pin is an active high digital input pin used to enable the device. With the EN pin low the device is in Sleep Mode. With the EN pin high, the device is in Normal Mode (V_{DD} and V_{PWR} applied). Exit from Sleep Mode initiates a

Power On Reset (POR). All internal registers will be placed in the reset state. The device has an Internal 100 kΩ resistor pull down on the ENABLE pin.

PULSE WIDTH MODULATION (PWM)

The PWM pins are control input pins for the MOSFET pre-drivers. The PWM pins provide parallel control and can be programmed for an OR function with the SPI bit or an AND function with the SPI bit (See Table 12, on page 25 for SPI message detail). Each PWM input pin has an internal 15µA pull down current source. The current sources are active when the device is in Normal Mode.

DRAIN VOLTAGE SENSE (VDSNSX)

The VDSNSx pin has multiple functions for control and diagnostics of the external MOSFET:

1. By monitoring the drain voltage of the external device, short circuits and open circuits are detected. The filter timer and threshold voltage are easily programmed through SPI (see Table 10, on page 23 and Table 11, on page 24 for SPI messages).
2. The VDSNSx pins are use to determine the external load resistance. Further information is provided in the Device Operation section of this specification.
3. The VDSNSx pins provide a drain to gate clamp for fast turn off of inductive loads and MOSFET protection.

GATE DRIVER OUTPUTS (GDX)

The GDX pins are the gate drive outputs for an external MOSFETS. Internal to the device is a Gate to Source resistor designed to hold the external MOSFET in the OFF state while the device is in POR.

INPUTS (P1, P3, P5, P7)

The input pins for octal serial switch outputs 1,3,5,7. Each input control pin has an internal pull down current source. Two outputs may be controlled in parallel using the PX pins (See Functional Device Operation on page 25).

VOLTAGE CALIBRATED INPUT (VCAL)

The Voltage calibrated input (VCAL) provides the IC with a reference voltage for analog circuits. VCAL (EXT or INT) must be applied for the CCD1 and CCD2 constant current controllers and Load Resistance measurement function to operate. For applications where measurements are not critical, the VCAL pin may grounded and an internally generated reference will be used. Using the internally generated reference will add ±10% to all tolerances in the parametric table.

LOAD RESISTANCE FEEDBACK (LRFDBK)

The LRFDBK pin is an operational amplifier output. The amplifier output voltage is proportional to the load resistance for the selected channel. The channel is selected via the SPI.

DEFAULT

The DEFAULT input controls the operation of each driver to a Default Mode. The DEFAULT input must be logic 0 for full function of all output drivers. For more information on the DEFAULT operation (See Functional Device Operation on page 19).

With the DEFAULT pin HIGH, the device is placed in Default Mode. The DEFAULT pin is pulled up to the VDD supply through an active pull up current source. In Default Mode the device operates in the following manner:

1. OSS outputs are disabled.
2. CCD1 and CCD2 outputs are disabled.
3. SPI ON/OFF control of GATE DRIVE (GD1 to GD6) outputs and on board PWM controllers are disabled. PWMx input control is enabled.

In the Default Mode the device retains all register information and output status information. Normal operation will resume when the DEFAULT pin transitions low again and the device will operate as programmed prior to Default Mode.

RESISTOR EXTERNAL REFERENCE (REXT)

The reference current is used in the equation to calculate the load resistance of the PWM outputs. The load resistance measurement current is inversely proportional to REXT current. The resistor value may be changed to adjust the load measurement current. A 24Ω resistor to ground sets the LRFDBK output to 260mV/Ω.

EXPOSED PAD

The silicon die is epoxy attached to the top side of the pad. Although the device does not use the pad for electrical conduction, the bottom side exposed pad of the package should be grounded.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

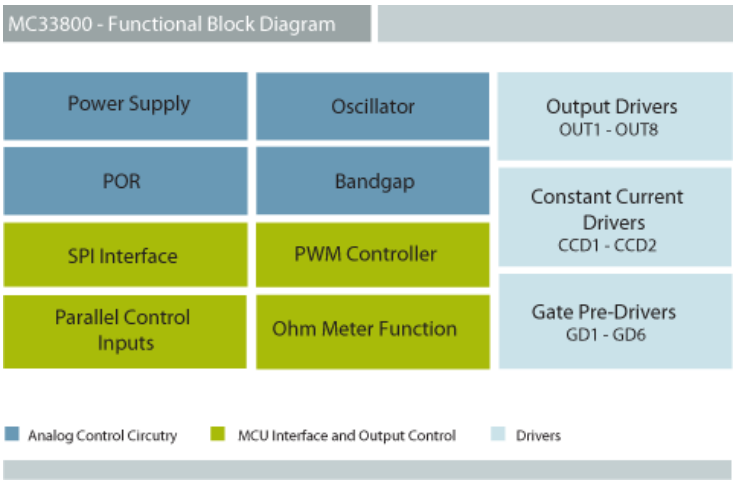

Figure 5. Functional Block Diagram

ANALOG CONTROL CIRCUITRY

The 33800 is designed to operate from 5.0 to 36V on the VPWR pin. The VPWR pin supplies power to all internal regulators, analog and logic circuit blocks. The VDD supply is used for setting communication threshold levels and supplying power to the SO driver. This IC architecture provides low quiescent current Sleep Modes. Applying VPWR to the device will cause a Power On Reset (POR). The on-chip oscillator supports the selectable PWM frequency and duty cycle. The on-chip voltage regulator and bandgap supply the required voltages to the internal circuitry.

MCU INTERFACE AND OUTPUT CONTROL

The device is designed with six flexible PWM gate driver outputs. Each driver may be controlled directly from the MCU and may be programmed through the SPI for a specific frequency and duty cycle.

LOW–SIDE DRIVERS: OUT1 – OUT8

The 33800 provides flexible control of 8 low side driver outputs. Outputs 1 and 2 are specifically designed with higher current limits to accommodate lamp inrush current. The device allows for parallel control of the outputs or SPI control through the use of several input command words.

CONSTANT CURRENT LOW SIDE DRIVERS: CCD1 AND CCD2

The CCD1/CCD2 constant current controllers are switching hysteretic current controllers with a superimposed dither. The controllers are designed to provide a programmable constant current through a solenoid valve. Fluid flow is controlled by the amount of current run through the driven solenoid valve.

GATE PRE-DRIVERS: GD1 – GD6

The GD1 – GD6 pins are the gate drive outputs for external MOSFETS. They can be PWM'ed with speed and duty cycle choices per the SPI command registers. Internal to the device is a Gate to Source resistor designed to hold the external MOSFET in the OFF state while the device is in POR.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

POWER SUPPLY

The 33800 is designed to operate from 5.0 to 36V on the VPWR pin. The VPWR pin supplies power to all internal regulators, analog and logic circuit blocks. The V_{DD} supply is used for setting communication threshold levels and supplying power to the SO driver. This IC architecture provides flexible microprocessor interfacing with low quiescent current Sleep Modes.

POWER-ON RESET (POR)

Applying V_{PWR}, V_{DD} and EN to the device will cause a Power On Reset (POR) and place the device in Normal or Default Mode.

Table 5. Modes of Operation

V_{PWR}	V_{DD}	ENable	DEFAULT	MODE
L	X	X	X	Power Off
H	L	X	X	SLEEP
H	H	L	X	SLEEP
H	H	H	L	NORMAL
H	H	H	H	DEFAULT

Command register settings from Power-ON Reset (POR) via V_{PWR} or V_{DD} are as follows:

- All Outputs Off
- Inputs Enabled and OR'd with SPI Bit.
- PWM Frequency and Duty Cycle Control Disabled.
- OSS Open Load Detect Current Enabled.
- OSS Outputs with Individual Control.
- Control Inputs P1,P3,P5,P7 Enabled and OR'd with the SPI Bit.
- CCD1 Output Off, Diagnostic Pull-up Enabled, DAC = 0.
- CCD2 Output Off, Diagnostic Pull-up Enabled, DAC = 0.

Power On Reset circuit incorporates a 0.5µs timer to prevent high frequency transients from causing a POR. During the low-voltage condition, internal logic states are maintained. To guarantee a POR from V_{PWR}, the VPWR pin must be less than 0.2V for greater than 1.0µs.

MODES OF OPERATION

The 33800 has three operating modes, Normal, Sleep and Default Mode. A discussion on Normal Mode follows.

NORMAL MODE

Normal Mode allows full functional control of the device. Transferring from Sleep Mode to Normal Mode performs a POR and resets all internal registers to the POR state. When entering Normal Mode from Default Mode, no POR is performed and register states are maintained.

Features programmed in Normal Mode are listed below. Further explanation of each feature is provided in subsequent paragraphs.

- Programmable PWM Frequency & Duty Cycle
- Programmable PWM Drain Fault Threshold
- CCD2 Constant Current Dither Frequency and Amplitude
- CCD2 DAC Programming
- CCD1 Constant Current Dither Frequency and Amplitude
- CCD1 DAC Programming
- On/Off OSS Open Load Detect Current
- Calibration of Timers (*Calibration Command*)
- Reset (*Reset Command*)
- No Operation (*NO_OP Command*)

DEFAULT MODE

The Default Mode allows the user to disable all outputs except the PWM pre-driver. In Default Mode the PWM pre-driver outputs may only be controlled via the PWM input pins. All register control bits and fault bits are maintained in Default Mode, however control for the pre-driver is accomplished through the PWM pins only.

With the DEFAULT pin HIGH, the device is placed in Default Mode. When exiting Default Mode, output control reverts to the internal register settings.

In Default Mode the device operates with the following parameters.

1. OSS outputs are disabled.
2. CCD1 and CCD2 outputs are disabled.
3. SPI ON/OFF control of GATE DRIVE (GD1 to GD6) outputs is disabled. PWMx input control is enabled. The device will operate as programmed prior to Default Mode.

In Default Mode the device retains all register information and output status information. Normal operation will resume when the DEFAULT pin transitions low again.

SLEEP MODE

Sleep Mode is entered by placing a logic [0] on the ENABLE or VDD pins. All outputs are commanded off and the device enters a low quiescent current state.

LOGIC COMMANDS AND REGISTERS

SPI AND MCU INTERFACE DESCRIPTION

The 33800 device directly interfaces to a 3.3 or 5.0V microcontroller unit (MCU) using 16 bit Serial Peripheral Interface (SPI) protocol. SPI serial clock frequencies up to 4.0MHz may be used when programming and reading output status information (production tested at 1MHz). Figure 6 illustrates the serial peripheral interface (SPI) configuration between an MCU and one 33800.

Command data is sent to the 33800 device through the SI input pin. As data is being clocked into the SI pin, status information is being clocked out of the device by the SO output pin. The response data received by the MCU during SPI communication depends on the previous SPI message sent to the device. The next SO response data is listed at the bottom of each command table (Table 7, on page 22, Table 12, on page 25, Table 22, on page 30 Table 23, on page 31, Table 26, on page 34.

SPI Integrity Check

Checking the integrity of the SPI communication with the initial power-up of the VDD and EN pins is recommended. After initial system start-up or reset, the MCU will write one 32-bit pattern to the 33800. The first 16-bits read by the MCU will be the fault status (SO message 1) of the outputs. The second 16-bits will be the same bit pattern sent by the MCU. By the MCU receiving the same bit pattern it sent, bus integrity is confirmed. The second 16-bit pattern the MCU sends to the device is the a command word and will be operated on by the device accordingly on rising edge of $\overline{CS}$.

Important A SCLK pulse count strategy has been implemented to ensure integrity of SPI communications. SPI messages consisting of 16 SCLK pulses and multiples of 8 clock pulses thereafter will be acknowledged. SPI messages consisting of other than 16 + multiples of 8 SCLK pulses will be ignored by the device.

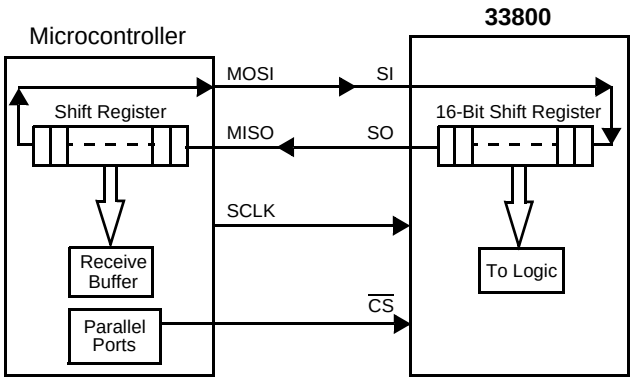

Figure 6. SPI Interface with Microprocessor

Two or more 33800 devices may be used in a module system. Multiple ICs may be SPI-configured in parallel or serial. Figures 7 and 8 show the configurations. When using the serial configuration, 32-clock cycles are required to transfer data in/out of the ICs.

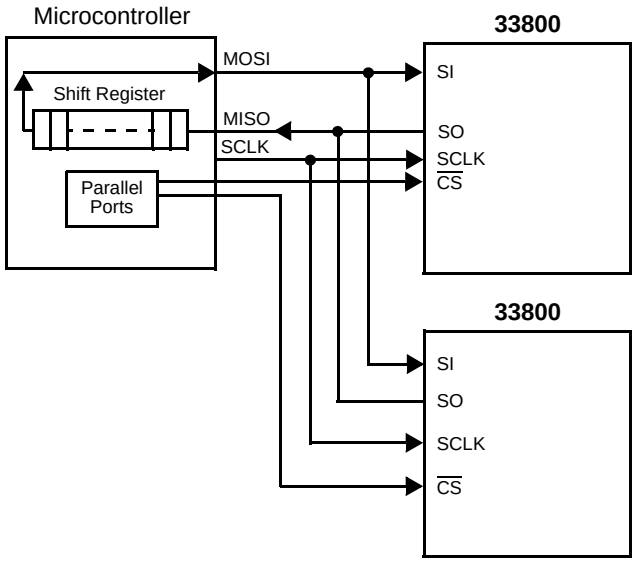

Figure 7. SPI Parallel Interface with Microprocessor

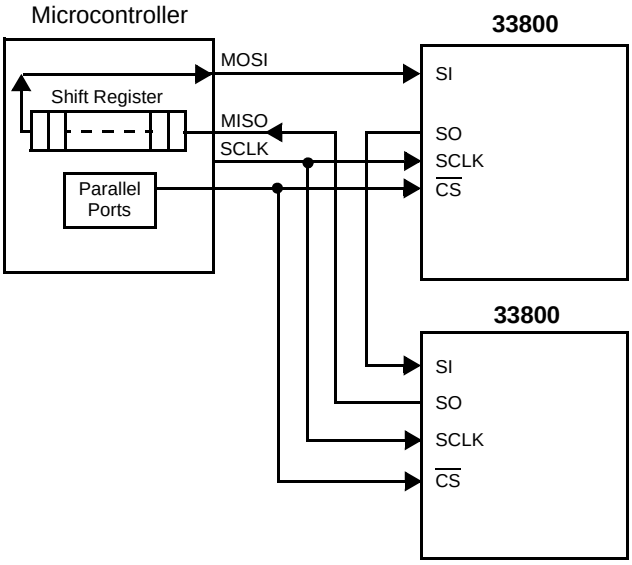

Figure 8. SPI Serial Interface with Microprocessor

PROGRAMMABLE PWM GATE DRIVER OUTPUTS

The 33800 device is designed with six flexible PWM gate driver outputs. Each driver may be controlled directly from the MCU or may be programmed through the SPI for a specific frequency and duty cycle.

The pre-drivers are designed with four diagnostic features:

- Off State Open Load Detect
- On State Short Circuit Detect
- Programmable Drain Threshold and Timer for Short Fault Detection
- Load Resistance Measurement

Each pre-driver is capable of detecting an open load in the off state and shorted load in the on state. All faults are reported through SPI communication. For open load detection, a resistor is placed between the drain sense pin and source sense pin of the IC. An open load fault is reported when the drain voltage is less than the 2.5V threshold. A shorted load fault is reported when the drain voltage is greater than the programmed threshold voltage. Programming of the drain short fault threshold voltage is done through SPI commands provided in Table 7.

Bits 6 through 9 are used to perform the load resistance measurement function as described in the Gate Drive On/Off Command section below.

GATE DRIVE ON/OFF COMMAND

The GD ON/OFF Command provides control bits for two functions:

- On/Off control of the GDx outputs.
- Load Resistance measurement function.

On/Off control bit 0 through bit 5 control gate drive outputs GD1 through GD6 respectively. Setting the bit to logic1 will enable the gate drive to the external MOSFET. Setting the bit to logic 0 will actively pull the gate to ground.

GD ON/OFF Command bits 6 through 9 control the load measurement feature. The gate drive pre-drivers are selected in matched pairs. Selecting a load resistance measurement disables a specified output pair and performs the resistance measurement using the defined pair. All other outputs will operate as programmed. Resistance is measured by passing a known current through the load and by measuring the voltage across it. The resistor placed on the REXT pin determines the current through the load during measurement. The voltage output on the LRFDBK pin is the differential load voltage with the defined current through it. From the two parameters, the load resistance may be calculated. Table 6 illustrates the load diagnostic multiplex function.

Table 6. Load Resistance Measurement Select

Bits 9876	MUX Select
0000	Normal Operation
0001	V_{DSNS1} to R_{EXT}, V_{DSNS2} to Diff-Amp +
0010	V_{DSNS2} to R_{EXT}, V_{DSNS1} to Diff-Amp +
0011	V_{DSNS3} to R_{EXT}, V_{DSNS4} to Diff-Amp +
0100	V_{DSNS4} to R_{EXT}, V_{DSNS3} to Diff-Amp +
0101	V_{DSNS5} to R_{EXT}, V_{DSNS6} to Diff-Amp +
0110	V_{DSNS6} to R_{EXT}, V_{DSNS5} to Diff-Amp +
0111	Normal Operation
1000	Normal Operation
1001	Normal Operation
1010	V_{DSNS2} to R_{EXT}, V_{DSNS1} to Diff-Amp +
1011	V_{DSNS3} to R_{EXT}, V_{DSNS1} to Diff-Amp +
1100	V_{DSNS4} to R_{EXT}, V_{DSNS1} to Diff-Amp +
1101	V_{DSNS5} to R_{EXT}, V_{DSNS1} to Diff-Amp +
1110	V_{DSNS6} to R_{EXT}, V_{DSNS1} to Diff-Amp +
1111	Normal Operation

PWM PIN ENABLE COMMAND

The PWM Pin Enable Command provides control bits for two functions:

- Enable or Disable of PWM input pins.
- Enable or Disable of the internal PWM controller for GD1 through GD6.

PWM pin Enable bit 0 through bit 5 enable or disable the PWM1 through PWM6 input pins respectively. A logic 0 in the SPI word will enable the PWM input pin, while logic 1 in the SPI word will disable the PWM input pin. Default state is with the PWM input pin enabled. With the PWM input pin disabled, the AND/OR function is also disabled and control is achieved through the Gate Drive ON/OFF command or the internal PWM controller.

AND/OR COMMAND

The AND/OR Command provides control bits for two functions:

- Determines AND/OR relation between ON/OFF SPI bit and PWM input pin.
- Enable or Disable of the internal PWM controller for G1 through GD6.

The AND/OR command describes the condition by which the PWM input pin controls the output driver. A logic[0] in the AND/OR register will OR the PWM input pin with the respective bit in the ON/OFF register. Likewise, a logic[1] in

the AND/OR register will AND the PWM input pin with the respective bit in the ON/OFF register. The AND/OR function is disabled when the PWM input pin is disabled.

Table 7. PWM Command

PWM Commands	Control Address					Command Bits										
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							R_{ld} Load Resistance Measurement Select				Gate Drive ON/OFF Bit					
GDX ON/OFF Command 0 = Off, 1 = On	0	1	0	0	1	X	0	0	0	0	0	0	0	0	0	0
								PWM Controller Enable Bit			PWM Pin Enable Bit					
PWM Pin Enable Command 0 = PWMX Pin Enabled 1 = PWMX Pin Disabled	0	1	0	1	0	X	X	0 PWM3	0 PWM2	0 PWM1	0	0	0	0	0	0
AND/OR Command 0 = PWMX Pin OR with SPI 1 = PWMX Pin AND with SPI	0	1	0	1	1	X	X	0 PWM6	0 PWM5	0 PWM4	0	0	0	0	0	0
Command	Control Address						Frequency Select			Duty Cycle Select						
PWM1 Freq & DC	0	1	1	0	0	X	0	0	0	0	0	0	0	0	0	0
PWM2 Freq & DC	0	1	1	0	1	X	0	0	0	0	0	0	0	0	0	0
PWM3 Freq & DC	0	1	1	1	0	X	0	0	0	0	0	0	0	0	0	0
PWM4 Freq & DC	0	1	1	1	1	X	0	0	0	0	0	0	0	0	0	0
PWM5 Freq & DC	1	0	0	0	0	X	0	0	0	0	0	0	0	0	0	0
PWM6 Freq & DC	1	0	0	0	1	X	0	0	0	0	0	0	0	0	0	0
	Control Address							V_{DSNS3}			V_{DSNS2}			V_{DSNS1}		
VDSNS123 Short Threshold	1	0	0	1	0	X	X	0	1	1	0	1	1	0	1	1
VDSNS123 Short Timer	1	0	0	1	1	X	X	0	1	1	0	1	1	0	1	1
	Control Address							V_{DSNS6}			V_{DSNS5}			V_{DSNS4}		
VDSNS456 Short Threshold	1	0	1	0	0	X	X	0	1	1	0	1	1	0	1	1
VDSNS456 Short Timer	1	0	1	0	1	X	X	0	1	1	0	1	1	0	1	1
Next SO Response (Message 1) 0 = No Fault, 1 = Fault	OvrVlt,TLim or CAL Flt	Reset	Fault StatusPWM6	Fault StatusPWM5	Fault StatusPWM4	Fault StatusPWM3	Fault StatusPWM2	Fault StatusPWM1	Fault StatusOUT8	Fault StatusOUT7	Fault StatusOUT6	Fault StatusOUT5	Fault StatusOUT4	Fault StatusOUT3	Fault StatusOUT2	Fault StatusOUT1

Table 8. And/Or/SPI/Parallel Control

R_{load} Measure	PWM Pin EN 0 = en 1 = dis	AND/OR Bit 0 = OR 1 = AND	ON/ OFF Bit	PWM Freq/ DC EN Bit	PWM Pin	Output
≠ 0	X	X	X	X	X	Rload Measure
0	1	X	0	0	X	OFF
0	1	X	0	1	X	Freq/DC
0	1	X	1	X	X	ON
0	0	0	0	0	0	OFF
0	0	0	0	1	0	Freq/DC
0	0	0	X	X	1	ON
0	0	0	1	X	X	ON
0	0	1	0	0	X	OFF
0	0	1	X	0	0	OFF
0	0	1	0	1	X	Freq/DC
0	0	1	X	1	0	Freq/DC
0	0	1	1	X	1	ON

PWM FREQUENCY/DUTY CYCLE COMMAND

The PWM Frequency/Duty Cycle Command allows the user to individually program a PWM output with a frequency and duty cycle. Once the PWM Freq/DC registers are programmed, the PWM output GD1, GD2, GD3 are controlled via the AND/OR command and GD4, GD5, GD6 are controlled via the PWM pin Enable Command. Pre-driver output control bits supersede the internal PWM controller. GDx outputs must be commanded OFF for the controller to function. (SeeTable 8)

The duty cycle of the PWM outputs is controlled by bits 0 through 6, inclusive. The duty cycle value is 1% per binary count from 1 to 100 with counts of 101 through 127 defaulting to 100%. For example:

Sending SPI WORD; 01100x1110001100

This would set PWM1 output to 1.28Khz frequency with a 12% duty cycle.

Table 9 defines the output frequency with the selected input bits.

Table 9. Frequency Select

Frequency Select Bits 987	Frequency Hz
000	10 Hz
001	20 Hz
010	40 Hz
011	80 Hz
100	160 Hz
101	320 Hz
110	640 Hz
111	1.28 kHz

Notes: Tolerance on selected frequency is +-10% with part calibrated. On state short faults may not be detected if t_on_short > 1/f_pwm * duty_cycle * 0.98.Off state open faults may not be detected if t_off_open > 1/fpwm * (1-duty_cycle) * 0.75.

VDSNSX SHORT THRESHOLD COMMAND

The short fault threshold voltage of the external MOSFET may be programmed via SPI. Table 10 illustrates the bit pattern required for a particular short fault threshold. Open load fault detect threshold is set internally to 2.5V and may not be programmed.

Table 10. VDSNSx Fault Threshold Select

PWM V_{DS} FLT Bits 210 543 876	VDSNSx Fault Threshold Select
000	0.5V
001	1.0V
010	1.5V
011	2.0
100	2.5V
101	3.0V
110	No Change
111	No Change

VDSNSX SHORT FAULT TIMER COMMAND

The Short Fault Timer can be programmed via the SPI to the values listed in Table 11, on page 24. When the 33800 detects an over-current condition, as defined by V_{DS} exceeding the programmed short fault voltage threshold, the

33800 will wait for the Short Fault Time period and then shut down the output drive, setting the fault status bit to a 1 in the Serial Output Response Register.

Table 11. PWM Short Fault Timer

PWM FLT Timer Bits 210 543 876	Fault Timer Select
000	30µs
001	60µs
010	120µs
011	240µs
100	480µs
101	960µs
110	No Change
111	No Change

Notes: Tolerance on fault timer setting is ±10% with calibrated part.

Example: Load Measurement Operation

To perform an accurate load resistance measurement the 33800 device uses an alternate channel to determine a differential load voltage and forces a known load current. With the differential load voltage and the forced current the load resistance is calculated. As shown in Table 6, channel 2 is used as the battery reference for the load measurement of channel 1. The current through the channel 1 load is set by the external resistor. Setting the resistance to 25Ω forces a current of 100mA. The measurement is sampled within 200µs and is held for 150ms on the Load Resistance Feedback (L_{RFDBK}) output. The differential amplifier has a fixed gain of 2.5V. Hence for this example, a 10Ω load will produce a 2.5V output. When a second pair is selected for measurement, the sample and hold is reset and the measurement is immediately directed to the new load measurement. The previous pair immediately revert back to normal operation.

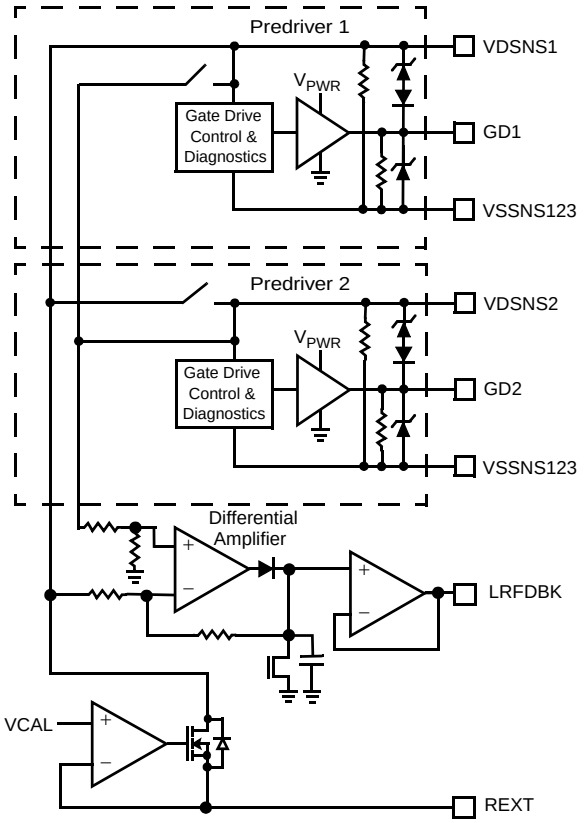

Figure 9. Example of Channel 1 Measurement

OCTAL OUTPUT DRIVER (OCTAL SERIAL SWITCH; OSS)

The 33800 provides flexible control of 8 low side driver outputs. Outputs 1 and 2 are specifically designed with higher current limit to accommodate lamp inrush current. The device allows for parallel control and/or SPI control through the use of several input command words. This section describes the logic operation and commands for the octal driver.

The 33800 Octal Output Driver message set consists of eight commands, and one response as shown in Table 12. Bits 11 through 15 determine the specific command and bits 0 through 10 determine how a specific output will operate. The 33800 operates on the command word on the rising edge of $\overline{CS}$. The Most Significant Bit (MSB) is sent and received first.

Note Upon Power-ON Reset all OSS bits are defined as shown in Table 12.

Table 12. OSS SPI Control Commands and Response

Command	Control Address					Command Bits										
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OSS ON/OFF Command 0 = off, 1 = on	0	0	0	0	1	X	X	X	0	0	0	0	0	0	0	0
Open Load Current Enable 0 = disable, 1 = enable	0	0	0	1	0	X	X	X	0	0	0	0	0	0	0	0
Shutdown/Retry from V_{PWR} Over Voltage 0 = shutdown, 1 = retry	0	0	0	1	1	X	X	X	1	1	1	1	1	1	1	1
Shutdown/Retry from Short Circuit 0 = shutdown, 1 = retry	0	0	1	0	0	X	X	X	1	1	1	1	1	1	1	1
TLim Command 0 = disable, 1 = enable	0	0	1	0	1	X	X	X	1	1	1	1	1	1	1	1
Fault Timer Command 0 = Fault Timer Disabled 1 = Fault Timer Enabled	0	0	1	1	0	X	X	X	1	1	1	1	1	1	1	1
Parallel Outputs(7&8,5&6,3&4,1&2) Parallel Input Pin Enable 0 = Individual Control, PX enabled 1 = Parallel Control, PX disabled	0	0	1	1	1	X	X	X	0 Output 7&8	0 Output 5&6	0 Output 3&4	0 Output 1&2	0 P7 en	0 P5 en	0 P3 en	0 P1 en
AND/OR Control 0 = PX Pin OR with SPI 1 = PX Pin AND with SPI	0	1	0	0	0	X	X	X	0	0	0	0	0	0	0	0
Next SO Response (Message 1) 0 = No Fault, 1 = Fault	OvrVlt,TLim or CAL Flt	Reset	Fault StatusPWM6	Fault StatusPWM5	Fault StatusPWM4	Fault StatusPWM3	Fault StatusPWM2	Fault StatusPWM1	Fault StatusOUT8	Fault StatusOUT7	Fault StatusOUT6	Fault StatusOUT5	Fault StatusOUT4	Fault StatusOUT3	Fault StatusOUT2	Fault StatusOUT1

ON/OFF CONTROL COMMAND

To program the 8 outputs of the 33800 ON or OFF, a 16-bit serial stream of data is entered into the SI pin. The first 8-bits of the control word are used to identify the on/off command and the remaining 8-bits are used to turn ON or OFF the specific output driver. When commanding an output ON or OFF, the Most Significant Bit (MSB) is sent and received first. Bit 7 corresponds to output 8 down to bit 0 which corresponds to output 1.

OPEN LOAD CURRENT ENABLE COMMAND

The Open Load Enable Command is provided to enable or disable the open load detect pull-down current. This feature allows the device to be used in LED applications. On power up reset (POR) or the RESET command the pull-down current sources are disabled. To enable the open load current source, the user must program the Open Load Current Disable Control register with logic[1]. Open load faults may not be reported with the pull-down current source disabled.

OVER-VOLTAGE SHUTDOWN/RETRY COMMAND

The Over Voltage Shutdown/Retry Command allows the user to select the fault strategy for the outputs. The over-voltage control bit sets the operation of the outputs when returning from over-voltage. Setting the over-voltage bit to logic[0] will force all outputs to remain OFF when V_{PWR} returns to normal level. Setting the over-voltage bit to logic[1] will command outputs to resume their previous state when V_{PWR} returns to normal level.

TLIM COMMAND, TIMER COMMAND

The TLim and Timer commands are used to enhance the short circuit protection strategy of the Octal Serial Switch output drivers.

The Timer protection scheme uses a low duty cycle in the event of a short circuit. The TLim protection circuit uses the

temperature of the output driver to determine the fault. Both methods may be selected or used individually. The following table provides an explanation of operation during fault condition.

The low duty cycle used for the timer protection scheme is set by the fault timer used to detect the short circuit. For short circuits detected based on the output voltage exceeding the fault detection voltage threshold, the outputs will be turned off for the duration of the refresh timer (typically 10ms) and turned on for the duration of the on-state short circuit fault timer (typically 500µs). For short circuits detected based on the output current exceeding the output current limit, the outputs will be turned off for the duration of the refresh timer (typically 10 ms) and turned on for the duration of the current limit fault timer (typically 50µs).

For off-state open load faults with retry timer enabled, the off-open fault is released and re-detected every 1-2 retry timer periods. Retry timer for 1-2, 3-4, 5-6, and 7-8 are out of phase and may report a load present, if the OSS read command $\overline{CS}$ is issued after the release, and before the re-detection (~500µs) of the off-state open load fault.

Table 13. TLim/Timer Control

Shutdn Retry Bit	TLIM Bit	Fault Timer Bit	Operation During Short Fault
1	0	X	Timer only, Outputs will retry on period OUT1-8 = ~500us for short circuit faults, and 50us for current limit faults ON, ~10ms OFF.
1	1	0	TLim only, Outputs will retry on TLim hysteresis.
1	1	1	Timer and TLim, Outputs will retry on period and driver temperature below threshold. OUT1-8 = ~500us ON, ~10ms OFF
0	0	X	Timer only, Outputs will not retry on period OUT1-8 = ~500us ON, OFF
0	1	0	TLim only, Outputs will not retry on TLim hysteresis.
0	1	1	Timer and TLim, Outputs will not retry on period or TLim. OUT1-8 = ~500us ON, OFF

All OSS outputs have a current limit control loop. Current limit is always active in Normal Mode. Current limit for OUT1 and OUT2 is 4.0 to 6.0A. Current limit for OUT3 through OUT8 is 1.0 to 2.0A.

PARALLEL OUTPUT, PX PIN ENABLE COMMAND

The Parallel Output command allows the user to parallel output for increased current capability and enables control of the PX input pin.

A logic 0 in the Parallel Output Command provides individual control. Logic 1 commands outputs to operate in parallel. For example, with bit 4 in the Parallel Output command a logic 1, outputs 1 & 2 are controlled together

With the outputs paralleled, and the P1 pin enabled, a logic 1 on SPI bit 0 or SPI bit 1 will command both outputs on. Similarly a logic 1 on the P1 pin will command both outputs on.

PX pin Enable bit 0 through bit 3 enables or disables the P1, P3, P5, P7 pins respectively. A logic 0 in the SPI word will enable the PX input pin, while logic 1 in the SPI word will disable the PX input pin. Default state is with the PX input pins enabled.

When paralleling output 1 & 2 the current limit is maintained at 4.0 to 6.0A. Parallel current limit for drivers 3&4, 5&6, 7&8 is increased to a range of 2.0 to 4.0A.

Using a MOSFET as output switches allows the connection of paired outputs. The $R_{DS(ON)}$ of MOSFET devices have inherent positive temperature coefficient providing balanced current sharing between outputs without destructive operation. This mode of operation may be desirable in the event the application requires lower power dissipation or the added capability of switching higher currents. Performance of parallel operation results in a corresponding decrease in $R_{DS(ON)}$, while the Output Current Limit increases correspondingly. Output OFF Open Load Detect current may increase based on how the Output OFF Open Load Detect is programmed.

Table 14. And/Or/SPI/Parallel Control

Parallel En Bit	PX Pin En Bit	PX Pin	AND/ OR Bit	SPI Bit 1	SPI Bit 0	Output 1&2
1	0	X	X	0	0	OFF
1	0	X	X	0	1	ON
1	0	X	X	1	0	ON
1	0	X	X	1	1	ON
1	1	0	1(or)	0	0	OFF
1	1	0	1(or)	0	1	ON
1	1	0	1(or)	1	0	ON
1	1	0	1(or)	1	1	ON
1	1	0	0(and)	X	X	OFF
1	1	X	0(and)	0	0	OFF
1	1	1	0(and)	0	1	ON
1	1	1	0(and)	1	0	ON
1	1	1	0(and)	1	1	ON

AND/OR COMMAND

The AND/OR Command provides control bits for the following function:

- Determines AND/OR relation between ON/OFF SPI bit and PX input pin.

The AND/OR command describes the condition by which the PX input pin controls the output driver. A logic[0] in the AND/OR register will OR the PX input pin with the respective bit in the ON/OFF register. Likewise, a logic[1] in the AND/OR register will AND the PX input pin with the respective bit in the ON/OFF register. The AND/OR function is disabled when the PX input pin is disabled.

SERIAL OUTPUT (SO) RESPONSE REGISTER

Fault reporting is accomplished through the SPI interface. All logic[1]s received by the MCU via the SO pin indicate fault. All logic[0]s received by the MCU via the SO pin indicate no fault. All fault bits are cleared on the positive edge of $\overline{CS}$. SO bits 15 to 0 represent the fault status of outputs 15 to 0. The timing between two write words must be greater than 450µs to allow adequate time to sense and report the proper fault status.

CCD1 CONSTANT CURRENT CONTROLLER

The CCD1 constant current controller is a switching hysteretic current controller with a superimposed dither. The controller is designed to provide a programmable constant current through a solenoid valve. Fluid flow is controlled by the amount of current run through the solenoid valve.

The master SPI device sends 16 bit command words to the 33800 device (see Table 15). The master device sets up the output current based on the CCD1 Control command. The IC is capable of sinking an average output current from 0mA to 1075mA (without dither). If operating the device with dither, the DAC + Dither value must be less than 1075mA or greater than 0.0mA. Commands outside of this command range will automatically lock out dither.

Programming the solenoid current begins by sending the CCD1 Control command. The command consists of an control address, Diagnostic Pull Up Enable bit (Diag_pu_EN), Dither Disable bit (DTHR_DIS), and a 9-bits of data for digital to analog conversion (DAC). The data is received and the DAC provides bias for a comparator to produce a threshold level. The comparator drives a switch control circuit which generates a frequency modulated signal for the output drive. The differential voltage across the sense resistor provides the feedback necessary to maintain the desired output current. The output current is continuously monitored as a differential voltage across the internal sense resistor. When the current is in recirculation and the driver is in the off state, the current will decay to the lower limit switch point. When the current reaches the lower limit, the driver will turn on to increase the current until the upper limit switch point is reached. The output current will continue to switch between the switch points, resulting in the desired average current. The switch points are set to a fixed ±5% of the commanded current. The switching frequency and accuracy are dependent upon the load inductance and resistance, battery voltage, dither amplitude and frequency, switch points and the commanded current.

Current dither is a method by which the average current is increased and decreased through the solenoid valve. The 33800 allows the user to program the frequency and amplitude of the dither control. Dither amplitude is implemented by increasing and decreasing the DAC by the programmed dither value. The rate at which the value changes is set by the programmed dither frequency. When reprogramming the dither amplitude or dither frequency, the update will occur on the start of a positive cycle.

The maximum value of the output (DAC + Dither) must be less than 1075mA. When a greater value is programmed the device will disable the dither on the output. Similarly, the minimum value of the output (DAC - Dither) must be greater than 0.0mA. Requesting a lower value will disable the dither on the output.

ON/OFF CONTROL BIT

The CCD1 output may be used as a standard 1.0A low side driver. For on/off control, the CCD1_DIS bit int the CCD1Frequency & Amplitude command must be set to logic 1. This disables the constant current driver and enables the on/off control. To turn the driver ON a logic 1 is placed in the ON/OFF control bit. A logic 0 placed in the ON/OFF control bit will turn the driver OFF.

The protection scheme in low side driver mode operates the same as constant current mode.

Table 15. CCD1 Constant Current Controller Commands

Command	Control Address					Command Bits										
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CCD1 Command Address					Diag Pull Up	DTHR DIS	9 BIT DAC Command Data								
CCD1 Control 0 = Pull Down Current Source 1 = Pull Up Current Source	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	CCD1 Command Address					CCD1 Retry	ON/ OFF	CCD1 DIS	TLim EN	Dither Amplitude			Dither Frequency			
CCD1 Frequency & Amplitude	1	0	1	1	1	1	0	0	1	0	1	1	0	1	0	0
Next SO Response (Message 2) 0 = No Fault, 1 = Fault	OvrVlt TLim or CAL Flt	Reset	Trim Set[19]	VCAL Status int=0 ext=1	Open Fault CCD2	Short Fault CCD2	Open Fault CCD1	Short Fault CCD1	Fault Status OUT8	Fault Status OUT7	Fault Status OUT6	Fault Status OUT5	Fault Status OUT4	Fault Status OUT3	Fault Status OUT2	Fault Status OUT1

Notes

19. Trim Set bit indicates (0=untrimmed, 1= trimmed)
20. VCAL Status bit indicates when internal or external supply is used. VCAL Bit = 0 indicates external, VCAL Bit = 1indicates internal.
21. Reset Bit indicates the device has performed a POR.
22. CCD1 DISable bit allows the CCD1 driver to operate as a standard 1.0A low side driver. With CCD1_DIS bit = 1 the CCD1 function is disabled.

Table 16. CCD1 Dither Frequency Select

Bits 3210	Dither Frequency
0000	Dither Off
0001	50Hz
0010	100Hz
0011	150Hz
0100	200Hz
0101	250Hz
0110	300Hz
0111	350Hz
1000	400Hz
1001	450Hz
1010	500 Hz
1011	133Hz
1100	166Hz
1101	233Hz
1110	266Hz
1111	No change
Notes: Frequencies above 250Hz are +- 20%	

Table 17. CCD1 Dither Amplitude Select

Bits 654	Dither Amplitude
000	Dither Off
001	50.4mA
010	100.8mA
011	151.2mA
100	201.6mA
101	252.0mA
110	302.4mA
111	352.8mA

CCD2 CONSTANT CURRENT CONTROLLER

The CCD2 constant current controller is a switching hysteretic current controller with a superimposed dither. The controller is designed to provide a programmable constant current through a solenoid valve. By controlling current through the solenoid valve, fluid flow control is achieved.

The master SPI device sends 16-bit command words to the 33800 device (see Table 18). The master device sets up the output current based on the CCD2 Control command. The IC is capable of sinking an average output current from 0.0mA to 232mA (without dither). If operating the device with dither, the DAC + Dither value must be less than 232mA or

greater than 0.0mA. Commands outside of this command range will automatically lock out dither.

Programming the solenoid current begins by sending the CCD2 Control command. The command consists of an control address, Diagnostic Pull-up Enable bit (Diag_pu_EN), Dither Disable bit (DTHR_DIS), and a 9-bits of data for digital to analog conversion (DAC). The data is received and the DAC provides bias for a comparator to produce a threshold level. The comparator drives a switch control circuit which generates a frequency modulated signal for the output drive. The differential voltage across the sense resistor provides the feedback necessary to maintain the desired output current. The output current is continuously monitored as a differential voltage across the internal sense resistor. When the current is recirculation and the driver is in the off state, the current will decay to the lower limit switch point. When the current reaches the lower limit, the driver will turn on to increase the current until the upper limit switch point is reached. The output current will continue to switch between the switch points, resulting in the desired average current. The switch points are set to a fixed +/-5% of the commanded current. The switching frequency and accuracy are dependent upon the load inductance and resistance, battery voltage, dither amplitude and frequency, switch points, and the commanded current.

Current dither is a method by which the average current is increased and decreased through the solenoid valve. The 33800 allows the user to program the frequency and amplitude of the dither control. Dither amplitude is implemented by increasing and decreasing the DAC by the programmed dither value. The rate at which the value is changed is set by the programmed dither frequency. When reprogramming the dither amplitude or dither frequency, the update will occur on the start of a positive cycle.

The maximum value of the output (DAC + Dither) must be less than 232mA. When a greater value is programmed, the device will disable dither on the output. Similarly, the minimum value of the output (DAC - Dither) must be greater than 0.0mA. Requesting a lower value will disable dither on the output.

Table 18. CCD2 Constant Current Controller Commands

Command	Control Address					Command Bits										
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CCD2 Command Address					Diag Pull-up	DTHR DIS	9 BIT DAC Command Data								
CCD2 Control 0 = Pull-down Current Source 1 = Pull-up Current Source	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	CCD2 Command Address					CCD2 Retry				Dither Amplitude			Dither Frequency			
CCD2 Frequency & Amplitude	1	1	0	0	1	1	X	X	X	0	1	1	0	1	0	0
Next SO Response (Message 2) 0 = No Fault, 1 = Fault	OvrVlt ,TLim or CAL Flt	Reset	Trim Set (23)	VCAL Status int=0 ext=1	Open Fault CCD2	Short Fault CCD2	Open Fault CCD1	Short Fault CCD1	Fault Status OUT8	Fault Status OUT7	Fault Status OUT6	Fault Status OUT5	Fault Status OUT4	Fault Status OUT3	Fault Status OUT2	Fault Status OUT1

Notes

23. Trim Set bit indicates (0 = untrimmed, 1 = trimmed)
24. VCAL Status bit indicates when internal or external supply is used. VCAL Bit = 0 indicates external, VCAL Bit = 1indicates internal.
25. Reset Bit indicates the device has performed a POR.

Table 19. CCD2 Dither Frequency Select

Bits 3210	Dither Frequency
0000	Dither Off
0001	50Hz
0010	100Hz
0011	150Hz
0100	200Hz
0101	250Hz
0110	300Hz
0111	350Hz
1000	400Hz
1001	450Hz
1010	500Hz
1011	133Hz
1100	166Hz
1101	233Hz
1110	266Hz
1111	No change
Notes: Frequencies above 250Hz are +- 20% - assumes part is calibrated	

Table 20. CCD2 Dither Amplitude Select

Bits 456	Dither Amplitude
000	Dither Off
001	21.8mA
010	32.7mA
011	43.6mA
100	54.5mA
101	65.4mA
110	75.3mA
111	87.2mA

Calibration Command

In cases where an accurate time base is required, the user may calibrate the internal timers using the *calibration command* (refer to Table 5). After the 33800 device receives the calibration command, the device expects a 32µs logic[0] calibration pulse on the $\overline{CS}$ pin. The pulse is used to calibrate the internal clock. SPI communication is allowed during calibration. Because the oscillator frequency changes with temperature, calibration is required for an accurate time base. The *calibration command* may be used to update the device on a periodic basis.

Table 21. Calibration Command

Command	Control Address					Command Bits										
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Calibration Command	1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X

Reset Command

The reset command resets all registers to Power-ON Reset (POR) state. Refer to Table 22, on page 30, for POR states or the paragraph entitled Power-ON Reset (POR) on page 19 of this datasheet.

Table 22. Reset Command

Command	Control Address					Command Bits										
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	1	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X
Next SO Response (Message 1) 0 = No Fault, 1 = Fault	OvrVlt ,TLim or CAL Flt	Reset	Fault Status PWM 6	Fault Status PWM 5	Fault Status PWM 4	Fault Status PWM 3	Fault Status PWM 2	Fault Status PWM 1	Fault Status OUT8	Fault Status OUT7	Fault Status OUT6	Fault Status OUT5	Fault Status OUT4	Fault Status OUT3	Fault Status OUT2	Fault Status OUT1

No Operation Command

Sending these two commands perform no operation. The device outputs will remain in previous state.

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Table 23. No Operation Command

Command	Control Address					Command Bits										
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NO Operation	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X
NO Operation	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X
Next SO Response (Message 1) 0 = No Fault, 1 = Fault	OvrVlt,TLim or CAL Flt	Reset	Fault StatusPWM6	Fault StatusPWM5	Fault StatusPWM4	Fault StatusPWM3	Fault StatusPWM2	Fault StatusPWM1	Fault StatusOUT8	Fault StatusOUT7	Fault StatusOUT6	Fault StatusOUT5	Fault StatusOUT4	Fault StatusOUT3	Fault StatusOUT2	Fault StatusOUT1

FAULT OPERATION

On each SPI communication, a 16-bit command word is sent to the 33800 and a 16-bit status word is received from the 33800.

The Most Significant Bit (MSB) is sent and received first.

Command Register Definition:
0 = Output Command Off
1 = Output Command On

SO Definition:
0 = No fault
1 = Fault

Table 24. Fault Operation

Serial Output (SO) Pin Reports

Over-current	SO Pin reports short-to-battery/supply or over-current condition.
Output ON Open Load Fault	Not reported on GDX and OUTX outputs. Reported on CCD1 and CCD2 outputs
Output OFF Open Load Fault	SO Pin reports output “OFF” open load condition.

Device Shutdowns

Over-voltage	Total device shutdown at V_{PWR} = 36.5 to 44V. Resumes normal operation with proper voltage. Upon recovery all outputs assume previous state or OFF based on the over-voltage bit in the Shutdown/Retry Control register.
Over-current	OUTX & CCDX outputs will remain in current limit until t_{SC} limit is reached. With TLim enabled, OUTX & CCDX outputs will remain in current limit until TLim is reached.

SPI Command Summary

Table 25 below provides a comprehensive list of SPI commands recognized by device 33800 and the reset state of each register.

Table 25. SPI Commands

Command Name	**Control Address**					**Command Bits**										
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MISCELLANEOUS																
Common Commands																
Calibration Command	1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X

Table 25. SPI Commands

Command Name	Control Address					Command Bits										
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset	1	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X
NO Operation	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X
NO Operation	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X
OSS COMMANDS																
OSS_X Commands									OUT 8	OUT 7	OUT 6	OUT 5	OUT 4	OUT 3	OUT 2	OUT 1
OSS ON/OFF 1 = on, 0 = off	0	0	0	0	1	X	X	X	0	0	0	0	0	0	0	0
Open Load Current Enable 0 = enable, 1 = disable	0	0	0	1	0	X	X	X	0	0	0	0	0	0	0	0
Shutdown/Retry from V_{PWR} Over-voltage 0 = shutdown, 1 = retry	0	0	0	1	1	X	X	X	1	1	1	1	1	1	1	1
Shutdown/Retry from Short Circuit 0 = shutdown, 1 = retry	0	0	1	0	0	X	X	X	1	1	1	1	1	1	1	1
TLim Enable 1 = enable, 0 = disable	0	0	1	0	1	X	X	X	1	1	1	1	1	1	1	1
Fault Timer Enable 1 = enable, 0 = disable	0	0	1	1	0	X	X	X	1	1	1	1	1	1	1	1
Parallel Outputs Enable (7&8,5&6,3&4,1&2) 0 = Individual Control 1 = Parallel Control PX Pin Enable 0 = enable PX 1 = disable PX (SPI only)	0	0	1	1	1	X	X	X	1 Out 7 & 8	1 OUT 5 & 6	1 OUT 4 & 3	1 OUT 2 & 1	0 P7 EN	0 P5 EN	0 P3 EN	0 P1 EN
AND/OR Control 1 = PX Pin AND with SPI 0 = PX Pin OR with SPI	0	1	0	0	0	X	X	X	0	0	0	0	0	0	0	0

Table 25. SPI Commands

Command Name	Control Address					Command Bits										
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GDX COMMANDS																
							R_{LD} Load Resistance Measurement Select				Gate Drive ON/OFF Bit					
GDX ON/OFF Command 0 = Off, 1 = On	0	1	0	0	1	X	0	0	0	0	0	0	0	0	0	0
								PWM Controller Enable Bit			PWM Pin Enable Bit					
PWM Pin Enable Command 0 = PWMX Pin Enabled 1 = PWMX Pin Disabled	0	1	0	1	0	X	X	0 PWM3	0 PWM2	0 PWM1	0	0	0	0	0	0
AND/OR Command 0 = PWMX Pin OR with SPI 1 = PWMX Pin AND with SPI	0	1	0	1	1	X	X	0 PWM6	0 PWM5	0 PWM4	0	0	0	0	0	0
							Frequency Select			**Duty Cycle Select**						
PWM1 Freq & Duty Cycle	0	1	1	0	0	X	0	0	0	0	0	0	0	0	0	0
PWM2 Freq & Duty Cycle	0	1	1	0	1	X	0	0	0	0	0	0	0	0	0	0
PWM3 Freq & Duty Cycle	0	1	1	1	0	X	0	0	0	0	0	0	0	0	0	0
PWM4 Freq & Duty Cycle	0	1	1	1	1	X	0	0	0	0	0	0	0	0	0	0
PWM5 Freq & Duty Cycle	1	0	0	0	0	X	0	0	0	0	0	0	0	0	0	0
PWM6 Freq & Duty Cycle	1	0	0	0	1	X	0	0	0	0	0	0	0	0	0	0
								V_{DSNS3}			V_{DSNS2}			V_{DSNS1}		
$V_{DSNS123}$ Short Threshold	1	0	0	1	0	X	X	0	1	1	0	1	1	0	1	1
$V_{DSNS123}$ Short Timer	1	0	0	1	1	X	X	0	1	1	0	1	1	0	1	1
								V_{DSNS6}			V_{DSNS5}			V_{DSNS4}		
$V_{DSNS456}$ Short Threshold	1	0	1	0	0	X	X	0	1	1	0	1	1	0	1	1
$V_{DSNS456}$ Short Timer	1	0	1	0	1	X	X	0	1	1	0	1	1	0	1	1
CCD COMMANDS																
						Diag EN	DTHR DIS	9 BIT DAC Command Data								
CCD1 Control	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0
						CCD1 Retry	LSD ON/ OFF	CCD1 DIS	TLim EN	Dither Amplitude			Dither Frequency			
CCD1 Frequency & Amplitude	1	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0
						Diag EN	DTHR DIS	9 BIT DAC Command Data								

Table 25. SPI Commands

Command Name	Control Address					Command Bits										
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CCD2 Control	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0
						CCD2 Retry	X	X	X	Dither Amplitude			Dither Frequency			
CCD2 Frequency & Amplitude	1	1	0	0	1	1	X	X	X	0	0	0	0	0	0	0
TLIM Query Command	1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X
TLim Query Response[27] 1=TLIM Fault on: Calibration Error, Freq. high: Calibration Error, Freq. low: VPWR Over-voltage	0	0	0	0	0 1	0 1	0 CCD1	0 OSS7	0 OSS6	0 OSS5	0 OSS4	0 OSS3	0 OSS2	0 OSS1	0 OSS0	0 1
UNUSED COMMANDS																
Invalid Command	1	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X
Invalid Command	1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X

Notes
26. 1 = VPWR Over-Voltage and 0 = Ok
27. 1 = 0 = Ok

Table 26. Serial Output (SO) Response Register

Next SO Response (Message 1) 0 = No Fault, 1 = Fault	OvrVlt, or TLim Fault	Reset	Fault Status PWM6	Fault Status PWM5	Fault Status PWM4	Fault Status PWM3	Fault Status PWM2	Fault Status PWM1	Fault Status OUT8	Fault Status OUT7	Fault Status OUT6	Fault Status OUT5	Fault Status OUT4	Fault Status OUT3	Fault Status OUT2	Fault Status OUT1
Next SO Response (Message 2) 0 = No Fault, 1 = Fault	OvrVlt, or TLim Fault	Reset	Trim Set[28]	VCAL Status int=0 ext=1	Open Fault CCD2	Short Fault CCD2	Open Fault CCD1	Short Fault CCD1	Fault Status OUT8	Fault Status OUT7	Fault Status OUT6	Fault Status OUT5	Fault Status OUT4	Fault Status OUT3	Fault Status OUT2	Fault Status OUT1

Notes
28. Trim Set bit indicates (0 = untrimmed, 1 = trimmed)

TYPICAL APPLICATIONS

INTRODUCTION

Output OFF Open Load Fault

An Output OFF Open Load Fault is the detection and reporting of an *open* load when the corresponding output is disabled (input bit programmed to a logic low state). The Output OFF Open Load Fault is detected by comparing the drain-to-source voltage of the specific MOSFET output to an internally generated reference. Each output has one dedicated comparator for this purpose.

Each output has an internal pull-down current source or resistor. The pull-down current sources are enabled on power-up and must be enabled for Open Load Detect to function. In cases were the Open Load Detect current is disabled, the status bit will always respond with logic 0. The device will only shut down the pull-down current in Sleep Mode or when disabled via the SPI.

During output switching, especially with capacitive loads, a false Output OFF Open Load Fault may be triggered. To prevent this false fault from being reported, an internal fault filter of 100µs to 450µs is incorporated. The duration for which a false fault may be reported is a function of the load impedance, $R_{DS(ON)}$, C_{OUT} of the MOSFET, as well as the supply voltage, V_{PWR}. The rising edge of $\overline{CS}$ triggers the built-in fault delay timer. The timer must time out before the fault comparator is enabled to detect a faulted threshold. Once the condition causing the Open Load Fault is removed, the device resumes normal operation. The Open Load Fault, however, will be latched in the output SO Response register for the MCU to read.

Under-voltage Shutdown

An under-voltage condition on V_{DD} results in the global shutdown of all outputs and reset of all control registers. The under-voltage threshold is between 0.8 and 2.8V.

An under-voltage condition on V_{PWR} also results in the global shutdown of all outputs and reset of all control registers. The under-voltage threshold is between 3.0 and 4.4V

Low-voltage condition ($4.4V < V_{PWR} < 9.0V$) will operate per the command word, however status reported on SO pin is not guaranteed and performance may be out of specification limits.

Output Voltage Shutdown

An over voltage condition on VDD (> 7.0) may result in permanent damage to the 33800. Over-voltage on the VPWR pin will cause the 33800 to shut down until the voltage returns to a normal value. Over voltage exceeding the maximum recommended voltage (45V) may cause permanent damage to the 33800.

Output Voltage Clamp

Each output of the 33800 incorporates an internal voltage clamp to provide fast turn-OFF and transient protection of each output. Each clamp independently limits the drain-to-source voltage to 50V. The total energy clamped (E_J) can be calculated by multiplying the current area under the current curve (I_A) times the clamp voltage (V_{CL}) (see Figure 10).

Characterization of the output clamps, using a single pulse non-repetitive method at 0.3A, indicates the maximum energy to be 50mJ at 150°C junction temperature per output.

.

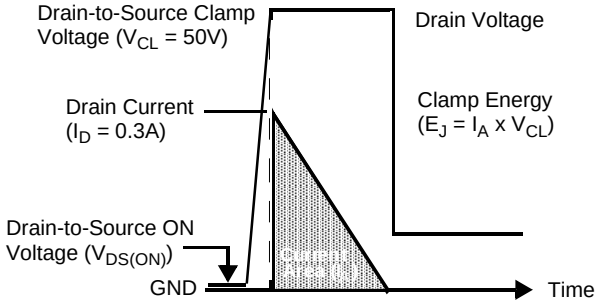


Figure 10. Output Voltage Clamping

Reverse Battery Protection

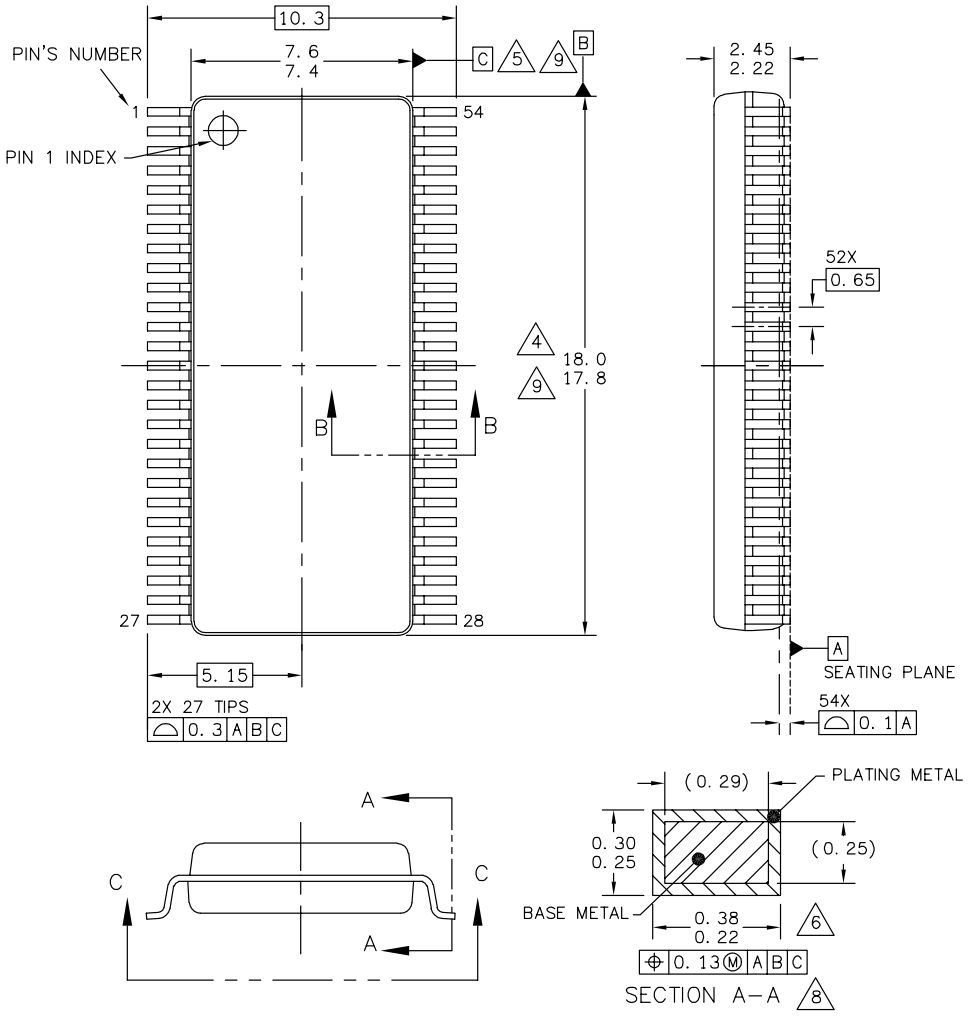
The 33800 device requires external reverse battery protection on the VPWR pin.

All outputs consist of a power MOSFET with an integral substrate diode. During reverse battery condition, current will flow through the load via the substrate diode. Under this circumstance relays may energize and lamps will turn on. If load reverse battery protection is desired, a diode must be placed in series with the load.

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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	CASE NUMBER: 1377-02	11 MAR 2005
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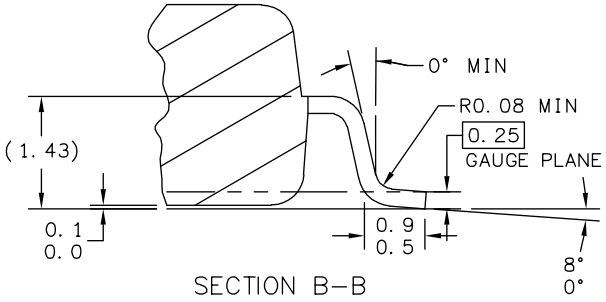

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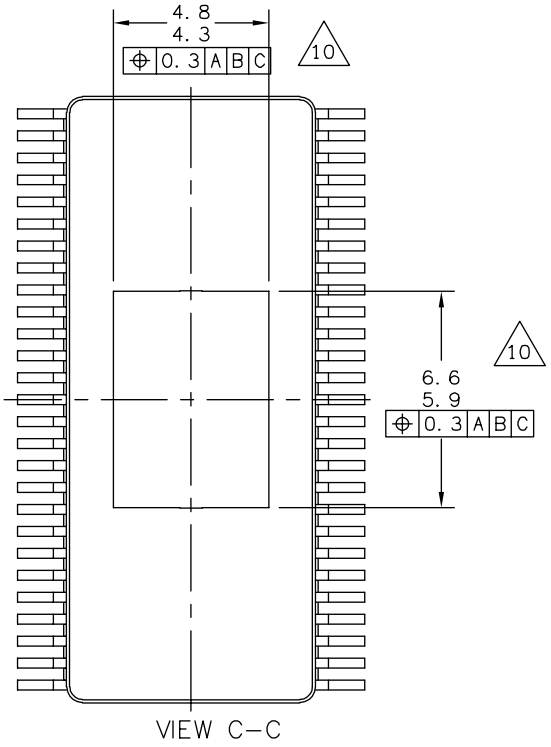

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REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	7/2006	• Initial Release
2.0	8/2006	• Updated format and style
3.0	7/2007	• Changed Part Number PC33800EK/R2 to MCZ33800EK/R2 in Ordering Information. • Changed Category from Product Preview to Advance Information.
4.0	8/2007	• Changed Octal Serial Driver, Output Refresh Timer, minimum value from “-” to 2.0ms on page 12
5.0	10/2007	• Added paragraph for PWM Frequency/Duty Cycle Command on page 23 • Revised Table 12, OSS SPI Commands and Response on page 25 • Revised Table 26, SPI Commands on page 31

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