LPC111xLV/LPC11xxLVUK

32-bit ARM Cortex-M0 MCU; up to 32 kB flash, 8 kB SRAM; 8-bit ADC

Rev. 2 — 10 October 2012 Product data sheet

1. General description

The LPC111xLV/LPC11xxLVUK is an ARM Cortex-M0-based, low-cost 32-bit MCU family, designed for 8/16-bit microcontroller applications, offering performance, low power, simple instruction set and memory addressing together with reduced code size compared to existing 8/16-bit architectures.

The LPC111xLV/LPC11xxLVUK operate at CPU frequencies of up to 50 MHz.

The peripherals of the LPC111xLV/LPC11xxLVUK include up to 32 kB of flash memory, up to 8 kB of SRAM data memory, a Fast-mode Plus I^2C-bus interface, one SSP/SPI interface, one UART, four general-purpose counter/timers, an 8-bit ADC, and up to 27 general-purpose I/O pins.

2. Features and benefits

- System:
  - ARM Cortex-M0 processor, running at frequencies of up to 50 MHz.
  - ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
  - Serial Wire Debug.
  - System tick timer.
- Memory:
  - Up to 32 kB on-chip flash programming memory with a 256 byte page erase function.
  - Up to 8 kB SRAM.
  - In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.
- Digital peripherals:
  - Up to 27 General-Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors and a configurable open-drain mode.
  - GPIO pins can be used as edge and level sensitive interrupt sources.
  - High-current output driver on one pin.
  - High-current sink drivers on two I^2C-bus pins in Fast-mode Plus.
  - Four general-purpose counter/timers with up to 7 capture inputs and 13 match outputs.
  - Programmable windowed WDT.
- Analog peripherals:

  8-bit ADC with input multiplexing among up to 8 pins.
- Serial interfaces:

- UART with fractional baud rate generation and internal FIFO.
- One SPI controller with SSP features and with FIFO and multi-protocol capabilities.
- I^2C-bus interface supporting full I^2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.

- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 2.5 % accuracy for T_{amb} = -20 °C to +85 °C and to 5 % accuracy for T_{amb} = -40 °C to -20 °C. The IRC can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
  - Clock output function with divider that can reflect the system oscillator clock, IRC clock, CPU clock, and the Watchdog clock.
- Power control:
  - Two reduced power modes: Sleep and Deep-sleep mode.
  - Ultra-low power consumption in Deep-sleep mode ($\leq$ 1.6 μA).
  - 5 μs wake-up time from Deep-sleep mode.
  - Processor wake-up from Deep-sleep mode via a dedicated start logic using up to 13 of the functional pins.
  - Power-On Reset (POR).
  - Brown-Out Detection (BOD) causing a forced reset.
- Unique device serial number for identification.
- Single power supply (1.65 V to 1.95 V)
- Available as WLCSP25, HVQFN24, and HVQFN33 package. Other package options are available for high-volume customers.

3. Applications

- Mobile phones
- Mobile accessories
- Cameras
- Tablets/Ultra books
- Active cables
- Portable medical electronics

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1101LVUK	WLCSP25	wafer level chip-size package; 25 bumps; 2.17 × 2.32 × 0.56 mm	-
LPC1102LVUK	WLCSP25	wafer level chip-size package; 25 bumps; 2.17 × 2.32 × 0.56 mm	-
LPC1112LVFHN24/003	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm	SOT616-3
LPC1114LVFHN24/103	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm	SOT616-3

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Table 1. Ordering information *…continued*

Type number	Package		
	Name	Description	Version
LPC1114LVFHN24/303	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm	SOT616-3
LPC1112LVFHI33/103	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC1114LVFHI33/303	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a

4.1 Ordering options

Table 2. Ordering options

Type number	Flash in kB	Total SRAM in kB	SPI/ SSP	I2C	UART	ADC	GPIO pins	Package
LPC1101LVUK	32	2	1	1	1	6-channel	21	WLCSP25
LPC1102LVUK	32	8	1	1	1	6-channel	21	WLCSP25
LPC1112LVFHN24/003	16	2	1	1	1	6-channel	20	HVQFN24
LPC1114LVFHN24/103	32	4	1	1	1	6-channel	20	HVQFN24
LPC1114LVFHN24/303	32	8	1	1	1	6-channel	20	HVQFN24
LPC1112LVFHI33/103	16	4	1	1	1	8-channel	27	HVQFN33
LPC1114LVFHI33/303	32	8	1	1	1	8-channel	27	HVQFN33

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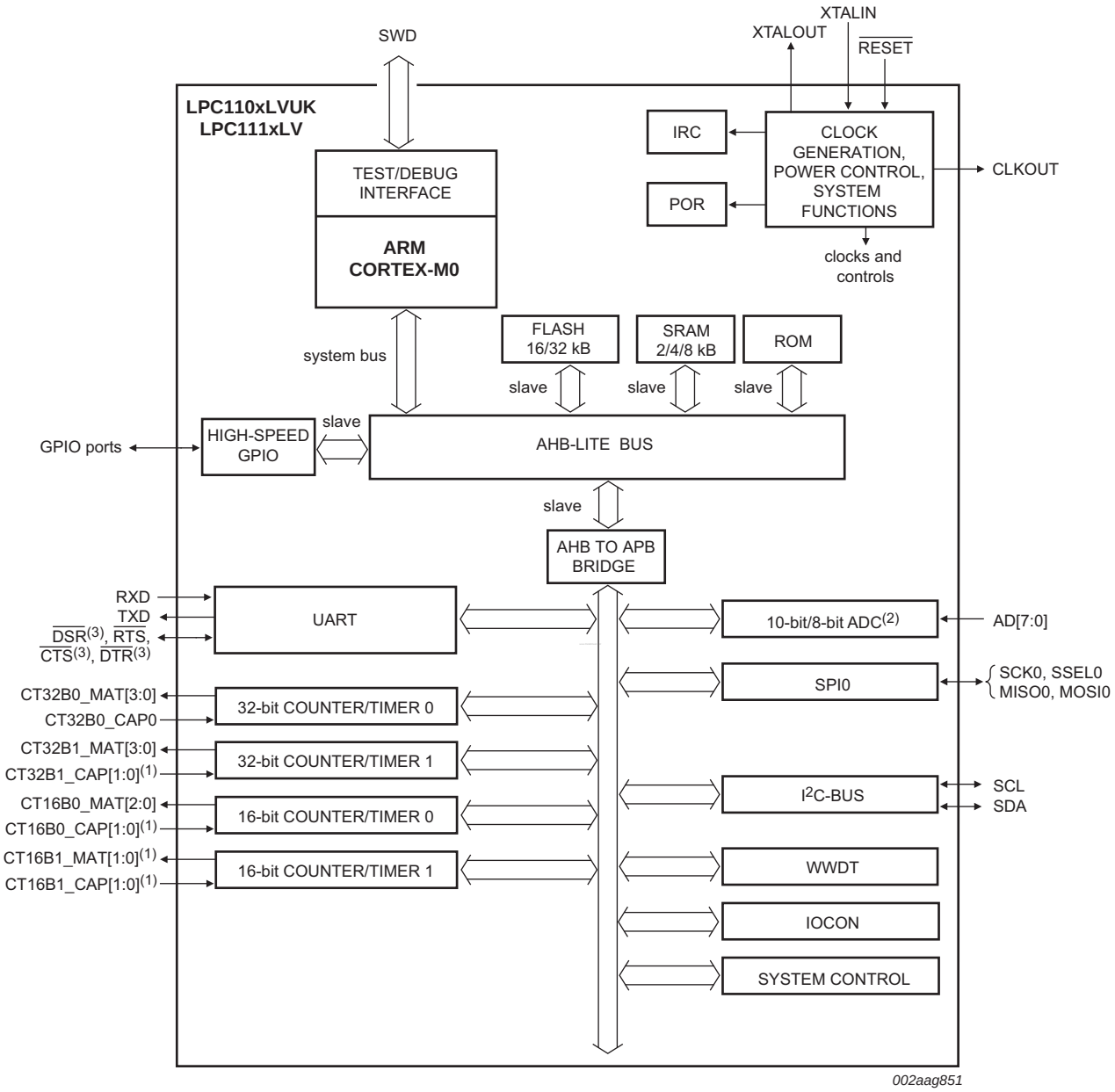
5. Block diagram



(1) CT16B1_MAT1, CT32B1_CAP1, CT1B0_CAP1, CT16B1_CAP1 available on HVQFN33 only. CT16B1_MAT0 available on HVQFN33 and WLCSP25 packages only.

(2) 6 channels on WLCSP25 and HVQFN24 packages. 8 channels on HVQFN33 packages.

(3) $\overline{\text{DSR}}$ on WLCSP25 package only. $\overline{\text{DTR}}$ on HVQFN33 package only. $\overline{\text{CTS}}$ on HVQFN24 and HVQFN33 packages only.

Fig 1. LPC111xLV/LPC11xxLVUK block diagram

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6. Pinning information

6.1 Pinning

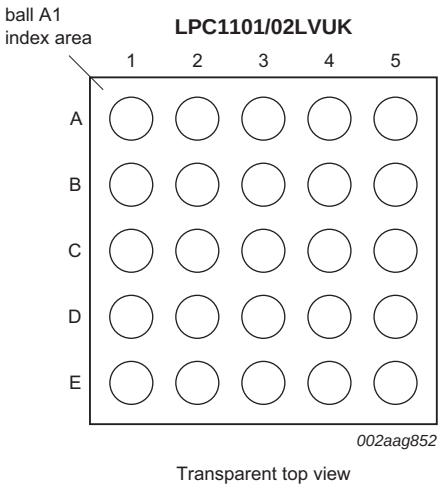

Fig 2. Pin configuration WLCSP25 package

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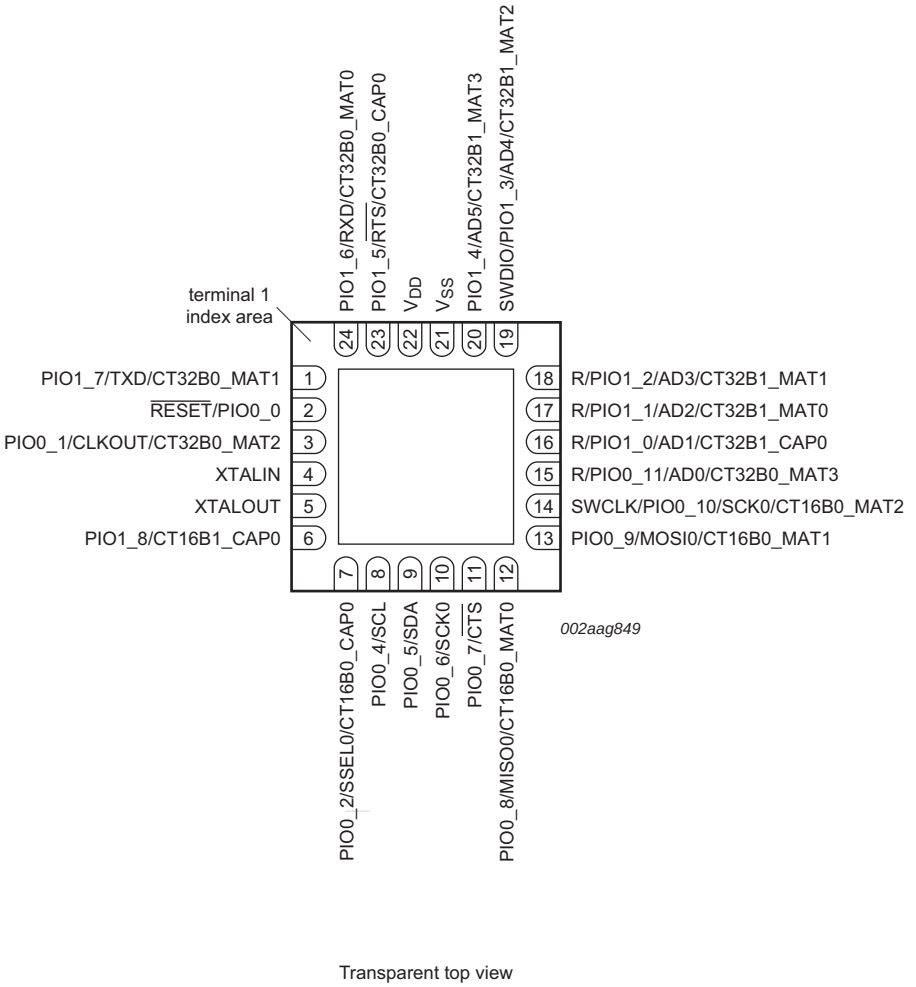

Transparent top view

For parts LPC1112LVFHN24/003, LPC1114LVFHN24/103, LPC1114LVFHN24/303.

Fig 3. Pin configuration HVQFN24 package

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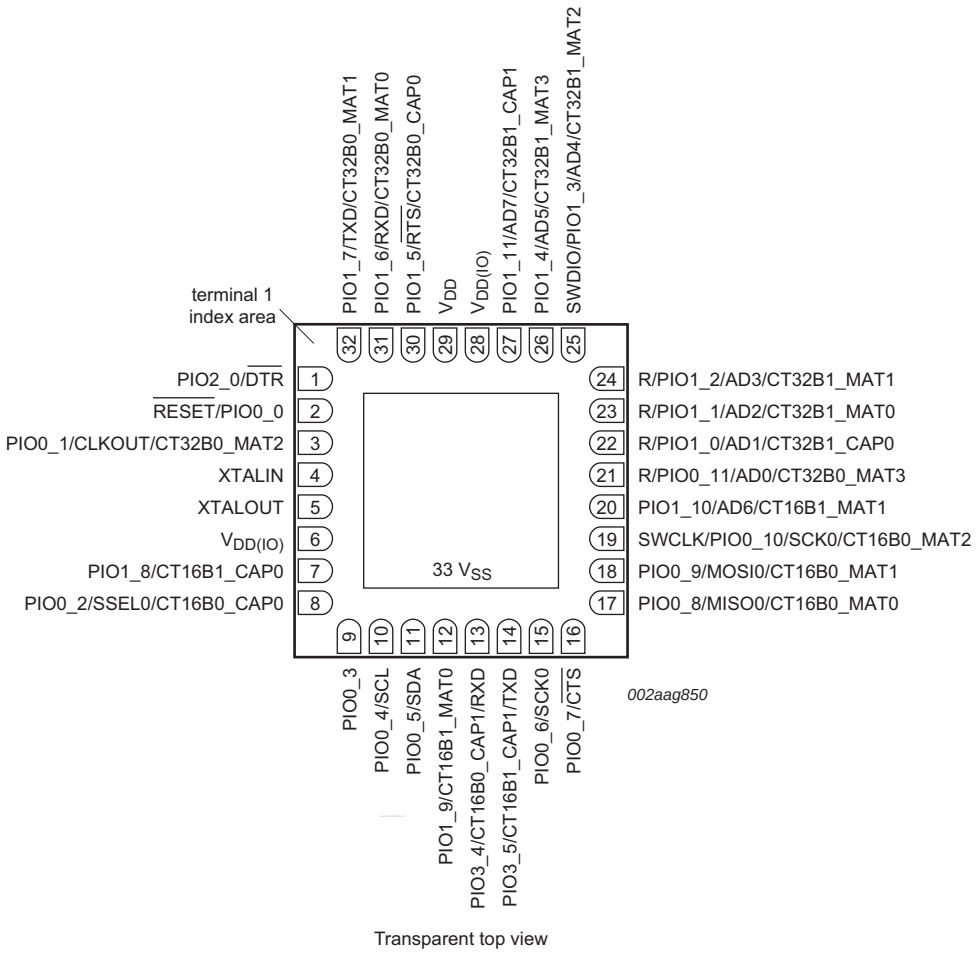

For parts LPC1112LVFHI33/103 and LPC1114LVFHI33/303.

Fig 4. Pin configuration HVQFN33 package

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6.2 Pin description

Table 3. LPC110xLVUK/LPC111xLV pin description table

Symbol	WLCSP25	HVQFN24	HVQFN33		Start logic input	Type	Reset state [1]	Description
$\overline{\text{RESET}}$/PIO0_0	D1	2	2	[2]	yes	I	I; PU	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
						I/O	-	**PIO0_0 —** General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	C3	3	3	[3]	yes	I/O	I; PU	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
						O	-	**CLKOUT —** Clockout pin.
						O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	B2	7	8	[3]	yes	I/O	I; PU	**PIO0_2 —** General purpose digital input/output pin.
						I/O	-	**SSEL0 —** Slave Select for SPI0.
						I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3	-	-	9	[3]	yes	I/O	I;PU	**PIO0_3 —** General purpose digital input/output pin.
PIO0_4/SCL	A2	8	10	[4]	yes	I/O	I; IA	**PIO0_4 —** General purpose digital input/output pin (open-drain).
						I/O	-	**SCL —** I^2C-bus, open-drain clock input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	A3	9	11	[4]	yes	I/O	I; IA	**PIO0_5 —** General purpose digital input/output pin (open-drain).
						I/O	-	**SDA —** I^2C-bus, open-drain data input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	A4	10	15	[3]	yes	I/O	I; PU	**PIO0_6 —** General purpose digital input/output pin.
						I/O	-	**SCK0 —** Serial clock for SPI0.
PIO0_7/$\overline{\text{CTS}}$	-	11	16	[3]	yes	I/O	I; PU	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
						I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	A5	12	17	[3]	yes	I/O	I; PU	**PIO0_8 —** General purpose digital input/output pin.
						I/O	-	**MISO0 —** Master In Slave Out for SPI0.
						O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	B5	13	18	[3]	yes	I/O	I; PU	**PIO0_9 —** General purpose digital input/output pin.
						I/O	-	**MOSI0 —** Master Out Slave In for SPI0.
						O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.

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Table 3. LPC110xLVUK/LPC111xLV pin description table

Symbol	WLCSP25	HVQFN24	HVQFN33		Start logic input	Type	Reset state [1]	Description
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	B4	14	19	[3]	yes	I	I; PU	**SWCLK —** Serial wire clock.
						I/O	-	**PIO0_10 —** General purpose digital input/output pin.
						I/O	-	**SCK0 —** Serial clock for SPI0.
						O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
R/PIO0_11/ AD0/CT32B0_MAT3	C5	15	21	[5]	yes	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCON block.
						I/O	-	**PIO0_11 —** General purpose digital input/output pin.
						I	-	**AD0 —** A/D converter, input 0.
						O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
R/PIO1_0/ AD1/CT32B1_CAP0	C4	16	22	[5]	yes	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCON block.
						I/O	-	**PIO1_0 —** General purpose digital input/output pin.
						I	-	**AD1 —** A/D converter, input 1.
						I	-	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	D5	17	23	[5]	no	O	I; PU	**R —** Reserved. Configure for an alternate function in the IOCON block.
						I/O	-	**PIO1_1 —** General purpose digital input/output pin.
						I	-	**AD2 —** A/D converter, input 2.
						O	-	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	D4	18	24	[5]	no	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCON block.
						I/O	-	**PIO1_2 —** General purpose digital input/output pin.
						I	-	**AD3 —** A/D converter, input 3.
						O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	E5	19	25	[5]	no	I/O	I; PU	**SWDIO —** Serial wire debug input/output.
						I/O	-	**PIO1_3 —** General purpose digital input/output pin.
						I	-	**AD4 —** A/D converter, input 4.
						O	-	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3	D3	20	26	[5]	no	I/O	I; PU	**PIO1_4 —** General purpose digital input/output pin with 10 ns glitch filter.
						I	-	**AD5 —** A/D converter, input 5.
						O	-	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
PIO1_5/$\overline{\text{RTS}}$/ CT32B0_CAP0	E2	23	30	[3]	no	I/O	I; PU	**PIO1_5 —** General purpose digital input/output pin.
						O	-	**$\overline{\text{RTS}}$ —** Request To Send output for UART.
						I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	D2	24	31	[3]	no	I/O	I; PU	**PIO1_6 —** General purpose digital input/output pin.
						I	-	**RXD —** Receiver input for UART.
						O	-	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.

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Table 3. LPC110xLVUK/LPC111xLV pin description table

Symbol	WLCSP25	HVQFN24	HVQFN33		Start logic input	Type	Reset state [1]	Description
PIO1_7/TXD/ CT32B0_MAT1	E1	1	32	[3]	no	I/O	I; PU	**PIO1_7 —** General purpose digital input/output pin.
						O	-	**TXD —** Transmitter output for UART.
						O	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_8/ CT16B1_CAP0	B1	6	7	[3]	no	I/O	I; PU	**PIO1_8 —** General purpose digital input/output pin.
						I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO1_9/ CT16B1_MAT0	B3	-	12	[3]	no	I/O	I; PU	**PIO1_9 —** General purpose digital input/output pin.
						O	-	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
PIO1_10/AD6/ CT16B1_MAT1	-	-	20	[5]	no	I/O	I;PU	**PIO1_10 —** General purpose digital input/output pin.
						I	-	**AD6 —** A/D converter, input 6.
						O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
PIO1_11/AD7/ CT32B0_MAT3	-	-	27	[5]	no	I/O	I;PU	**PIO1_11 —** General purpose digital input/output pin.
						I	-	**AD7 —** A/D converter, input 7.
						O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
PIO2_0/$\overline{\text{DTR}}$	-	-	1	[3]	no	I/O	I;PU	**PIO2_0 —** General purpose digital input/output pin.
						O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for UART.
PIO2_1/$\overline{\text{DSR}}$	A1	-	-	[3]	no	I/O	I; PU	**PIO2_1 —** General purpose digital input/output pin.
						I	-	**$\overline{\text{DSR}}$ —** Data Set Ready input for UART.
PIO3_4/ CT16B0_CAP1/RXD	-	-	13	[3]	no	I/O	I;PU	**PIO3_4 —** General purpose digital input/output pin.
						I	-	**CT16B0_CAP1 —** Capture input 1 for 16-bit timer 0.
						I	-	**RXD —** Receiver input for UART.
PIO3_5/ CT16B1_CAP1/TXD	-	-	14	[3]	no	I/O	I;PU	**PIO3_5 —** General purpose digital input/output pin.
						I	-	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
						O	-	**TXD —** Transmitter output for UART.
V_{DD}	E3	22	29; 6; 28		-	-	-	1.8 V supply voltage to the core, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	C1	4	4	[6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	C2	5	5	[6]	-	O	-	Output from the oscillator amplifier.
V_{SS}	E4	21	33		-	-	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level 0; IA = inactive, no pull-up/down enabled.

[2] See Figure 28 for the reset pad configuration.

[3] Pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 27).

[4] I^2C-bus pads compliant with the I^2C-bus specification for I^2C standard mode and I^2C Fast-mode Plus.

[5] Pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as an ADC input, digital section of the pad is disabled (see Figure 27).

[6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

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7. Functional description

7.1 ARM Cortex-M0 processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption.

7.2 On-chip flash program memory

The LPC111xLV/LPC11xxLVUK contains up to 32 kB of on-chip flash memory.

The flash memory is divided into 4 kB sectors with each sector consisting of 16 pages. Individual pages of 256 byte each can be erased using the IAP erase page command.

7.3 On-chip SRAM

The LPC111xLV/LPC11xxLVUK contains up to 8 kB on-chip static RAM memory.

7.4 Memory map

The LPC111xLV/LPC11xxLVUK incorporates several distinct memory regions, shown in the following figures. Figure 5 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 megabyte in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kilobytes of space. This allows simplifying the address decoding for each peripheral.

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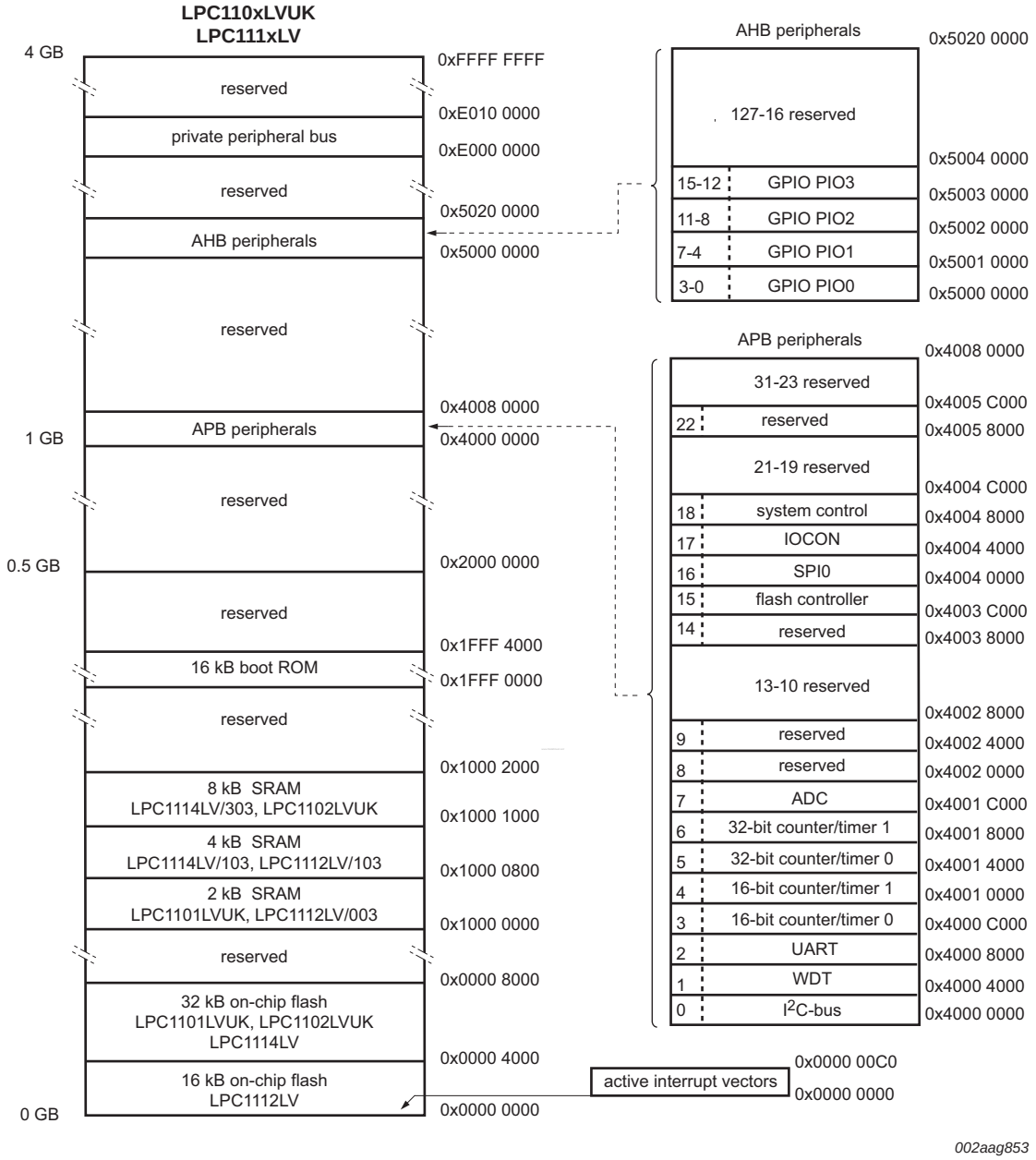

Fig 5. LPC111xLV/LPC11xxLVUK memory map

7.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.

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- In the LPC111xLV/LPC11xxLVUK, the NVIC supports 32 vectored interrupts including up to 13 inputs to the start logic from individual GPIO pins.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any GPIO pin (total of up to 18 pins) regardless of the selected function, can be programmed to generate an interrupt on a level, or rising edge or falling edge, or both.

7.6 IOCON block

The IOCON block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

7.7 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC111xLV/LPC11xxLVUK use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Additionally, any GPIO pin (total of up to 18 pins) providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

7.7.1 Features

- Bit level port registers allow a single instruction to set or clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with pull-ups enabled after reset with the exception of the I^2C-bus pins PIO0_4 and PIO0_5.
- Pull-up/pull-down resistor configuration can be programmed through the IOCON block for each GPIO pin (except for pins PIO0_4 and PIO0_5).
- All GPIO pins (except PIO0_4 and PIO0_5) are pulled up to 1.8 V (V_{DD} = 1.8 V) if their pull-up resistor is enabled in the IOCON block (single power supply).
- Programmable open-drain mode.

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7.8 UART

The LPC111xLV/LPC11xxLVUK contains one UART.

Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The UART includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.8.1 Features

- Maximum UART data bit rate of 3.125 MBit/s.
- 16 Byte Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.

7.9 SPI serial I/O controller

The LPC111xLV/LPC11xxLVUK contains one SPI controller.

The SPI controller is capable of operation on an SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SPI supports full-duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.9.1 Features

- Maximum SPI speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.10 I^2C-bus serial I/O controller

The LPC111xLV/LPC11xxLVUK contains one I^2C-bus controller.

The I^2C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock Line (SCL) and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the

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capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.10.1 Features

- The I^2C-interface is a standard I^2C-bus compliant interface with open-drain pins. The I^2C-bus interface also supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.
- The I^2C-bus controller supports multiple address recognition and a bus monitor mode.

7.11 ADC

The LPC111xLV/LPC11xxLVUK contains one ADC. It is a single 8-bit successive approximation ADC with up to eight channels.

Remark: ADC specifications are valid for T_{amb} = -40 °C to +85 °C on HVQFN33 and WLCSP25 packages. ADC specifications are valid for T_{amb} = -10 °C to 85 °C on the HVQFN24 package.

7.11.1 Features

- 8-bit successive approximation ADC.
- Input multiplexing among 6 pins (WLCSP25 and HVQFN24 packages).
- Input multiplexing among 8 pins (HVQFN33 packages).
- Power-down mode.
- Measurement range 0 V to V_{DD}.
- 8-bit sampling rate of up to 10 kSamples/s.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or timer match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

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7.12 General purpose external event counter/timers

The LPC111xLV/LPC11xxLVUK includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.12.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- Up to two capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

7.13 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.14 Windowed WatchDog Timer

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.14.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.

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- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the IRC or the dedicated watchdog oscillator (WDO). This gives a wide range of potential timing choices of watchdog operation under different power conditions.

7.15 Clocking and power control

7.15.1 Crystal oscillators

The LPC111xLV/LPC11xxLVUK include three independent oscillators. These are the system oscillator, the Internal RC oscillator (IRC), and the Watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC111xLV/LPC11xxLVUK will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 6 for an overview of the LPC111xLV/LPC11xxLVUK clock generation.

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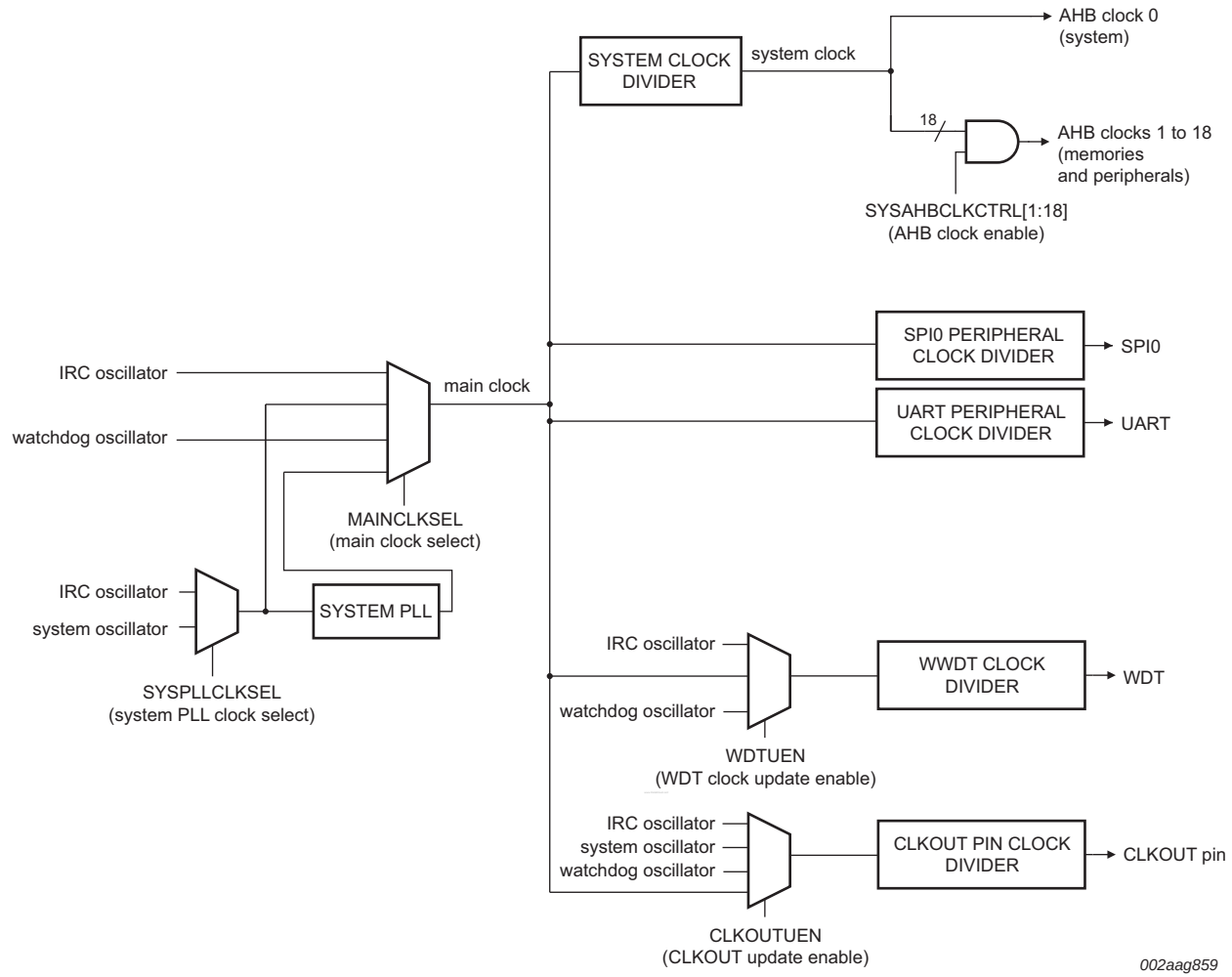

Fig 6. LPC111xLV/LPC11xxLVUK clock generation block diagram

7.15.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 2.5 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC111xLV/LPC11xxLVUK use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.15.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

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7.15.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over processing and temperature is ±40 %.

7.15.2 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The PLL output frequency must be lower than 100 MHz. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.15.3 Clock output

The LPC111xLV/LPC11xxLVUK features a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

7.15.4 Wake-up process

The LPC111xLV/LPC11xxLVUK begin operation at power-up by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the system oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

7.15.5 Power control

The LPC111xLV/LPC11xxLVUK support a variety of power control features. There are two special modes of processor power reduction: Sleep mode, and Deep-sleep mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing fine-tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.15.5.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

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7.15.5.2 Deep-sleep mode

In Deep-sleep mode, the chip is in Sleep mode, and in addition all analog blocks are shut down. As an exception, the user has the option to keep the IRC, the BOD, and the watchdog timer/watchdog oscillator running for self-timed wake-up. Deep-sleep mode allows for additional power savings.

Up to 13 pins can serve as external wake-up pins to the start logic to wake up the chip from Deep-sleep mode.

Unless the watchdog oscillator or the IRC are selected to run in Deep-sleep mode, the clock source should be switched to IRC before entering Deep-sleep mode, because the IRC can be switched on and off glitch-free.

7.16 System control

7.16.1 Start logic

The start logic connects external pins to corresponding interrupts in the NVIC. Each pin shown in Table 3 as input to the start logic is connected to an individual interrupt in the NVIC interrupt vector table. The start logic pins can serve as external interrupt pins when the chip is in Active mode. In addition, an input signal on the start logic pins can wake up the chip from Deep-sleep mode when all clocks are shut down.

The start logic must be configured in the system configuration block and in the NVIC before being used.

7.16.2 Reset

Reset has four sources on the LPC111xLV/LPC11xxLVUK: the $\overline{\text{RESET}}$ pin, the Watchdog reset, the BrownOut Detection (BOD) circuit, and Power-On Reset (POR). The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

7.16.3 BrownOut Detection (BOD)

The LPC111xLV/LPC11xxLVUK includes a BOD circuit which monitors the voltage level on the V_{DD} pin. If this voltage falls below a fixed level (see Table 8), the BOD asserts a chip reset.

7.16.4 Code security (Code Read Protection - CRP)

This feature of the LPC111xLV/LPC11xxLVUK allows user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details see the *LPC111xLV user manual*.

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There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via the UART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled (NO_ISP mode). For details see the *LPC111xLV user manual*.

7.16.5 APB interface

The APB peripherals are located on one APB bus.

7.16.6 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the Boot ROM.

7.16.7 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs. In addition, start logic inputs serve as external interrupts (see Section 7.16.1).

7.17 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0. Serial wire debug with four breakpoints and two watchpoints is supported.

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8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)			1.65	1.95	V
V_I	input voltage	only valid when the V_{DD} supply voltage is present 1.65 V ≤ V_{DD} < 1.8 V	[2]	−0.5	+3.0	V
		V_{DD} ≥ 1.8 V		−0.5	+5.0	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	−(0.5V_{DD}) < V_I < (1.5V_{DD}); T_j < 125 °C		-	100	mA
T_{stg}	storage temperature	non-operating	[3]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[4]	−6500	+6500	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Refer to the JEDEC spec (J-STD-033B.1) for further details.

[4] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

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9. Static characteristics

9.1 Static characteristics

Table 5. Static characteristics (single power supply

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)			1.65	1.8	1.95	V
Power consumption							
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash					
		system clock = 12 MHz; V_{DD} = 1.8 V	[2][3][4][5]	-	2	-	mA
		system clock = 50 MHz; V_{DD} = 1.8 V	[2][3][5][6]	-	8	-	mA
		Sleep mode; system clock = 12 MHz; V_{DD} = 1.8 V	[2][3][4][5]	-	0.8	-	mA
		Deep-sleep mode; V_{DD} = 1.8 V	[2][3][7]	-	1.6	-	µA
Standard port pins, RESET							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function;	[8][9]				
		V_{DD} = 1.8 V		0	-	3.0	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	1.65 V ≤ V_{DD} ≤ 1.95 V; I_{OH} = 3 mA		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	1.65 V ≤ V_{DD} ≤ 1.95 V; I_{OL} = 3 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 1.65 V ≤ V_{DD} ≤ 1.95 V		3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; 1.65 V ≤ V_{DD} ≤ 1.95 V		3	-	-	mA

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Table 5. Static characteristics (single power supply *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[10]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[10]	-	-	50	mA
I_{pd}	pull-down current	V_I = 1.8 V (V_{DD} = 1.8 V)		10	29	90	µA
I_{pu}	pull-up current	V_I = 0 V; 1.65 V ≤ V_{DD} ≤ 1.95 V		−3	−13	−85	µA
		V_{DD} < V_I < 3.0 V		0	0	0	µA
High-drive output pin (PIO0_7)							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function; V_{DD} = 1.8 V	[8][9]	0	-	3.0	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	1.65 V ≤ V_{DD} ≤ 1.95 V; I_{OH} = 10 mA		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	1.65 V ≤ V_{DD} ≤ 1.95 V; I_{OL} = 3 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 1.65 V ≤ V_{DD} ≤ 1.95 V		10	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 1.65 V ≤ V_{DD} ≤ 1.95 V		3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[10]	-	-	50	mA
I_{pd}	pull-down current	V_I = 1.8 V		10	29	90	µA
I_{pu}	pull-up current	V_I = 0 V; 1.65 V ≤ V_{DD} ≤ 1.95 V		−3	−13	−85	µA
		V_{DD} < V_I < 3.0 V		0	0	0	µA

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Table 5. Static characteristics (single power supply *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I²C-bus pins (PIO0_4 and PIO0_5)							
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	$0.05V_{DD}$	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I²C-bus pins configured as standard mode pins 1.65 V ≤ V_{DD} ≤ 1.95 V		2.5	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I²C-bus pins configured as Fast-mode Plus pins 1.65 V ≤ V_{DD} ≤ 1.95 V;		15	-	-	mA
I_{LI}	input leakage current	$V_I = V_{DD}$	[11]	-	2	4	µA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	1.8	1.95	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] T_{amb} = 25 °C.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled. BOD disabled for all measurements.

[4] IRC enabled; system oscillator disabled; system PLL disabled.

[5] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to UART and SPI0 disabled in system configuration block.

[6] IRC disabled; system oscillator enabled; system PLL enabled.

[7] All oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0x0000 18FF.

[8] Including voltage on outputs in 3-state mode.

[9] V_{DD} supply voltage must be present.

[10] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[11] To V_{SS}.

9.1.1 Analog characteristics

Remark: ADC specifications are valid for T_{amb} = -40 °C to +85 °C on HVQFN33 and WLCSP25 packages. ADC specifications are valid for T_{amb} = -10 °C to +85 °C on the HVQFN24 package.

Table 6. 8-bit ADC static characteristics
T_{amb} = −40 °C to +85 °C for HVQFN33 and WLCSP25 packages. T_{amb} = −10 °C to +85 °C for the HVQFN24 package. V_{DD} = 1.8 V ± 5 %; 8-bit resolution.

Symbol	Parameter		Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DD}	V
C_{ia}	analog input capacitance		-	-	1	pF
DNL	differential non-linearity	[1][2]	-	-	± 1	LSB
INL	integral non-linearity	[3]	-	-	± 1.5	LSB
E_O	offset error	[4]	-	-	± 1	LSB

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Table 6. 8-bit ADC static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for HVQFN33 and WLCSP25 packages. T_{amb} = −10 °C to +85 °C for the HVQFN24 package. V_{DD} = 1.8 V ± 5 %; 8-bit resolution.

Symbol	Parameter		Min	Typ	Max	Unit
E_G	gain error	[5]	-	-	± 2	LSB
$f_{clk(ADC)}$	ADC clock frequency		-	-	110	kHz
f_s	sampling rate		-	-	10	kSamples/s
R_{vsi}	voltage source interface resistance		-	-	40	kΩ
R_i	input resistance	[6][7]	-	-	2.5	MΩ

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 7.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 7.

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 7.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 7.

[6] T_{amb} = 25 °C; maximum sampling frequency f_s = 10 kSamples/s and analog input capacitance C_{ia} = 1 pF.

[7] Input resistance R_i depends on the sampling frequency fs: $R_i = 1 / (f_s \times C_{ia})$.

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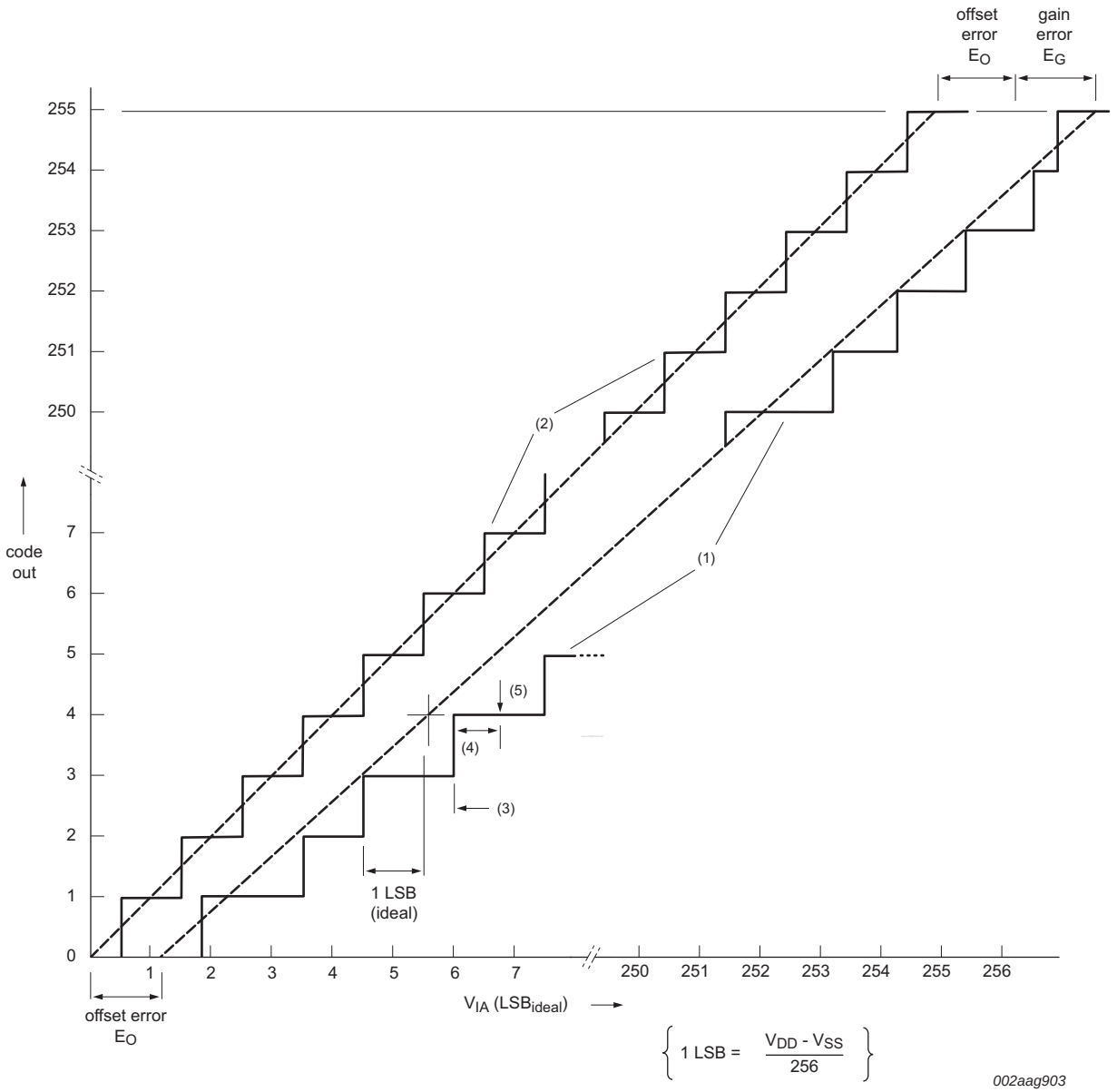

(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 7. ADC characteristics

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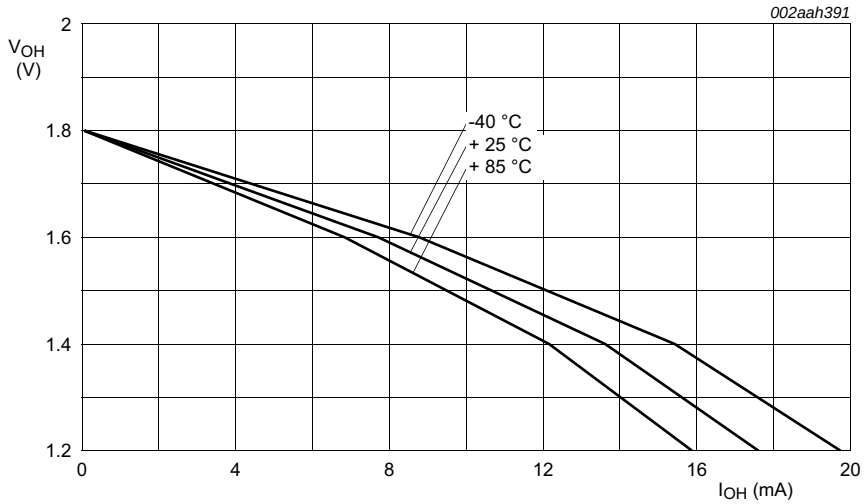
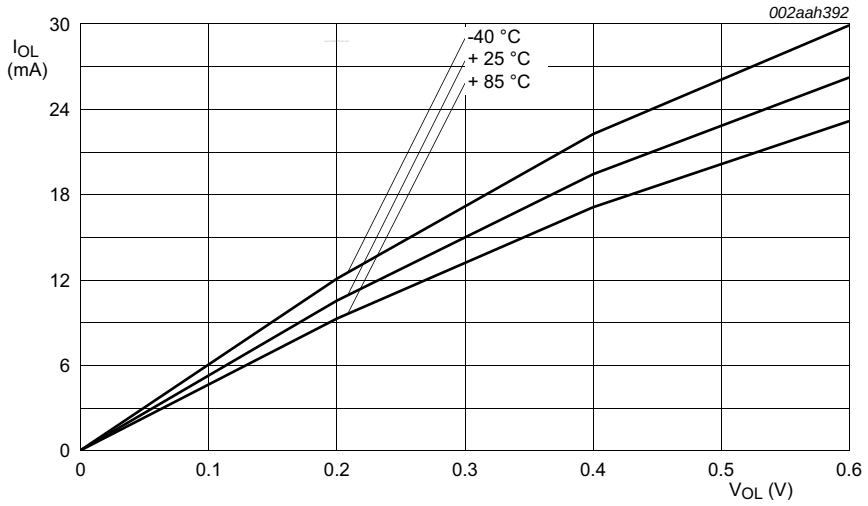
9.2 Electrical pin characteristics



Conditions: high-drive pin PIO0_7; V_{DD} = 1.8 V.

Fig 8. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}.



Conditions: I^2C-bus pins PIO0_4 and PIO0_5; V_{DD} = 1.8 V; configured for Fast mode plus in the IOCON PIO0_4 and PIO0_5 registers.

Fig 9. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

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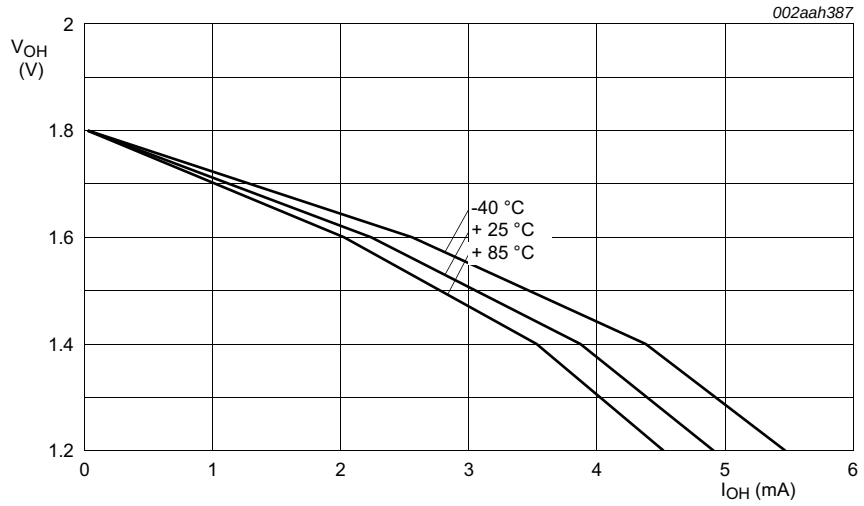
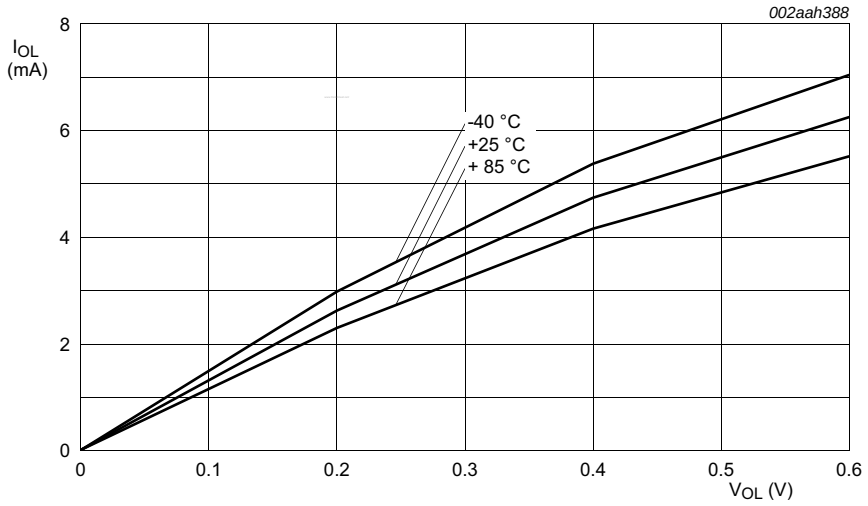


Conditions: standard port pins; V_{DD} = 1.8 V.

Fig 10. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: standard port pins; V_{DD} = 1.8 V.

Fig 11. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

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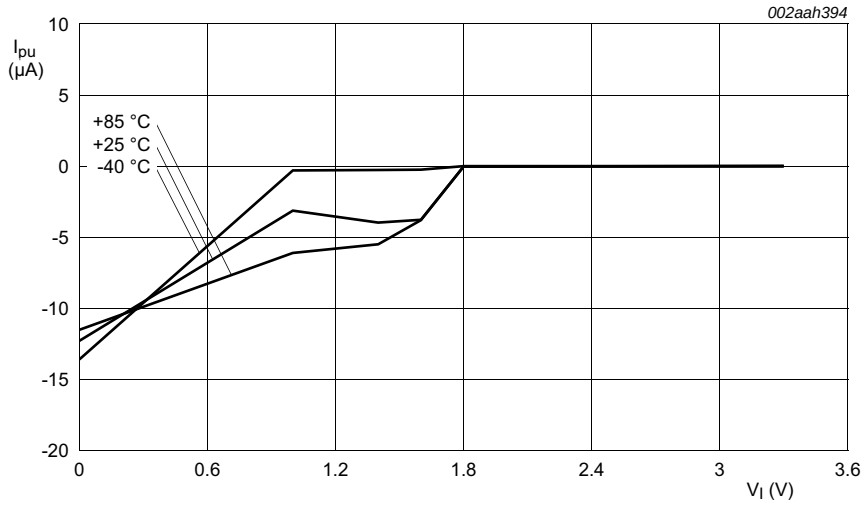
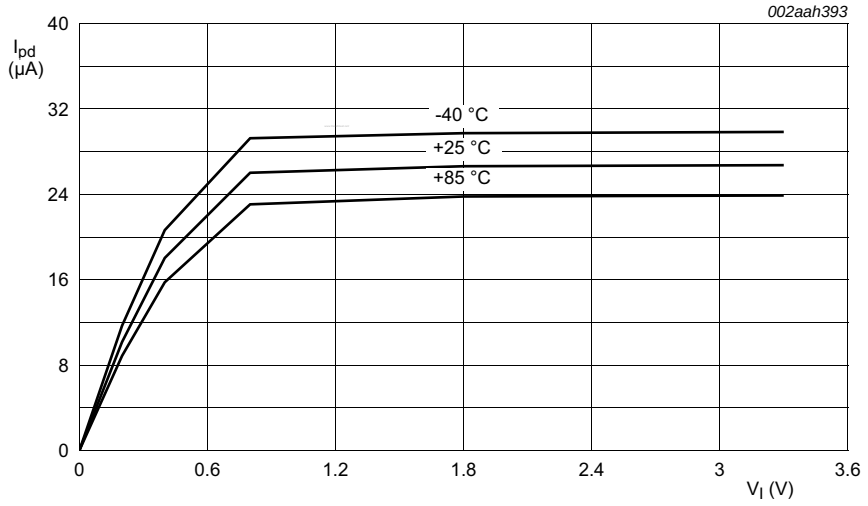


Conditions: standard port pins; V_{DD} = 1.8 V.

Fig 12. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: standard port pins; V_{DD} = 1.8 V.

Fig 13. Typical pull-down current I_{pd} versus input voltage V_I

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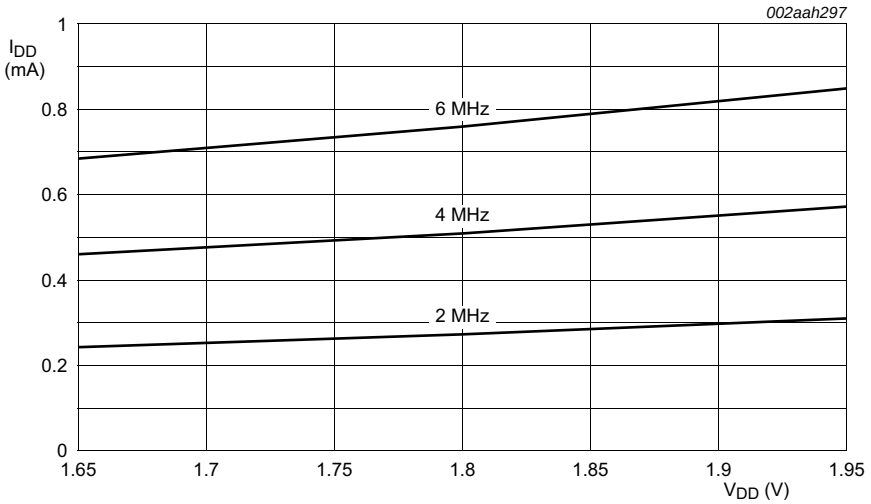
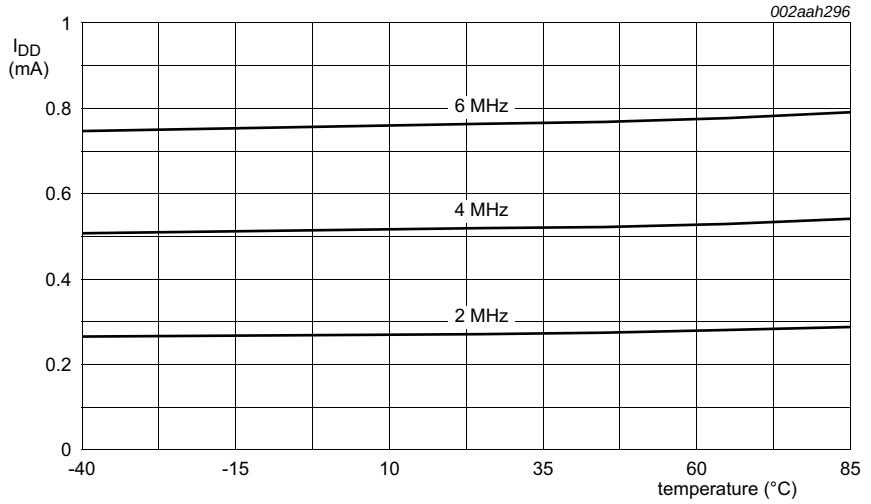
9.3 Power consumption



Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; System oscillator, system PLL, IRC, BOD disabled; system clock provided by external clock.

Fig 14. Active mode (2 MHz to 6 MHz): Typical supply current I_{DD} versus supply voltage V_{DD} for different clock frequencies



Conditions: V_{DD} = 1.8 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; System oscillator, system PLL, IRC, BOD disabled; system clock provided by external clock.

Fig 15. Active mode (2 MHz to 6 MHz): Typical supply current I_{DD} versus temperature for different clock frequencies

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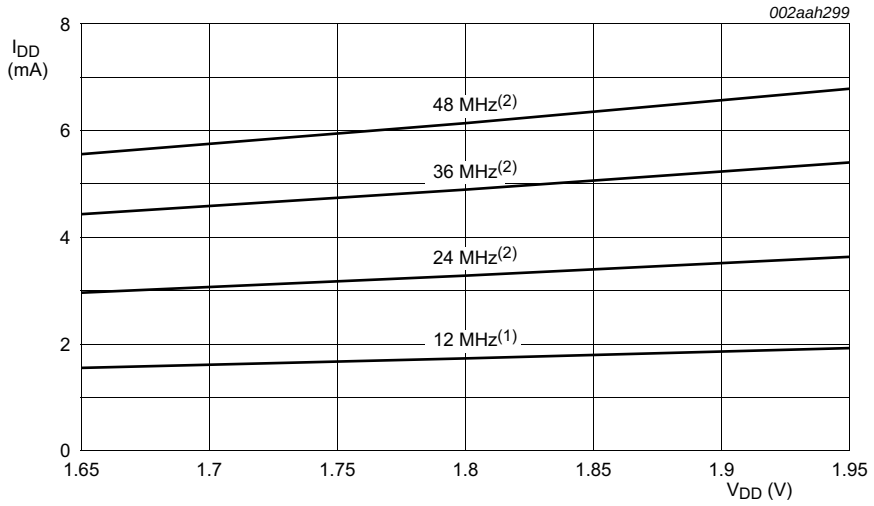
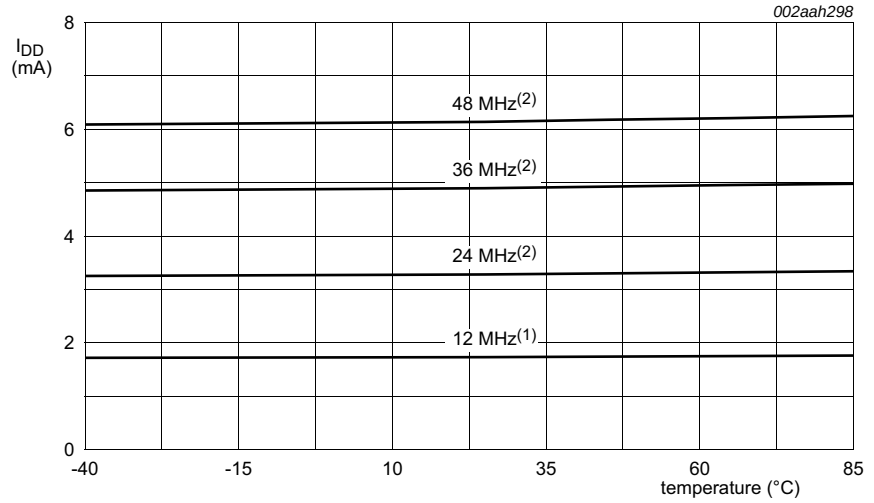


Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 16. Active mode: Typical supply current I_{DD} versus supply voltage for different system clock frequencies



Conditions: V_{DD} = 1.8 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 17. Active mode: Typical supply current I_{DD} versus temperature for different system clock frequencies

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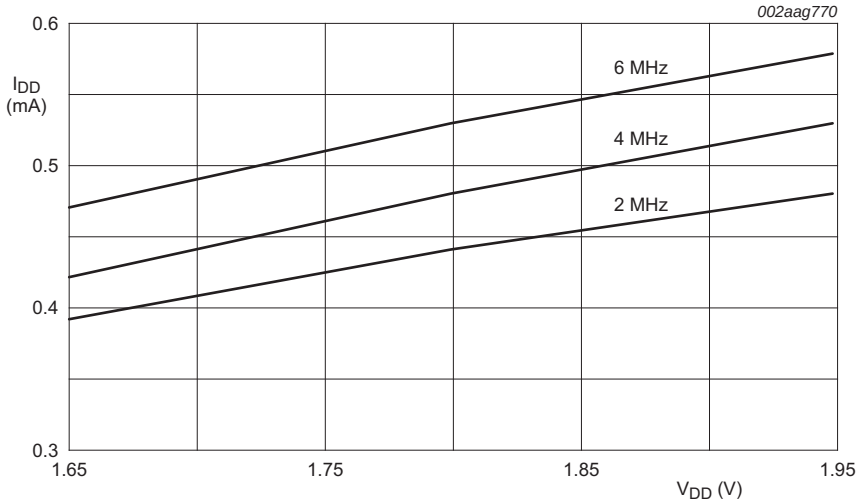
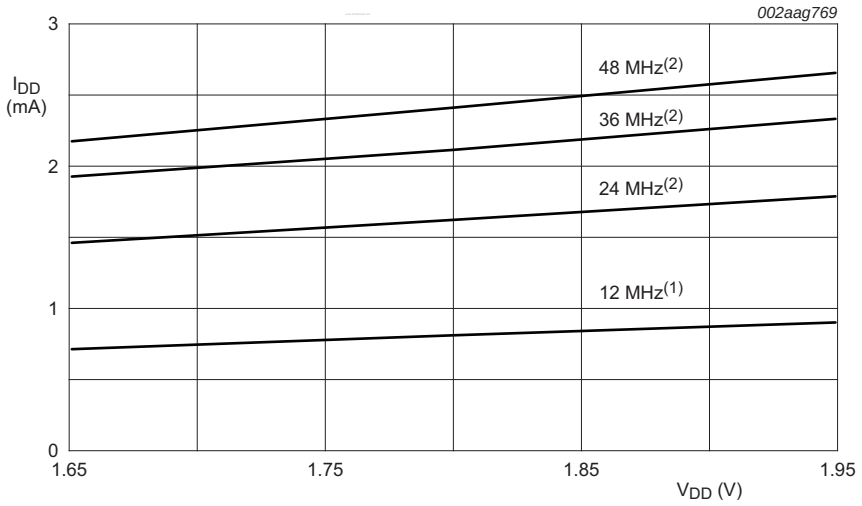


Conditions: T_{amb} = 25 °C; Sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; System oscillator and system PLL disabled; IRC disabled; system clock provided by external clock.

Fig 18. Sleep mode (2 MHz to 6 MHz): Typical supply current I_{DD} versus supply voltage V_{DD} for different clock frequencies



Conditions: T_{amb} = 25 °C; Sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 19. Sleep mode (12 MHz to 48 MHz): Typical supply current I_{DD} versus supply voltage V_{DD} for different clock frequencies

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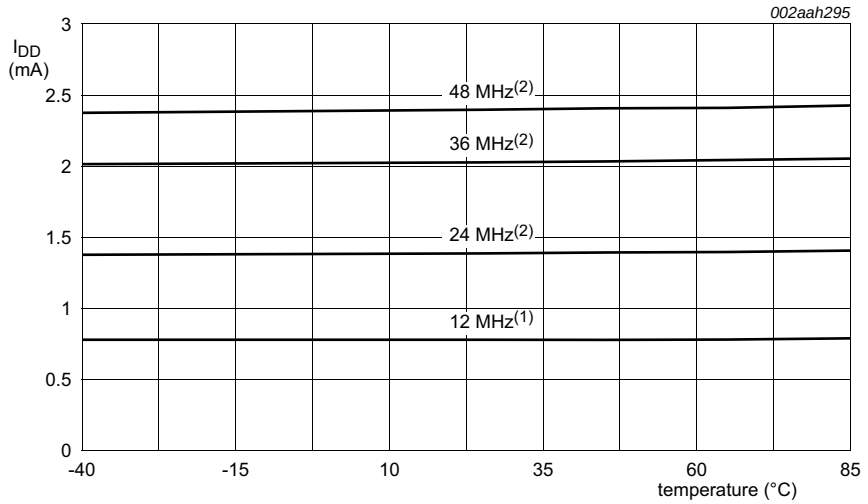
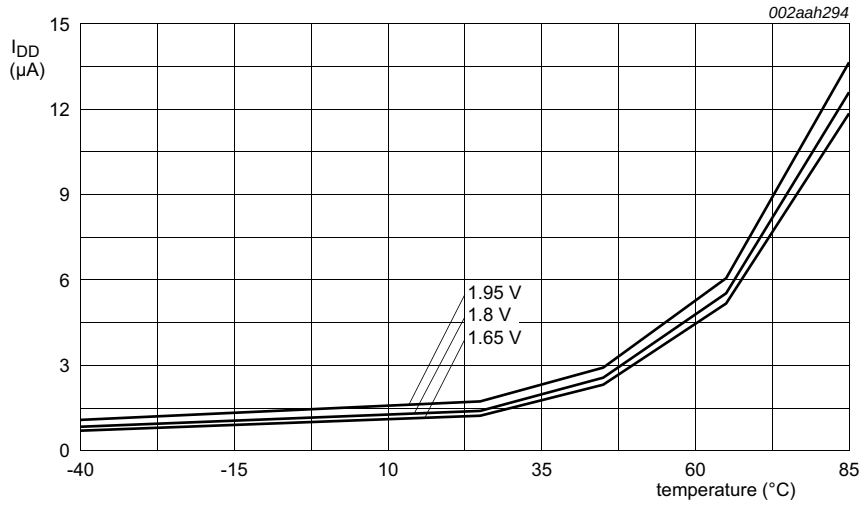


Conditions: T_{amb} = 25 °C; V_{DD} = 1.8 V; Sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 20. Sleep mode (12 MHz to 48 MHz): Typical supply current I_{DD} versus temperature for different clock frequencies



Conditions: all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 21. Deep-sleep mode: Typical supply current I_{DD} versus temperature

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9.4 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

Table 7. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
IRC	0.26	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.18	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	0.004	-	-	System oscillator running; PLL off; independent of main clock frequency.
Main PLL	-	0.061	-	
ADC	-	0.08	0.29	
CLKOUT	-	0.18	0.45	Main clock divided by 4 in the CLKOUTDIV register.
CT16B0	-	0.02	0.06	
CT16B1	-	0.02	0.06	
CT32B0	-	0.02	0.07	
CT32B1	-	0.02	0.06	
GPIO	-	0.23	0.88	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCON	-	0.03	0.10	
I2C	-	0.04	0.13	
ROM	-	0.04	0.15	
SPI0	-	0.12	0.45	
UART	-	0.22	0.82	
WWDT	-	0.02	0.06	Main clock selected as clock source for the WWDT.

9.5 BOD static characteristics

Table 8. BOD static characteristics

T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	reset level 0				
		assertion	-	1.46	-	V
		de-assertion	-	1.63	-	V

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10. Dynamic characteristics

10.1 Flash memory

Table 9. Flash characteristics

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

10.2 External clock

Table 10. Dynamic characteristic: external clock

T_{amb} = –40 °C to +85 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

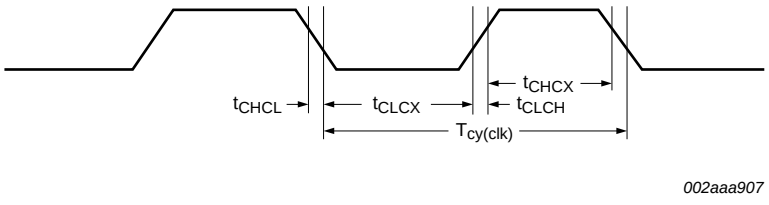

Fig 22. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

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10.3 Internal oscillators

Table 11. Dynamic characteristic: internal oscillators
V_{DD} = 1.65V to 1.95 V.

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	*-20 °C ≤ T_{amb} ≤ +85 °C*	12 - 2.5 %	12	12 + 2.5 %	MHz
		-40 °C ≤ T_{amb} < -20 °C	12 - 5 %	12	12 + 5 %	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

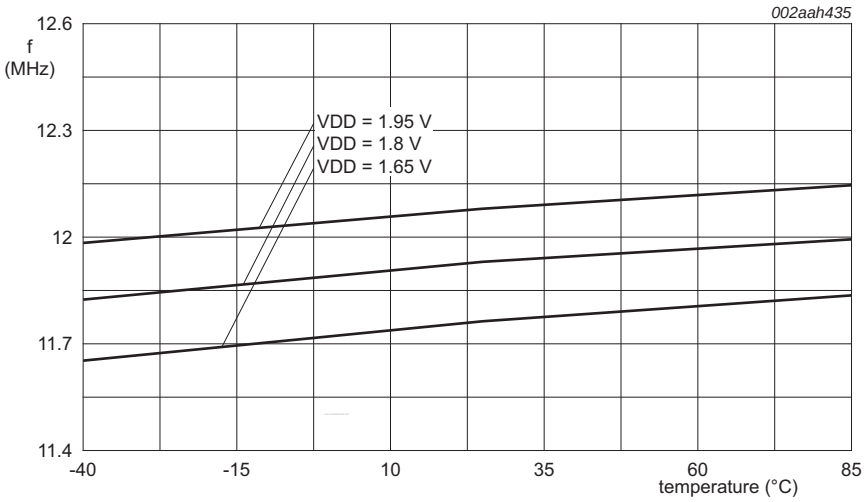

Fig 23. Typical internal RC oscillator frequency for different supply voltages V_{DD}

Table 12. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +85 °C) is ±40 %.

[3] See the *LPC111xLV user manual*.

10.4 I²C-bus

Table 13. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency	Standard-mode	0	100	kHz
		Fast-mode	0	400	kHz
		Fast-mode Plus	0	1	MHz

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Table 13. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals	-	300	ns
			Standard-mode			
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)}$ + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

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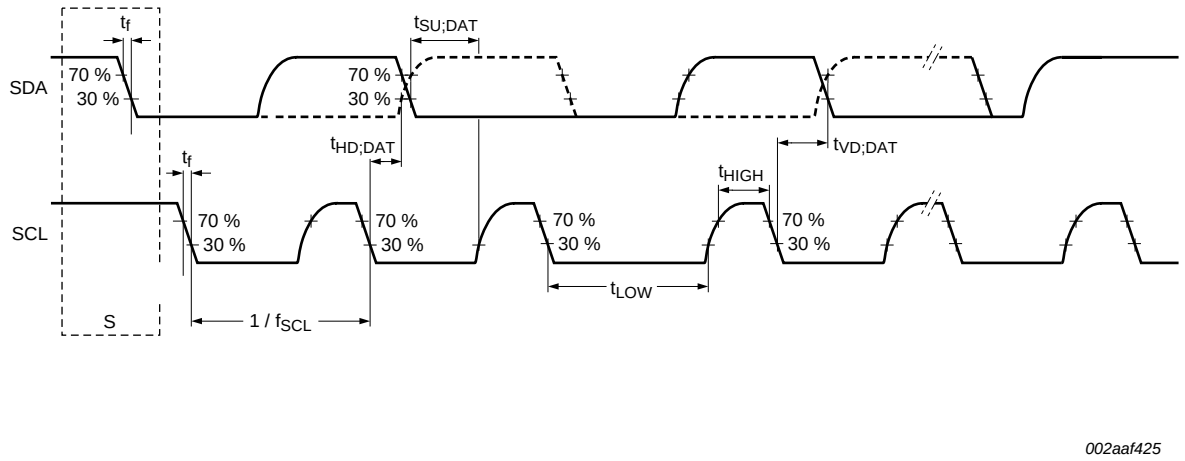

Fig 24. I²C-bus pins clock timing

10.5 SPI interface

Table 14. Dynamic characteristics of SPI pins in SPI mode

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI master (in SPI mode)							
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	50	-	-	ns
		when only transmitting	[1]	40	-	-	ns
t_{DS}	data set-up time	in SPI mode 1.8 V < V_{DD} < 1.95 V	[2]	24	-	-	ns
t_{DH}	data hold time	in SPI mode	[2]	0	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2]	0	-	-	ns

[1] $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

[2] T_{amb} = −40 °C to 85 °C.

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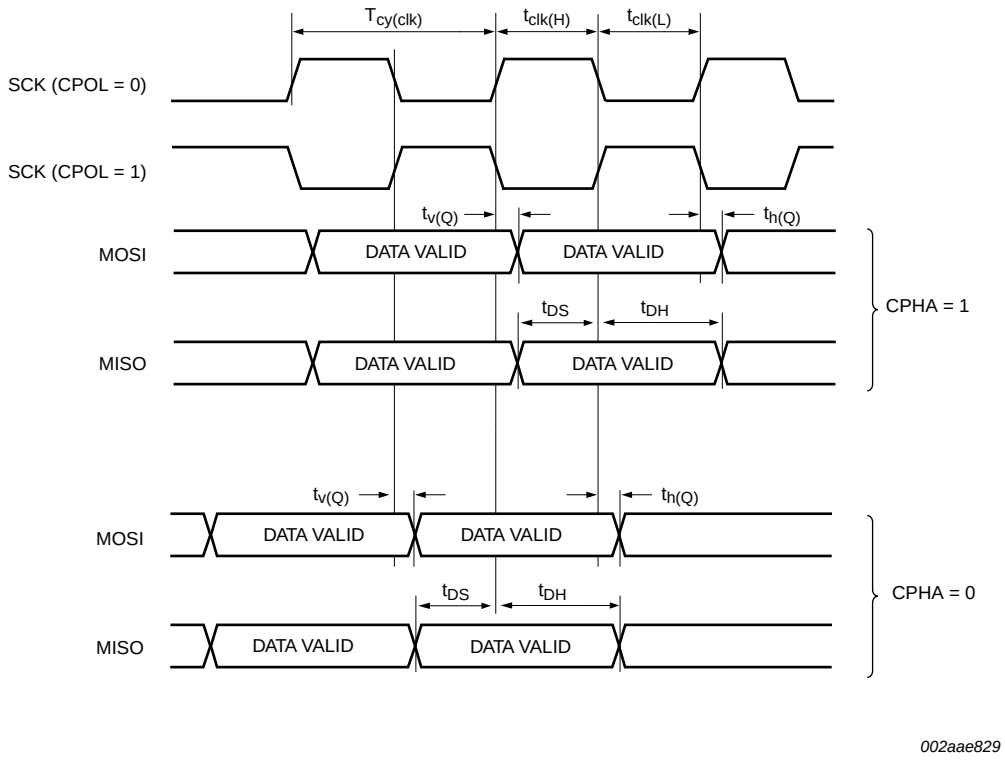

Fig 25. SPI master timing in SPI mode

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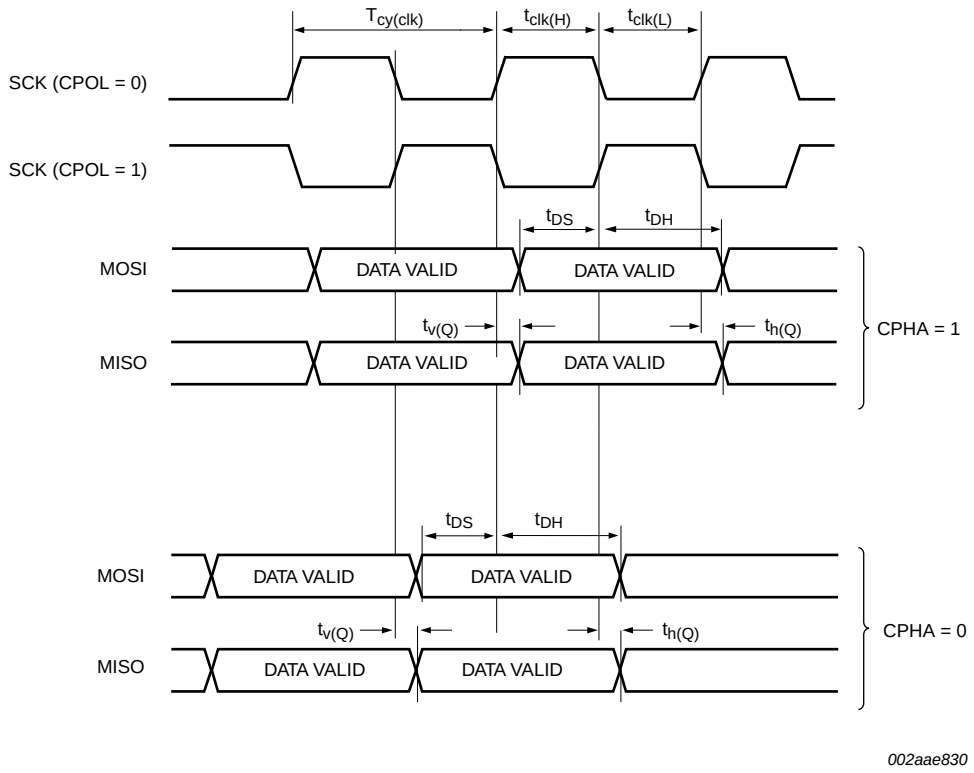

Fig 26. SPI slave timing in SPI mode

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11. Application information

11.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 6:

- The ADC input trace must be short and as close as possible to the LPC111xLV/LPC11xxLVUK chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

11.2 Standard I/O pad configuration

Figure 27 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Analog input

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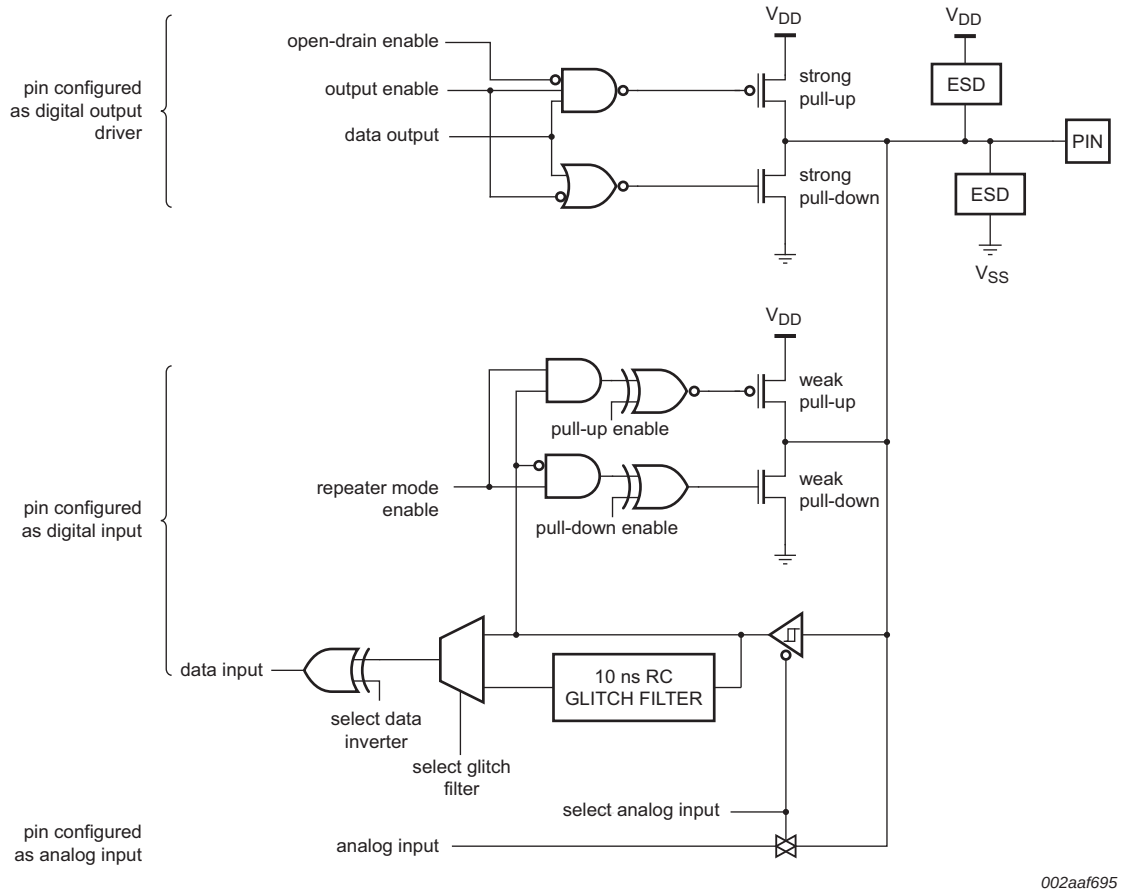

Fig 27. Standard I/O pad configuration

11.3 Reset pad configuration

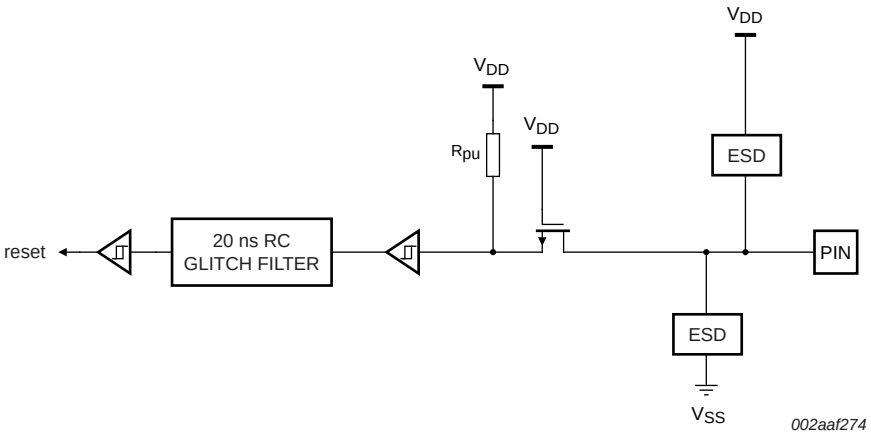

Fig 28. Reset pad configuration

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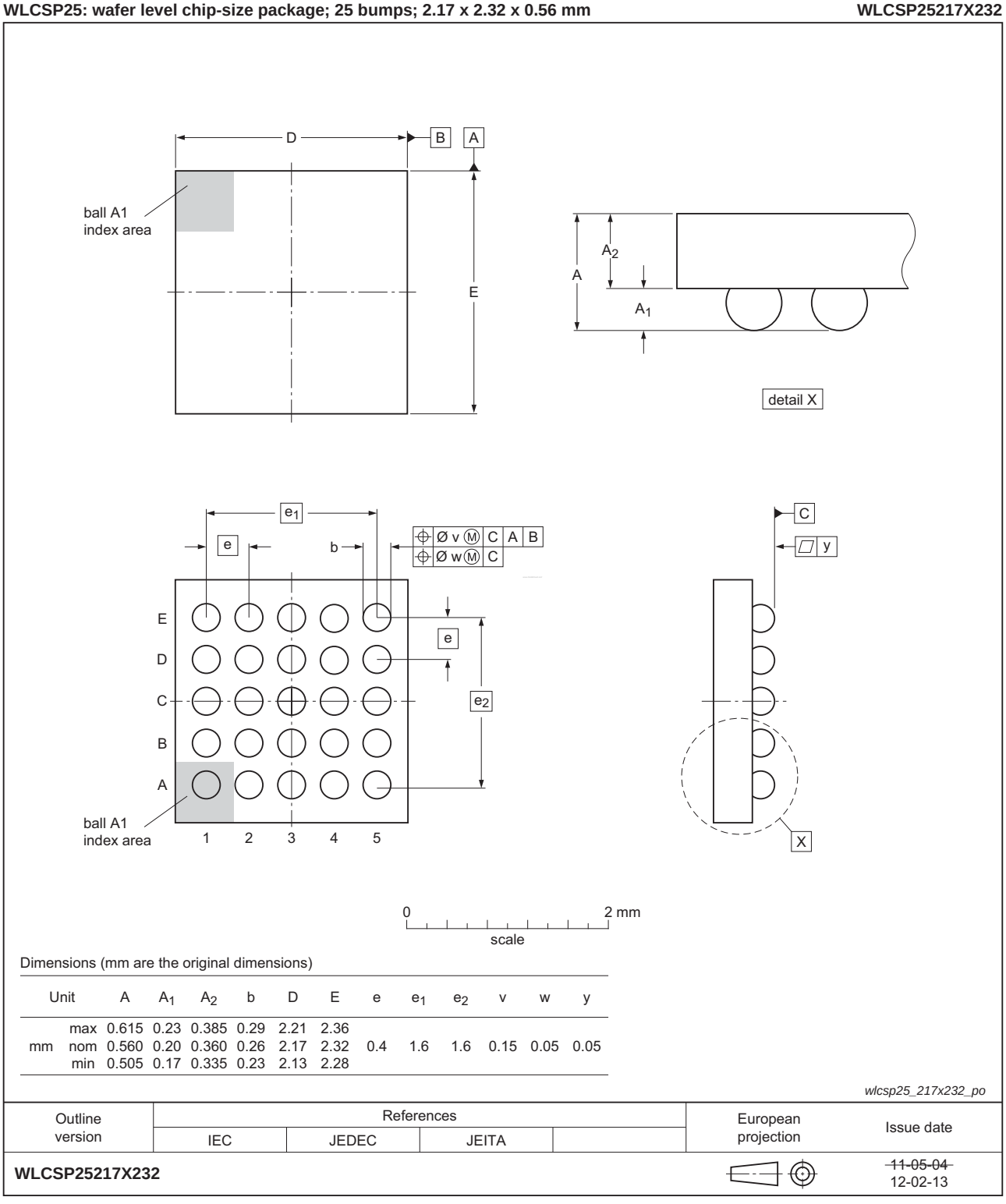
12. Package outline

WLCSP25: wafer level chip-size package; 25 bumps; 2.17 x 2.32 x 0.56 mm **WLCSP25217X232**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
	max	0.615	0.23	0.385	0.29	2.21	2.36						
mm	nom	0.560	0.20	0.360	0.26	2.17	2.32	0.4	1.6	1.6	0.15	0.05	0.05
	min	0.505	0.17	0.335	0.23	2.13	2.28						

wlcsp25_217x232_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
WLCSP25217X232						~~11-05-04~~ 12-02-13

Fig 29. Package outline (WLCSP25)

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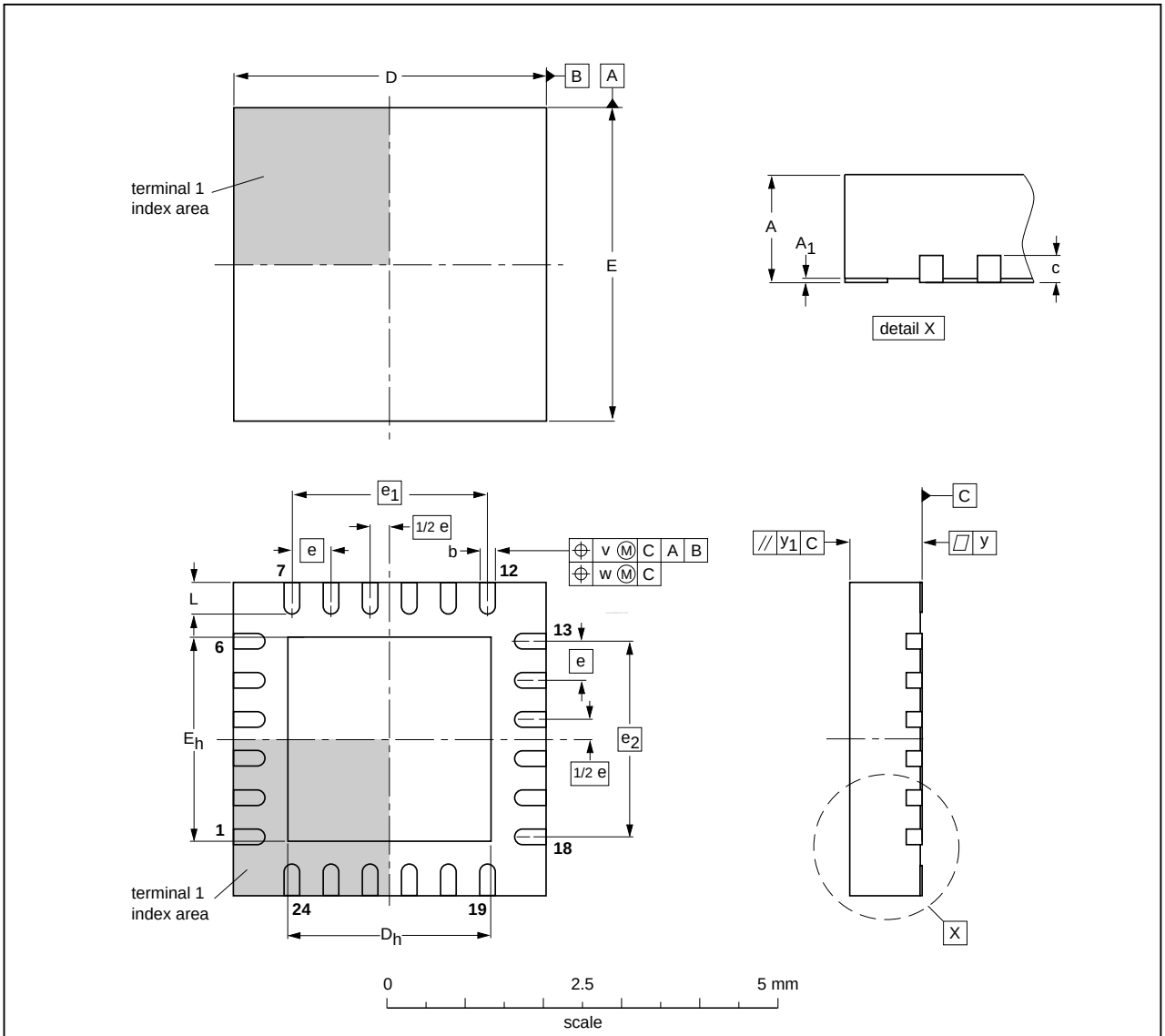
HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-3**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.75 2.45	4.1 3.9	2.75 2.45	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-3	- - -	MO-220	- - -			~~04-11-19~~ 05-03-10

Fig 30. Package outline (HVQFN24)

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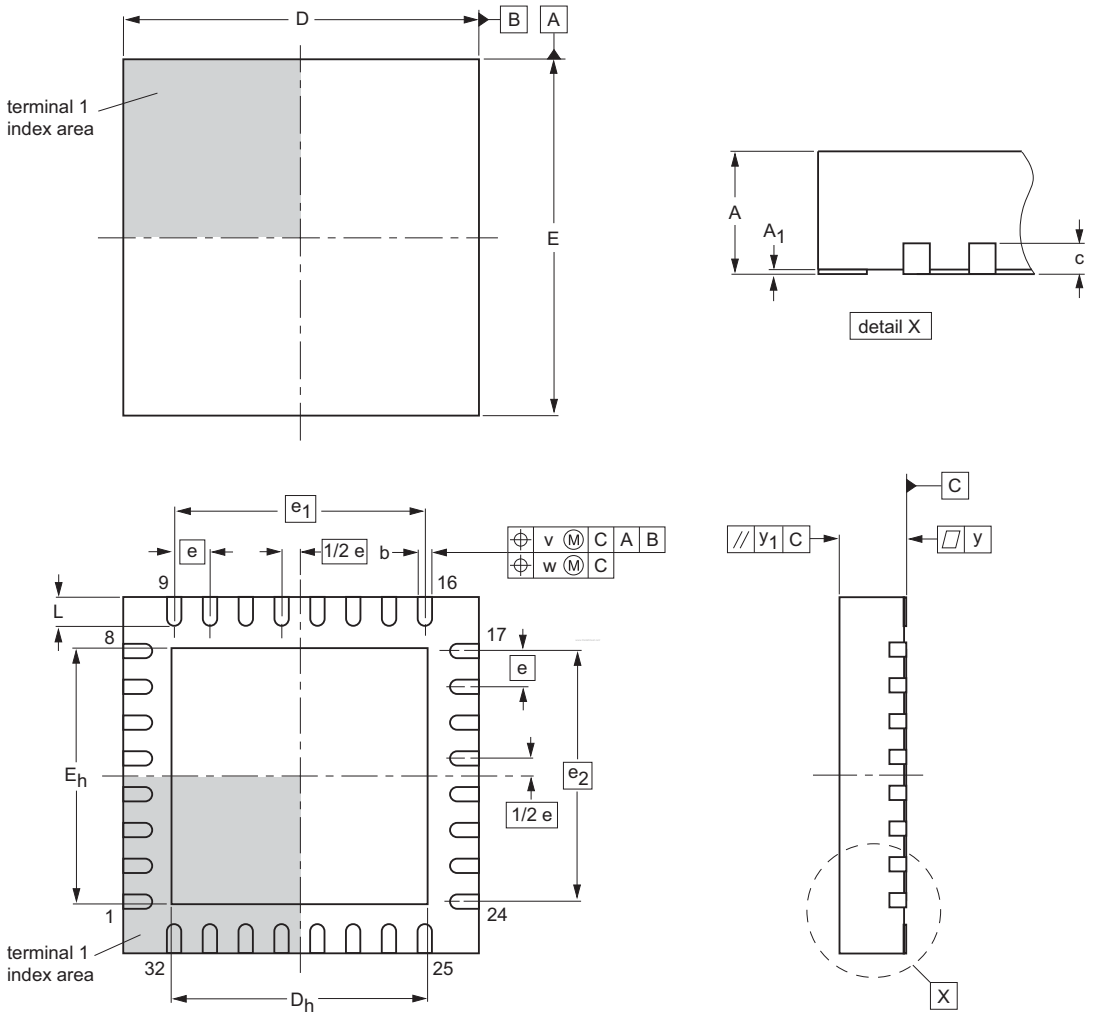
HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm



Dimensions (mm are the original dimensions)

Unit[1]		A[1]	A_1	b	c	D[1]	D_h	E[1]	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	0.85	0.05	0.30	0.2	5.1	3.75	5.1	3.75	0.5	3.5	3.5	0.5	0.1	0.05	0.05	0.1
	nom																
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33f_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
		MO-220				~~11-10-11~~ 11-10-17

Fig 31. Package outline (HVQFN33)

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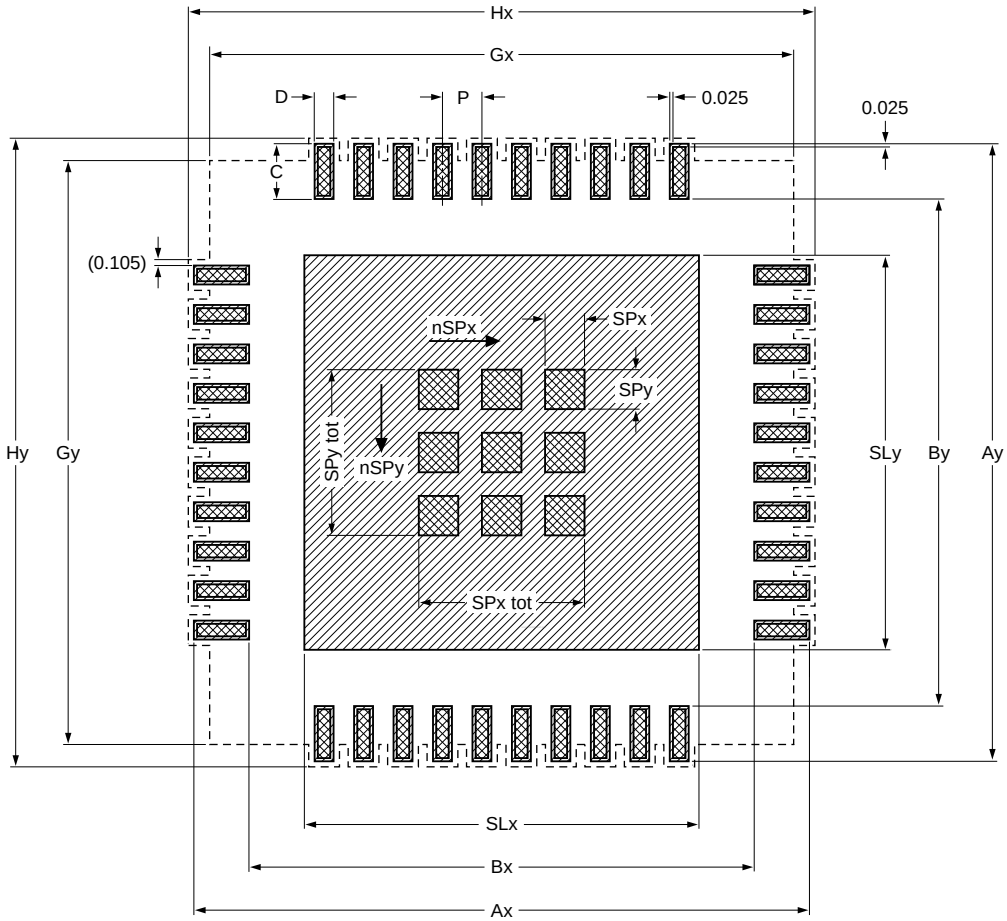
13. Soldering

Footprint information for reflow soldering of HVQFN24 package **SOT616-3**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

solder paste deposit

solder land plus solder paste

occupied area

nSPx	nSPy
2	2

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.500	5.000	5.000	3.200	3.200	0.900	0.240	2.500	2.500	1.500	1.500	0.550	0.550	4.300	4.300	5.250	5.250

Issue date ~~07-05-07~~ 09-06-15 *sot616-3_fr*

Fig 32. Reflow soldering for the HVQFN24 package

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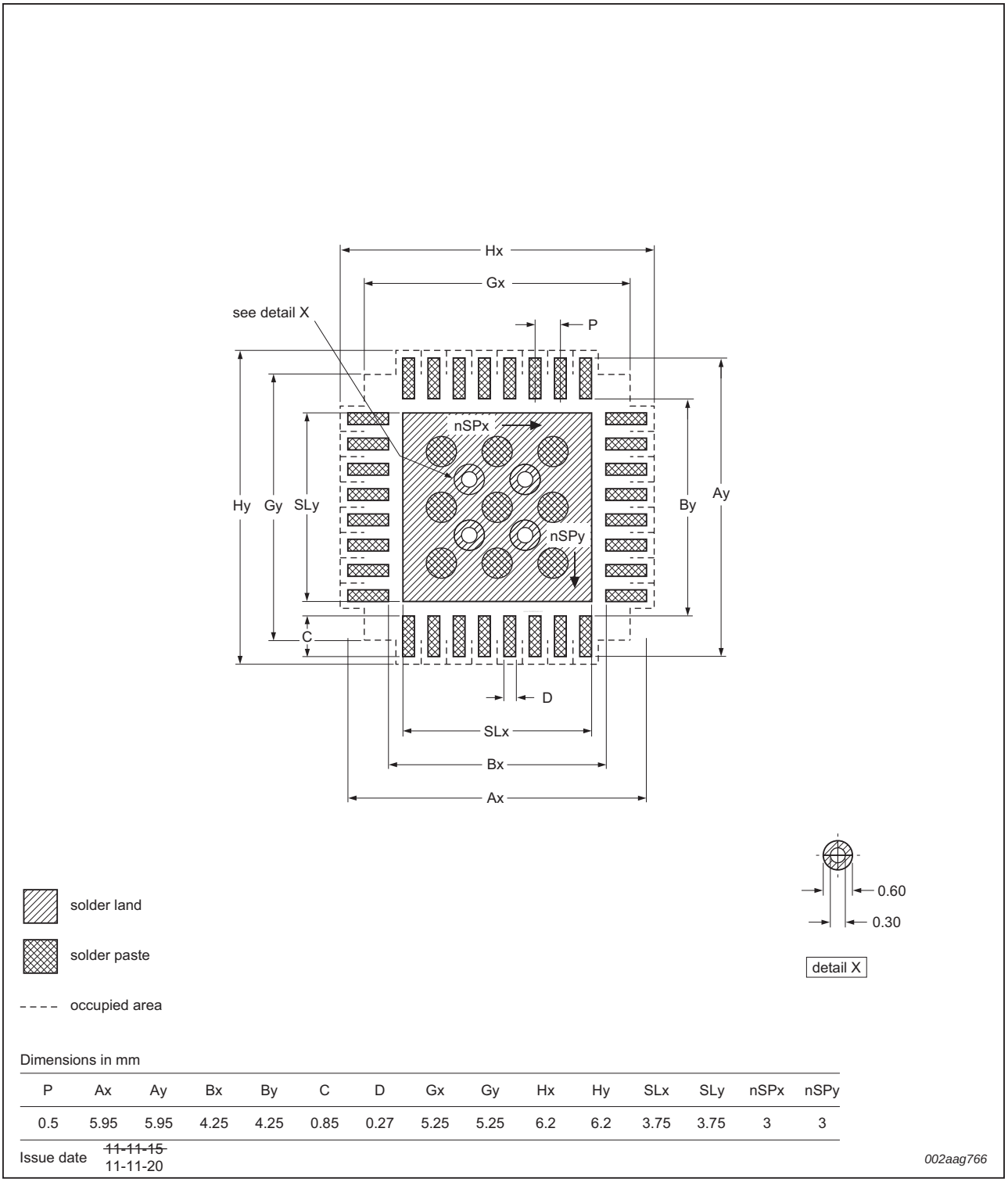
Footprint information for reflow soldering of HVQFN33 package



Dimensions in mm

P	Ax	Ay	Bx	By	C	D	Gx	Gy	Hx	Hy	SLx	SLy	nSPx	nSPy
0.5	5.95	5.95	4.25	4.25	0.85	0.27	5.25	5.25	6.2	6.2	3.75	3.75	3	3

Issue date ~~11-11-15~~ 11-11-20

002aag766

Fig 33. Reflow soldering for the HVQFN33 (5x5) package

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14. Abbreviations

Table 15. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	Brown-Out Detect
GPIO	General-Purpose Input/Output
JEDEC	Joint Electron Devices Engineering Council
NVM	Non-Volatile Memory
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
TTL	Transistor-Transistor Logic
USART	Universal Synchronous Asynchronous Receiver/Transmitter

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15. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC111XLV_LPC11XXLVUK v.2	20121010	Product data sheet	-	LPC111XLV_LPC11XXLVUK v.1
Modifications:	• Functions CT16B0_CAP1/RXD added to pin PIO3_4. • Functions CT16B1_CAP1/TXD added to pin PIO3_5. • Function CT32B1_CAP1 added to pin PIO1_11. • Capture/clear functionality added to counter/timers. See Section 7.12. • Figure 21 “Deep-sleep mode: Typical supply current I_{DD} versus temperature” updated. • Electrical pin characteristics data combined in Section 9.2 for dual and single power supplies. • SSP timing characteristics in slave mode removed for single power supply parts in Table 14. • Table 11 “Dynamic characteristic: internal oscillators” and Figure 23 updated. • Figure 33 corrected. • Removed dual-power supply option. All parts use a single 1.8 V +/- 10 % power supply. • Removed 10-bit ADC. Only the 8-bit ADC is available. • Temperature range for ADC characteristics on the HVQFN24 package restricted to T_{amb} = -10 °C to +85 °C. • BOD interrupt level 0 removed in Table 8. • IRC accuracy updated to 2.5 % accuracy for T_{amb} = -20 °C to +85 °C and to 5 % accuracy for T_{amb} = -40 °C to -20 °C. • Data sheet status changed to Product data sheet.			
LPC111XLV_LPC11XXLVUK v.1	20120621	Objective data sheet	-	-

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16. Legal information

17. Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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