

# New Jersey Semi-Conductor Products, Inc.

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## 2N5719-2N5723 SCRs .5 Amp, Planar

### ABSOLUTE MAXIMUM RATINGS

	2N5719	2N5720	2N5721	2N5722	2N5723
Repetitive Peak Off-State Voltage, $V_{DRM}$	60V	100V	200V	300V	400V
Repetitive Peak Reverse Voltage, $V_{RRM}$	60V	100V	200V	300V	400V
Non-Repetitive Peak Off-State Voltage, $V_{DSM}$	500V				
DC On-State Current, $I_T$					
75°C Ambient	250mA				
100°C Case	500mA				
Repetitive Peak On-State Current, $I_{TRM}$	up to 30A				
Peak One Cycle Surge (Non-Rep) On-State Current, $I_{TSM}$	8A				
Peak Gate Current, $I_{GM}$	250mA				
Average Gate Current, $I_{G(AV)}$	25mA				
Reverse Gate Current, $I_{GR}$	3mA				
Reverse Gate Voltage, $V_{GR}$	6V				
Operating and Storage Temperature Range	-65°C to +150°C				

### ELECTRICAL SPECIFICATIONS

Test	Symbol	Min.	Typical	Max.	Units	Test Conditions
<b>SUBGROUP 1</b>						
Visual and Mechanical	—	—	—	—	—	
<b>SUBGROUP 2 (25°C TESTS)</b>						
Off-State Current	$I_{DRM}$	—	.01	0.1	$\mu A$	$R_{GK} = 1K, V_{DRM} = \text{Rating}$
Reverse Current	$I_{RRM}$	—	.01	0.1	$\mu A$	$R_{GK} = 1K, V_{RRM} = \text{Rating}$
Reverse Gate Voltage	$V_{GR}$	5	8	—	V	$I_{GR} = 0.1mA$
Gate Trigger Current	$I_{GT}$	—	2	20	$\mu A$	$R_{GS} = 10K, V_D = 5V$
Gate Trigger Voltage	$V_{GT}$	0.44	0.50	0.6	V	$R_{GS} = 100\Omega, V_D = 5V$
On-State Voltage	$V_T$	—	1.2	1.5	V	$i_T = 0.5A$ (pulse test)
Holding Current	$I_H$	0.3	0.8	2.0	mA	$R_{GK} = 1K, V_D = 5V$
<b>SUBGROUP 3 (25°C TESTS)</b>						
Off-State Voltage — Critical Rate of Rise	$dv/dt$	100	150	—	$V/\mu S$	$R_{GK} = 1K, V_D = 30V$
Gate Trigger — on Pulse Width	$t_{pg(on)}$	—	0.1	0.5	$\mu S$	$I_G = 10mA, I_T = 1A, V_D = 30V$
Delay Time	$t_d$	—	0.1	—	$\mu S$	$I_G = 10mA, I_T = 1A, V_D = 30V$
Rise Time	$t_r$	—	0.3	—	$\mu S$	$I_G = 10mA, I_T = 1A, V_D = 30V$
Circuit Commutated Turn-Off Time	$t_q$	—	15	30	$\mu S$	$I_T = 1A, i_r = 1A, R_{GK} = 1K$
2N5724, 2N5725, 2N5726, 2N5727, 2N5728		—	30	50	$\mu S$	
<b>SUBGROUP 4 (150° TESTS)</b>						
High Temp. Off-State Current	$I_{DRM}$	—	10	100	$\mu A$	$R_{GK} = 1K, V_{DRM} = \text{Rating}$
High Temp. Reverse Current	$I_{RRM}$	—	20	100	$\mu A$	$R_{GK} = 1K, V_{RRM} = \text{Rating}$
High Temp. Gate Trigger Voltage	$V_{GT}$	0.10	0.15	—	V	$R_{GS} = 100\Omega, V_D = 5V$
High Temp. Holding Current	$I_H$	0.10	0.15	—	mA	$R_{GK} = 1K, V_D = 5V$
<b>SUBGROUP (-65°C TESTS)</b>						
Low Temp. Gate Trigger Voltage	$V_{GT}$	—	0.7	0.9	V	$R_{GS} = 100\Omega, V_D = 5V$
Low Temp. Gate Trigger Current	$I_{GT}$	—	50	125	$\mu A$	$R_{GS} = 10K, V_D = 5V$
Low Temp. Holding Current	$I_H$	—	1.2	3.0	mA	$R_{GK} = 1K, V_D = 5V$

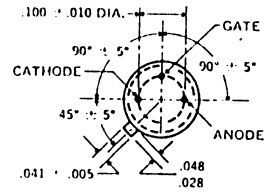
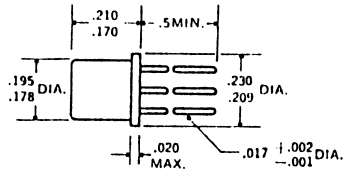
Note 1. See rating curves for full rating information.

2. Blocking voltage ratings apply over the full operating temperature range, provided the gate is connected to the cathode through a resistor, 1K or smaller, or other adequate gate bias is used.

NJ Semi-Conductors reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by NJ Semi-Conductors is believed to be both accurate and reliable at the time of going to press. However NJ Semi-Conductors assumes no responsibility for any errors or omissions discovered in its use. NJ Semi-Conductors encourages customers to verify that datasheets are current before placing orders.

MECHANICAL SPECIFICATIONS

2N5719-2N5723



Dimensions in inches.

T0-18

