TOSHIBA

TOSHIBA Original CMOS 8-Bit Microcontroller

TLCS-870 Series

TMP87PM75FG

TOSHIBA CORPORATION

Semiconductor Company

Important Notices

Thank you for your continued patronage of Toshiba microcontrollers.

This page gives you important information on using Toshiba microcontrollers. Please be sure to check each item for proper use of our products.

TOSHIBA Microcontrollers
870 Family
(TMP87CH75) (TMP87CM75) (TMP87PM75)

Datasheet Modifications: I²C Bus Mode Control

The following problem is included in the explanation of the I²C bus function of this data sheet.
It will guide the correction as follows. Please read it for the explanation of this data sheet as follows.

Section: "I²C Bus Mode Control"

- In the explanation of the Serial Bus Interface Control Register 1
  1. Delete the setting examples where the serial clock frequency exceeds 100 kHz.
  2. Add the following note.

SCK	Serial clock selection	000 : Reserved (Note) 001 : Reserved (Note) 010 : 57.1 kHz 011 : 29.9 kHz 100 : 15.3 kHz 101 : 7.72 kHz 110 : 3.88 kHz 111 : reserved	at fc = 8MHz (Output on SCL pin)	Write only

Note: This I²C bus circuit does not support the Fast mode. It supports the Standard mode only. Although the I²C bus circuit itself allows the setting of a baud rate over 100 kbps, the compliance with the I²C specification is not guaranteed in that case.

- In "(3) Serial clock"
  1. Add the following sentence about the communication baud rate.

a. Clock source

The SCK (bits 2 to 0 in the SBICR1) is used to select a maximum transfer frequency outputted on the SCL pin in the master mode. Set a communication baud rate that meets the I²C bus specification, such as the shortest pulse width of t_{LOW}, based on the equations shown below.

Four or more machine cycles are required for both the high and low levels of the pulse width of a clock which is input externally in both the master and slave mode.

$t_{LOW} = 2^n/f_c$

$t_{HIGH} = 2^n/f_c + 12/f_c$

$fscl = 1/(t_{Low} + t_{HIGH})$

Document Change Notification

The purpose of this notification is to inform customers about the launch of the Pb-free version of the device. The introduction of a Pb-free replacement affects the datasheet. Please understand that this notification is intended as a temporary substitute for a revision of the datasheet.

Changes to the datasheet may include the following, though not all of them may apply to this particular device.

1. Part number

   Example: TMPxxxxxxF → TMPxxxxxxFG

   All references to the previous part number were left unchanged in body text. The new part number is indicated on the prelims pages (cover page and this notification).

2. Package code and package dimensions

   Example: LQFP100-P-1414-0.50C → LQFP100-P-1414-0.50F

   All references to the previous package code and package dimensions were left unchanged in body text. The new ones are indicated on the prelims pages.

3. Addition of notes on lead solderability

   Now that the device is Pb-free, notes on lead solderability have been added.

4. RESTRICTIONS ON PRODUCT USE

   The previous (obsolete) provision might be left unchanged on page 1 of body text. A new replacement is included on the next page.

5. Publication date of the datasheet

   The publication date at the lower right corner of the prelims pages applies to the new device.

1. Part number

2. Package code and dimensions

Previous Part Number (in Body Text)	Previous Package Code (in Body Text)	New Part Number	New Package Code	OTP
TMP87PM75F	P-QFP100-1420-0.65A	TMP87PM75FG	QFP100-P-1420-0.65A	—

*: For the dimensions of the new package, see the attached Package Dimensions diagram.

3. Addition of notes on lead solderability

The following solderability test is conducted on the new device.

Lead solderability of Pb-free devices (with the G suffix)

Test	Test Conditions	Remark
Solderability	(1) Use of Lead (Pb) ·solder bath temperature = 230°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux (2) Use of Lead (Pb)-Free ·solder bath temperature = 245°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux	Leads with over 95% solder coverage till lead forming are acceptable.

4. RESTRICTIONS ON PRODUCT USE

The following replaces the "RESTRICTIONS ON PRODUCT USE" on page 1 of body text.

5. Publication date of the datasheet

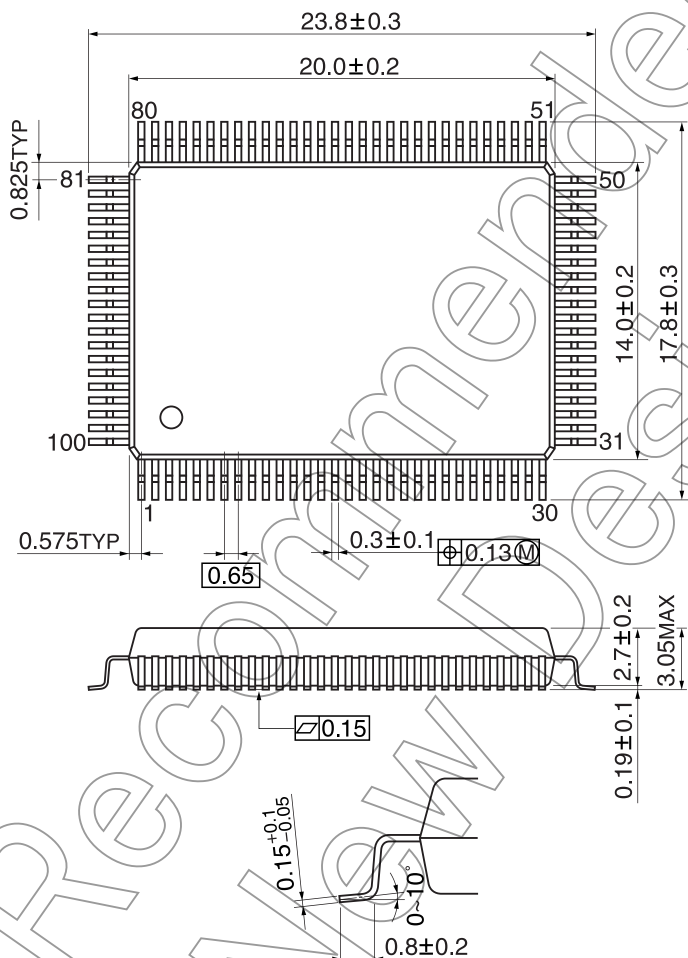
The publication date of this datasheet is printed at the lower right corner of this notification.

(Annex)

Package Dimensions

QFP100-P-1420-0.65A

Unit: mm



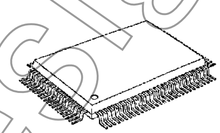
CMOS 8-Bit Microcontroller

TMP87PM75F

The 87PM75 is a One-Time PROM microcontroller with low-power 256 K bits (32 Kbytes) electrically programmable read only memory for the 87CH75/CM75 system evaluation. The 87PM75 is pin compatible with the 87CH75/CM75. The operations possible with the 87CH75/CM75 can be performed by writing programs to PROM. The 87PM75 can write and verify in the same way as the TC57256AD using an adaptor socket BM11124 and an EPROM programmer.

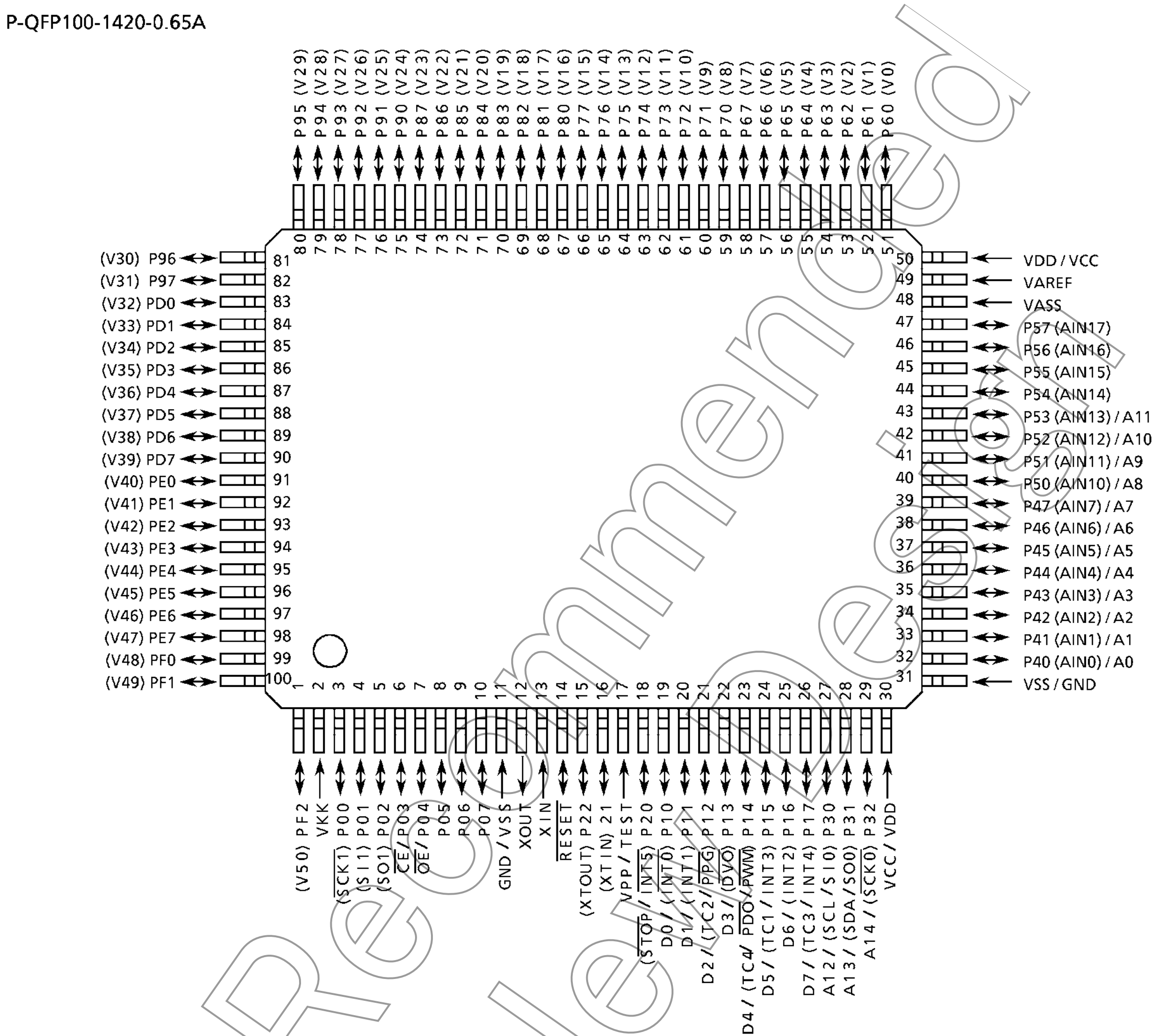
Part No.	OTP	RAM	Package	Adaptor Socket
TMP87PM75F	32 K × 8-bit	1 K × 8-bit	P-QFP100-1420-0.65A	BM11124

P-QFP100-1420-0.65A



TMP87PM75F

Pin Assignments (Top View)



Note: All VDDs should be connected externally for keeping the same voltage level.

Pin Function

The 87PM75 has two modes: MCU and PROM.

(1) MCU mode
In this mode, the 87PM75 is pin compatible with the 87CH75/CM75 (fix the TEST pin at low level).

(2) PROM mode

Pin Name (PROM mode)	Input / Output	Functions	Pin Name (MCU mode)
A14 to A12	Input	PROM address inputs	P32 to P30
A11 to A8			P53 to P50
A7 to A0			P47 to P40
D7 to D0	I/O	PROM data input/outputs	P17 to P10
$\overline{CE}$	Input	Chip enable signal input (active low)	P03
$\overline{OE}$		Output enable signal input (active low)	P04
VPP	Power supply	+ 12.5 V / 5 V (Program supply voltage)	TEST
VCC		+ 5 V	VDD
GND		0 V	VSS
P57 to P54	I/O	Pull-up with resistance for input processing	
P05, P02, P01		PROM mode setting pin. Be fixed at high level.	
P21			
P07, P06, P00		PROM mode setting pin. Be fixed at low level.	
P22, P20			
$\overline{RESET}$			
XIN	Input	Connect an 8 MHz oscillator to stabilize the internal state.	
XOUT	Output		
PF2 to PF0	I/O	Open	
PE7 to PE0			
PD7 to PD0			
P97 to P90			
P87 to P80			
P77 to P70			
P67 to P60			
VKK	Power supply	0 V (GND)	
VAREF			
VASS			

OPERATIONAL DESCRIPTION

The following explains the 87PM75 hardware configuration and operation. The configuration and functions of the 87PM75 are the same as those of the 87CH75/M75, except in that a one-time PROM is used instead of an on-chip mask ROM.

The 87PM75 is placed in the *single-clock* mode during reset. To use the dual-clock mode, the low-frequency oscillator should be turned on by executing [SET (SYSCR2). XTEN] instruction at the beginning of the program.

1. OPERATING MODE

The 87PM75 has two modes: MCU and PROM.

1.1 MCU Mode

The MCU mode is activated by fixing the TEST / VPP pin at low level.

In the MCU mode, operation is the same as with the 87CH75/M75 (the TEST / VPP pin cannot be used open because it has no built-in pull-down resistance).

1.1.1 Program Memory

The 87PM75 has a 32K × 8-bit (addresses 8000_H-$FFFF_H$ in the MCU mode, addresses 0000_H-$7FFF_H$ in the PROM mode) of program memory (OTP).

The use the 87PM75 as the system evaluation for the 87CH75/CM75, the program should be writen to the program memory area as shown in Figure 1-1.

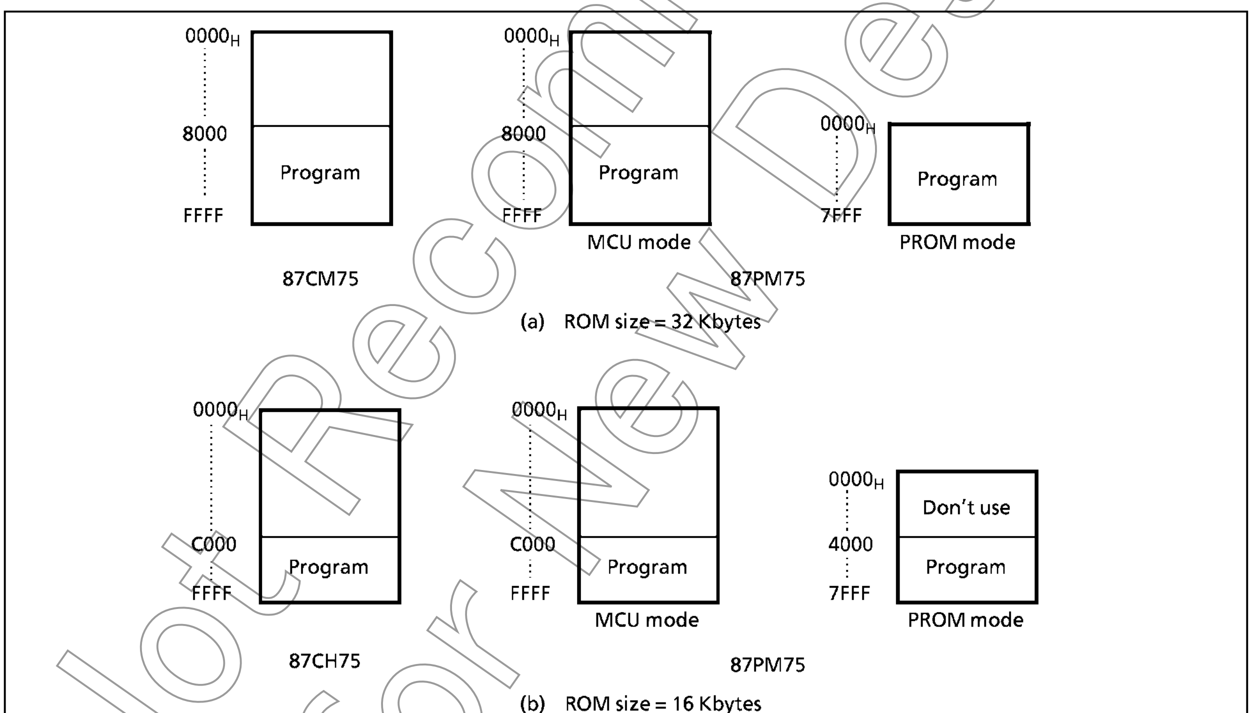


Figure 1-1. Program Memory Area

Note: Either write the data FF_H to the unused area or set the PROM programmer to access only the program storage area.

1.1.2 Data Memory

The 87PM75 has an on-chip 1k × 8-bit data memory (static RAM).

1.1.3 Input/Output Circuitry

(1) Control pins

The control pins of the 87PM75 are the same as those of the 87CH75/CM75 except that the TEST pin has is no built-in pull-down resistance.

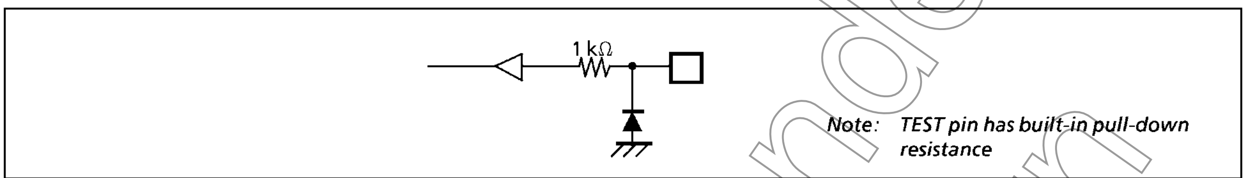


Figure 1-2. TEST Pin

(2) I/O ports

The I/O circuitries of 87PM75 I/O ports are the same as the code A type I/O circuitries of the 87CH75/M75.

Whe using as an evaluator of other I/O code D, external pull-down resistors are required.

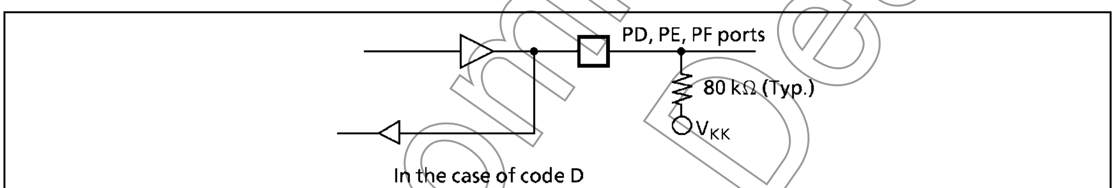


Figure 1-3. I/O Circuitry Code and External Circuitry

1.2 PROM Mode

The PROM mode is activated by setting the pins TEST, $\overline{RESET}$ and the ports P07-P00, P22-P20 as shown in Figure 1-4. The PROM mode is used to write and verify programs with a general-purpose PROM programmer. The high-speed programming mode I and II can be used for program operation. The 87PM75 is not supported an electric signature mode, so the ROM type must be set to TC57256AD.
Set the adaptor socket switch to "N".

Note: Please set the high-speed programming mode accoding to each manual of PROM programmer.

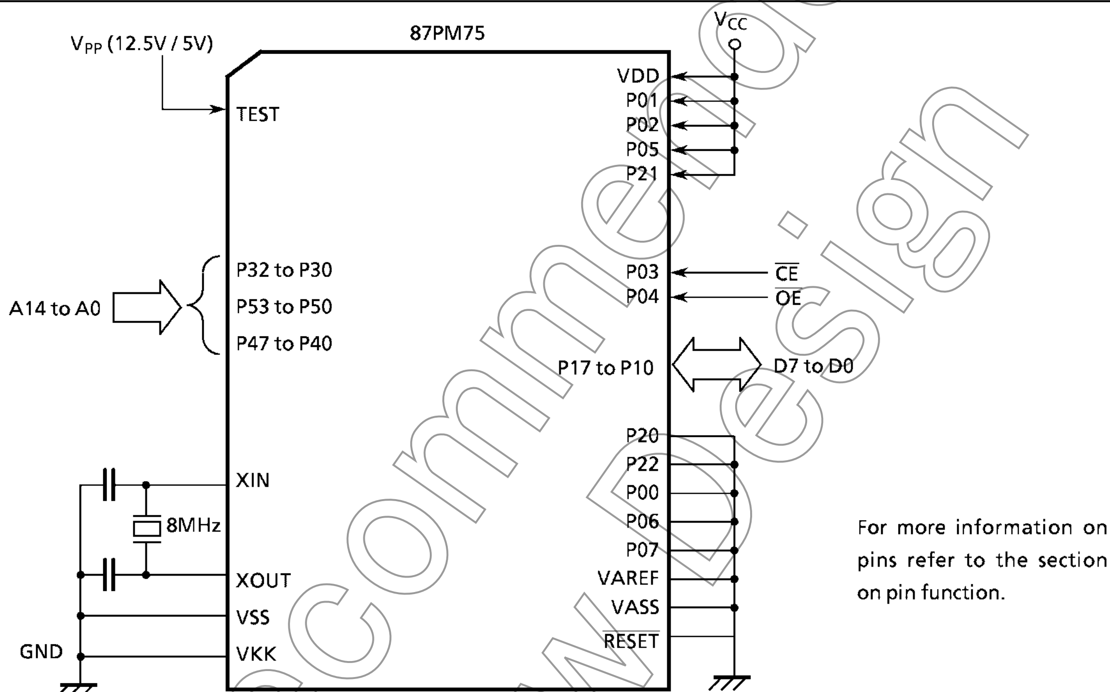


Figure 1-4. Setting for PROM Mode

1.2.1 Programming Flowchart (High-speed Programming Mode-I)

The high-speed programming mode is achieved by applying the program voltage (+12.5V) to the VPP pin when Vcc = 6V. After the address and input data are stable, the data is programmed by applying a single 1ms program pulse to the $\overline{CE}$ input. The programmed data is verified. If incorrect, another 1ms program pulse is applied and then the programmed data is verified. This process should be repeated (up to 25 times) until the program operates correctly. Programming for one address is ended by applying additional program pulse with width 3 times that needed for initial programming (number of programmed times × 1ms). After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5V.

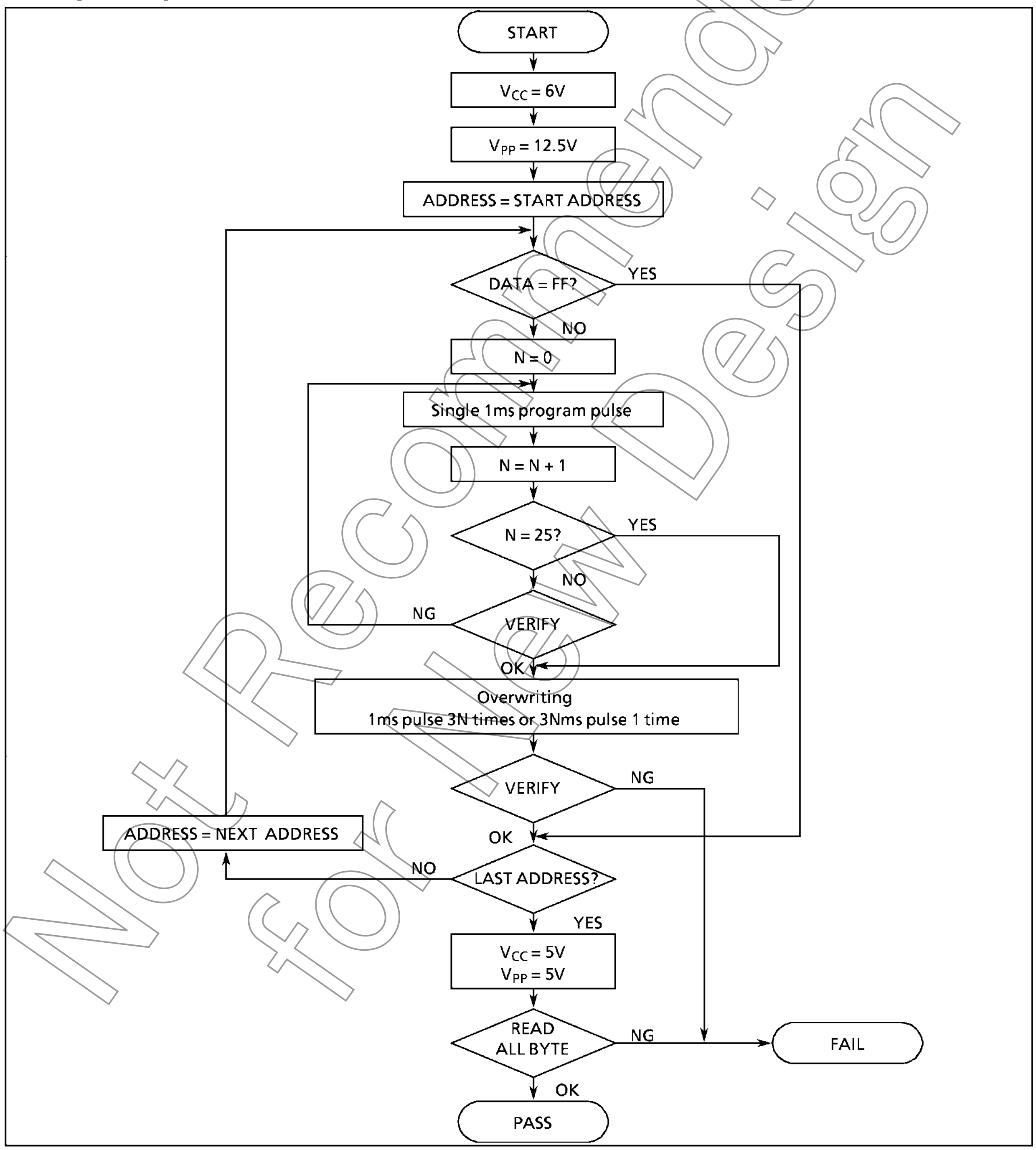


Figure 1-5. Flow Chart of High-speed Programming Mode - I

1.2.2 Programming Flowchart (High-speed Programming Mode-II)

The high-speed programming mode is achieved by applying the program voltage (+ 12.75 V) to the Vpp pin when Vcc = 6.25 V. After the address and input data are stable, the data is programmed by applying a single 0.1ms program pulse to the $\overline{CE}$ input. The programmed data is verified. If incorrect, another 0.1ms program pulse is applied and then the programmed data is verified. This process should be repeated (up to 25 times) until the program operates correctly. After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.

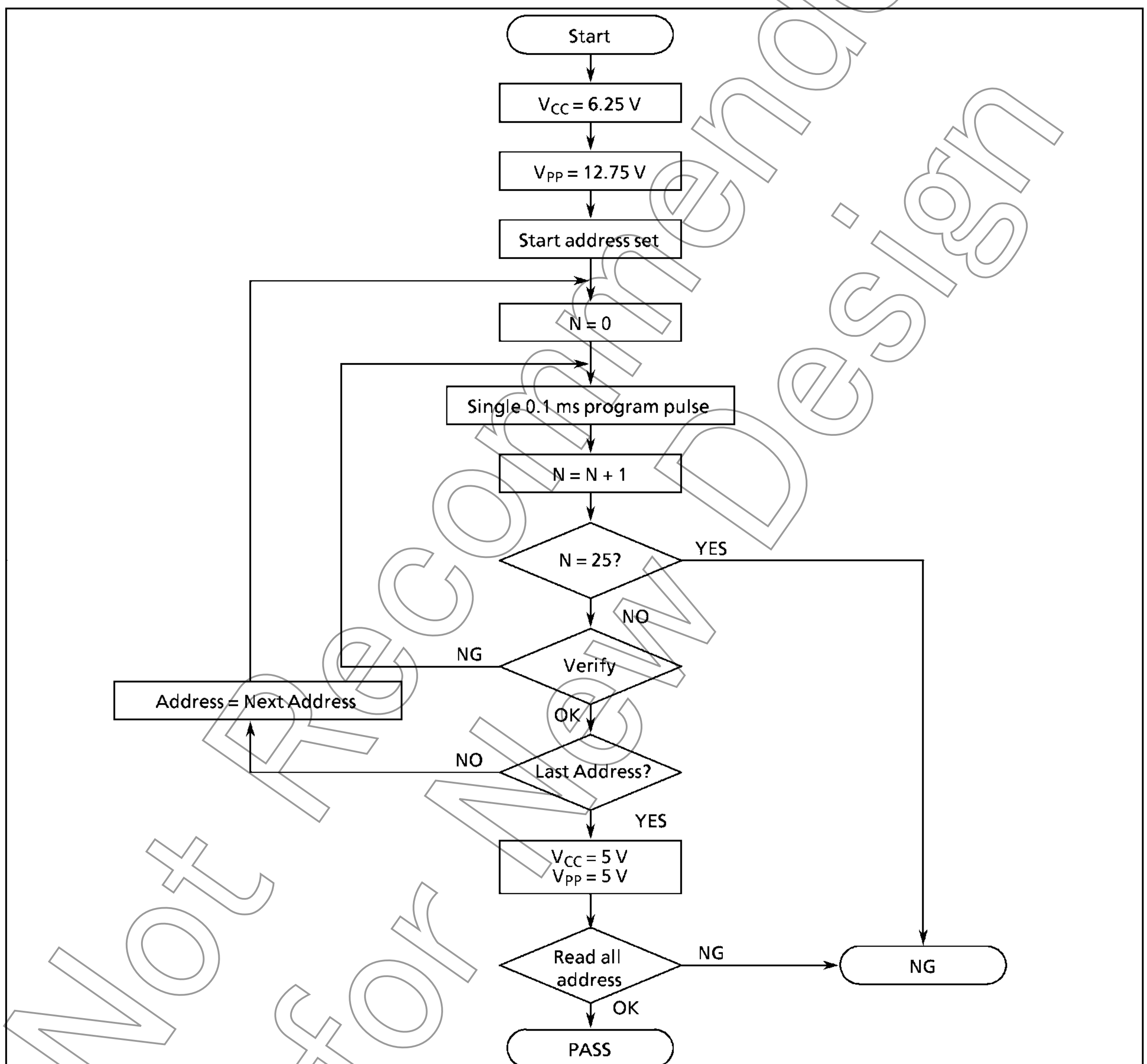


Figure 1-6. Flowchart of High-speed Programming Mode - II

1.2.3 Writing Method for General-purpose PROM Program

(1) Adapters
BM11124: TMP87PM75F

(2) Adapter setting
Switch (SW1) is set to side N.

(3) PROM programmer specifying

i) PROM type is specified to TC57256AD.
Writing voltage: 12.5 V (high-speed program Ⅰ mode)
12.75 V (high-speed program Ⅱ mode)

ii) Data transfer (copy) (note 1)
In TMP87PM75, EPROM is within the addresses 0000_H to $7FFF_H$. Data is required to be transferred (copied) to the addresses where it is possible to write. The program area in MCU mode and PROM mode is referred to "Program memory area" in Figure 1-1.

Ex. In the block transfer (copy) mode, executed as below.
ROM capacity of 32KB: transferred addresses 8000_H to $FFFF_H$ to addresses 0000_H to $7FFF_H$
ROM capacity of 16KB: transferred addresses $C000_H$ to $FFFF_H$ to addresses 4000_H to $7FFF_H$

iii) Writing address is specified. (note 1)
Start address: 0000_H (When ROM capacity of 16KB, start address is 4000_H)
End address: $7FFF_H$

(4) Writing
Writing/Verifying is required to be executed in accordance with PROM programmer operating procedure.

Note 1:	*The specifying method is referred to the PROM programmer description. Either write the data FF_H to addresses 0000_H to $3FFF_H$ when ROM capacity of 16KB.*
Note 2:	*When MCU is set to an adapter or the adapter is set to PROM programmer, a position of pin 1 must be adjusted. If the setting is reserved, MCU, the adapter and PROM program is damaged.*
Note 3:	*The TMP87PM75 does not support the electric signature mode (hereinafter referred to as "signature"). If the signature is used in PROM program, a device is damaged due to applying 12V ± 0.5V to the address pin 9 (A9). The signature must not be used.*

Electrical Characteristics

Absolute Maximum Ratings

(V_{SS} = 0 V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Program Voltage	V_{PP}	TEST / VPP	– 0.3 to 13.0	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	P2, P3, P4, P5, P6, XOUT, $\overline{RESET}$	– 0.3 to V_{DD} + 0.3	V
	V_{OUT3}	Source open drain ports	V_{DD} – 40 to V_{DD} + 0.3	
Output Current (Per 1 pin)	I_{OUT1}	P15 to P17, P3, P4, P5	3.2	mA
	I_{OUT2}	P0, P10 to P14, P2	30	
	I_{OUT3}	P8, P9, PD, PE, PF	– 12	
	I_{OUT4}	P6, P7	– 25	
Output Current (Total)	ΣI_{OUT1}	P15 to P17, P3, P4, P5	60	mA
	ΣI_{OUT2}	P0, P10 to P14, P2	160	
	ΣI_{OUT3}	P6, P7, P8, P9, PD, PE, PF	– 200	
Power Dissipation [Topr = 25°C]	PD	Note 2	1200	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 70	°C

Note 1: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Note 2: Power Dissipation (PD) ; For PD, it is necessary to decrease 14.3 mW/°C.

Note 3: All VDDs should be connected externally for keeping the same voltage level.

Recommended Operating Conditions

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 8 MHz	NORMAL 1, 2 modes	4.5	5.5	V
				IDLE1, 2 modes			
			fs = 32.768 kHz	SLOW mode	2.7		
				SLEEP mode			
				STOP mode	2.0		
Output Voltage	V_{OUT3}	Source open drain ports			V_{DD} – 38	V_{DD}	V
Input High Voltage	V_{IH1}	Except hysteresis input	V_{DD} ≧ 4.5 V		V_{DD} × 0.70	V_{DD}	V
	V_{IH2}	Hysteresis input			V_{DD} × 0.75		
	V_{IH3}		V_{DD} < 4.5 V		V_{DD} × 0.90		
Input Low Voltage	V_{IL1}	Except hysteresis input	V_{DD} ≧ 4.5 V		0	V_{DD} × 0.30	V
	V_{IL2}	Hysteresis input				V_{DD} × 0.25	
	V_{IL3}		V_{DD} < 4.5 V			V_{DD} × 0.10	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 V to 5.5 V		0.4	8.0	MHz
			V_{DD} = 2.7 V to 5.5 V			4.2	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc: Supply voltage range is specified in NORMAL 1/2 mode and IDLE 1/2 mode.

D.C. Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V	–	–	± 2	μA
	I_{IN2}	Open drain ports, Tri-state ports					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$	V_{IN} = 5.5 V / 0 V				
	I_{IN4}	PD, PE, PF ports (Note3)		–	–	80	
Input Resistance	R_{IN2}	$\overline{RESET}$		100	220	450	kΩ
Pull-down Resistance	R_K	Source open drain ports	V_{DD} = 5.5 V, V_{KK} = – 30 V	50	80	110	
Output Leakage Current	I_{LO1}	Sink open drain ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
	I_{LO2}	Source open drain ports	V_{DD} = 5.5 V, V_{OUT} = – 32 V	–	–	– 2	
	I_{LO3}	Tri-state ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V / 0 V	–	–	± 2	
Output High Voltage	V_{OH2}	Tri-state ports	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	V
	V_{OH3}	P8, P9, PD, PE, PF	V_{DD} = 4.5 V, I_{OH} = – 8 mA	2.4	–	–	
Output Low Voltage	V_{OL}	Except XOUT, P0, P10 to P14, P2	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	V
Output Low current	I_{OL3}	P0, P10 to P14, P2	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	20	–	mA
Output High current	I_{OH}	P6, P7	V_{DD} = 4.5 V, V_{OH} = 2.4 V	–	– 20	–	mA
Supply Current in NORMAL 1, 2 modes	I_{DD}		V_{DD} = 5.5 V fc = 8 MHz fs = 32.768 kHz V_{IN} = 5.3 V / 0.2 V	–	12	18	mA
Supply Current in IDLE 1, 2 modes				–	6	9	
Supply Current in SLOW mode			V_{DD} = 3.0 V fs = 32.768 kHz V_{IN} = 2.8 V / 0.2 V	–	30	60	μA
Supply Current in SLEEP mode				–	15	30	
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V	–	0.5	10	μA

Note 1: Typical values show those at Topr = 25°C , V_{DD} = 5 V.
Note 2: Input Current I_{IN1}, I_{IN3} : The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

A/D Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 to 6.0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}	$V_{AREF} - V_{ASS} \geqq 2.5$ V	V_{DD} – 1.5	–	V_{DD}	V
	V_{ASS}		V_{SS}			
Analog Input Voltage	V_{AIN}		V_{ASS}	–	V_{AREF}	V
Analog Supply Current	I_{REF}	V_{AREF} = 5.5 V, V_{ASS} = 0.0 V	–	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 5.0 V, V_{SS} = 0.0 V V_{AREF} = 5.000 V V_{ASS} = 0.000 V	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

Note: Quantizing error is not contained in those errors.

A.C. Characteristics

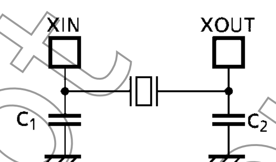
(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	t_{cy}	In NORMAL1, 2 modes	0.5	–	10	μs
		In IDLE1, 2 modes				
		In SLOW mode	117.6	–	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input), fc = 8 MHz	50	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	14.7	–	–	μs
Low Level Clock Pulse Width	t_{WSL}					

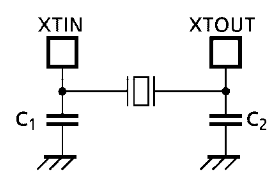
Recommended Oscillating Conditions

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Constant	
					C_1	C_2
High-frequency Oscillation	Ceramic Resonator	8 MHz	KYOCERA	KBR8.0M	30pF	30pF
		4 MHz	KYOCERA	KBR4.0MS		
			MURATA	CSA4.00MG		
	Crystal Oscillator	8 MHz	TOYOCOM	210B 8.0000	20pF	20pF
		4 MHz	TOYOCOM	204B 4.0000		
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	NDK	MX-38T	15pF	15pF



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note: An electrical shield by metal shied plate on the IC package should be recommend able in order to prevent the device from the high electric fieldstress applied for continuous reliable operation.

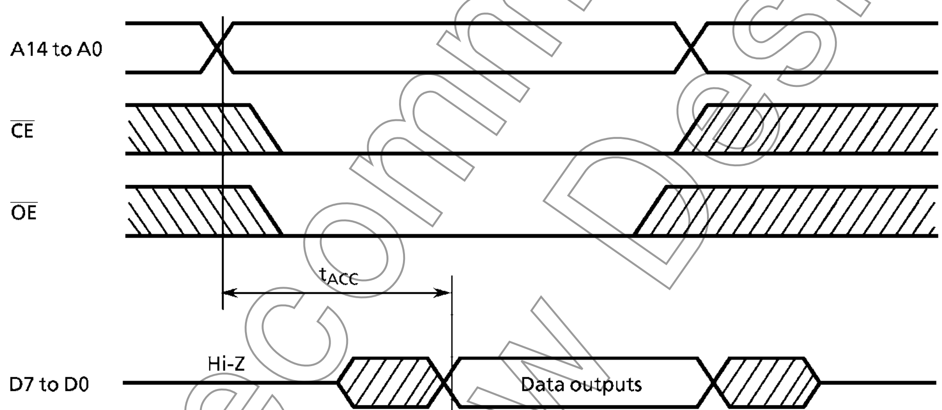
D.C./A.C. Characteristics (PROM mode)

(V_{SS} = 0 V)

(1) Read Operation (Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.12$	V
Power Supply Voltage	V_{CC}		4.75	5.00	5.25	V
Program Power Supply Voltage	V_{PP}		$V_{CC} - 0.6$ V	V_{CC}	$V_{CC} + 6.0$	V
Address Access Time	t_{ACC}	$V_{CC} = 5.0 \pm 0.5$ V	–	1.5 tcyc + 300	–	ns

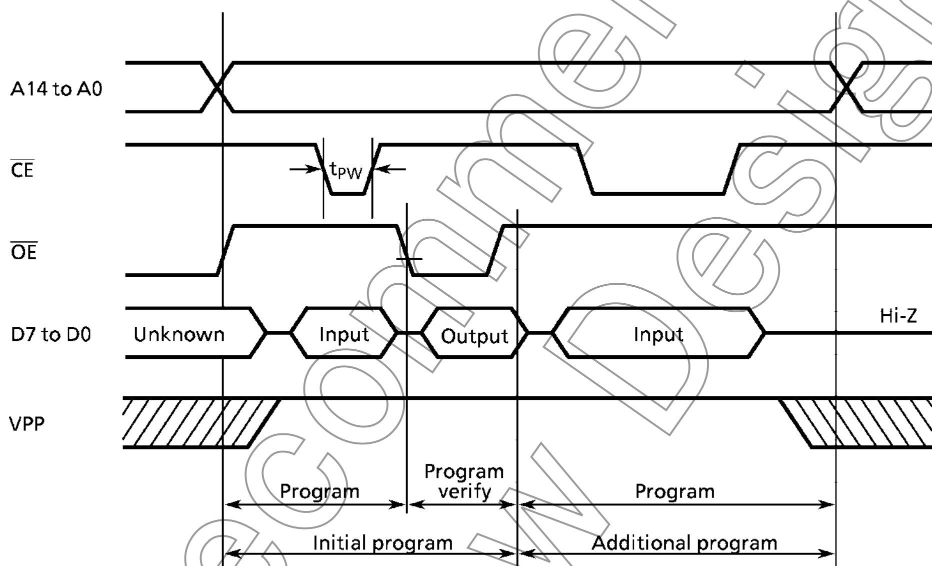
Note: tcyc = 500 ns at 8 MHz



Timing Waveforms of Read Operation

(2) High-Speed Programming Operation (Topr = 25 ± 5°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.12$	V
Power Supply Voltage	V_{CC}		5.75	6.0	6.25	V
Program Power Supply Voltage	V_{PP}		12.0	12.5	13.0	V
Initial Program Pulse Width	t_{PW}	V_{CC} = 6.0 V ± 0.25 V V_{PP} = 12.5 ± 0.25 V	0.95	1.0	1.05	ms

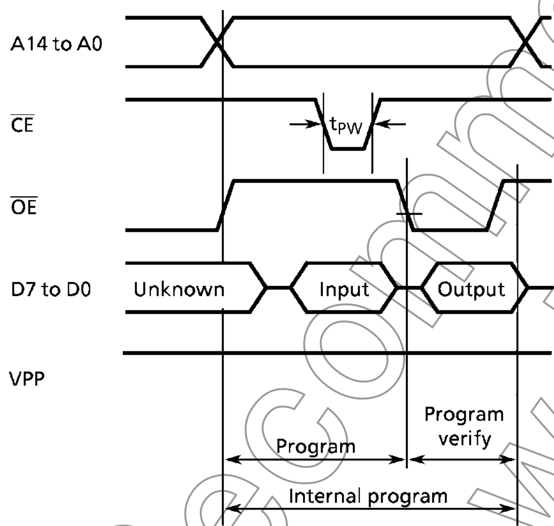


Note1:	*When V_{cc} power supply is turned on or after, V_{pp} must be increased.* *When V_{cc} power supply is turned off or before, V_{pp} must be decreased.*
Note2:	*The device must not be set to the EPROM programmer or picked up from it under applying the program voltage (12.75 V ± 0.5 V) to the V_{pp} pin as the device is damaged.*
Note3:	*Be sure to execute the recommended programing mode with the recommended programing adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.*

Timing Waveforms of Programming Operation

(3) Program Operation (High speed write mode - II) (Topr = 25 ± 5°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.12$	V
Supply Voltage	V_{CC}		6.00	6.25	6.50	V
Program Supply Voltage	V_{PP}		12.50	12.75	13.0	V
Initial Program Pulse Width	t_{PW}	V_{CC} = 6.0 V ± 0.25 V V_{PP} = 12.5 ± 0.25 V	0.095	0.1	0.105	ms



Note1: When V_{cc} power supply is turned on or after, V_{pp} must be increased.
When V_{cc} power supply is turned off or before, V_{pp} must be decreased.

Note2: The device must not be set to the EPROM programmer or picked up from it under applying the program voltage (12.75 V ± 0.25 V) to the V_{pp} pin as the device is damaged.