LXT331

Dual T1/E1 Line Interface Unit

Datasheet

The LXT331 is a Dual Line Interface Unit (DLIU) optimized for North America 1.544 Mbps (T1) and international 2.048 Mbps (E1/CEPT) applications. It features a constant low output impedance transmitter for high return loss. Transmit pulse shape is selectable for various line lengths and cable types. The data recovery circuit also offers selectable slicer ratios for T1 or E1 applications.

The LXT331 offers both a serial interface (SIO) for microprocessor control and a hardware control mode for stand-alone operation.

The LXT331 offers a variety of advanced diagnostic and performance monitoring features. It uses an advanced double-poly, double-metal CMOS process and requires only a single 5-volt power supply.

Applications

- Digital Access and Cross-connect Systems (DACS)
- T1/E1 Multiplexer
- SONET/SDH Multiplexers
- Digital Loop Carrier (DLC) terminals
- Cost efficient AFE for Digital Backend ASICS
- Analog LOS using PMRK/NMRK

Product Features

- Complete line driver and data recovery functions
- Constant low output impedance transmitter with a programmable equalizer that shapes pulses to meet the DSX-1 pulse template from 0 to 655 ft.
- High transmit and receive return loss
- Meets or exceeds industry specifications including ITU G.703 and ANSI T1. 102-1993
- Compatible with industry standard framers
- Minimum receive signal of 500 mV, with selectable slicer levels (E1/DSX-1) to improve SNR
- Analog loopback function
- Transmit performance monitors with Driver Fail Monitor (DFM) output for transmit driver short circuit detection
- Transmit Driver Performance Monitor (DPM) output on external pins MTIP and MRING
- Available in 44-pin PLCC and 44-pin QFP packages

As of January 15, 2001, this document replaces the Level One document *LXT331 — Dual T1/E1 Line Interface Unit*.

Order Number: 249074-001
January 2001

Datasheet

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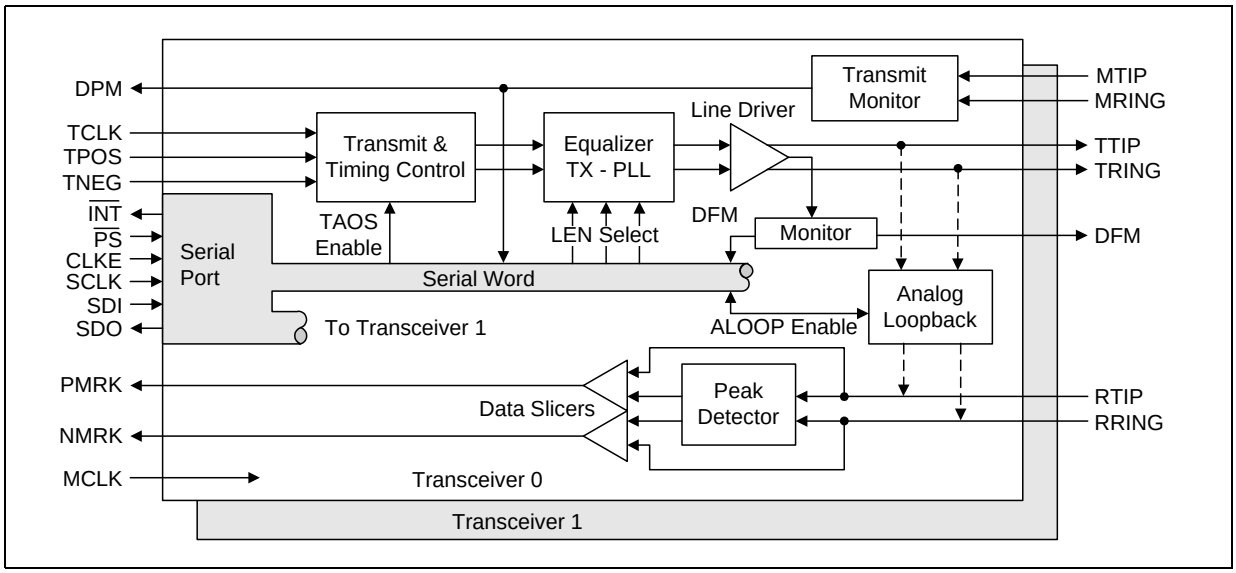
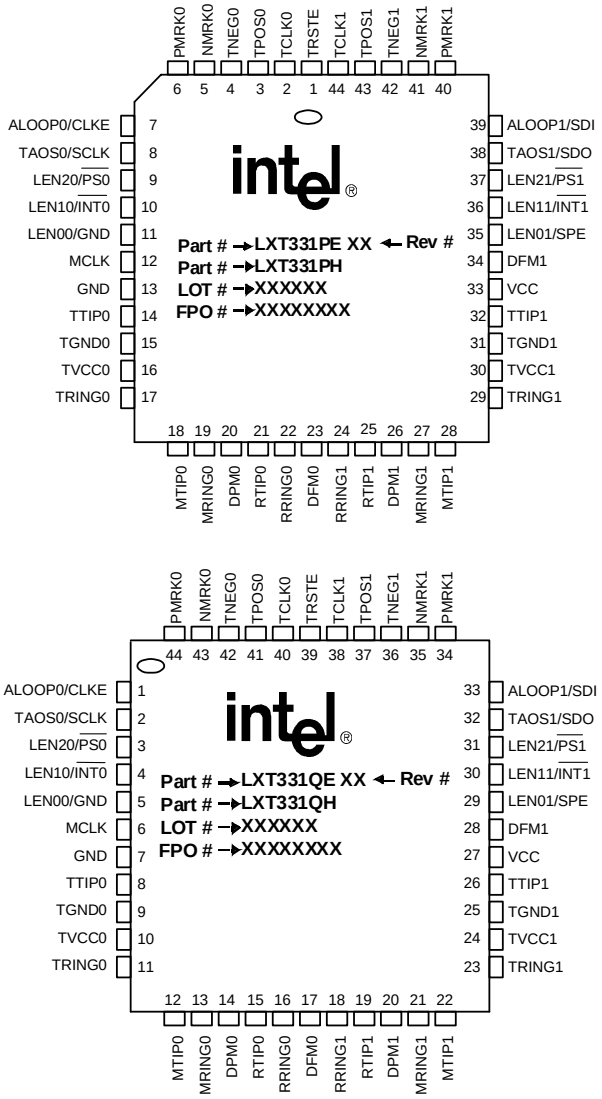
Figure 1. LXT331 Block Diagram



1.0 Pin Assignments & Signal Descriptions

Figure 2. LXT331 44 Pin Assignments and Markings



Package Topside Markings

Marking	Definition
Part #	Unique identifier for this product family.
Rev #	Identifies the particular silicon “stepping” — refer to the specification update for additional stepping information.
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

Table 1. Pin Descriptions

Pin PLCC	Pin QFP	Symbol	I/O[1]	Description
1	39	TRSTE	DI	**Tristate Enable**. Forces all output pins to tri-state when held High and forces chip into reset mode. Holds reset mode for 6 µs after TRSTE returns Low.
2	40	TCLK0	DI	**Transmit Clock — Port 0**. 1.544 MHz for T1, 2.048 MHz for E1. The transmit data inputs are sampled on the falling edge of TCLK. If TCLK is pulled Low, the transmit drivers are powered down and TTIP and TRING transmit outputs go to a high impedance state.
3 4	41 42	TPOS0 TNEG0	DI DI	**Transmit Positive and Negative Data, Port 0**. These pins drive the positive and negative sides of the bipolar input pair for port 0. Data to be transmitted onto the line is input at these pins.
5 6	43 44	NMRK0 PMRK0	DO DO	**Receive Negative and Positive Marks, Port 0**. These pins are the data outputs from port 0. A signal on NMRK corresponds to receipt of a negative pulse on RTIP/RRING. A signal on PMRK corresponds to receipt of a positive pulse on RTIP/RRING. NMRK/PMRK outputs are Return-to-Zero (RZ).
7	1	CLKE	DI	**Clock Edge Select *(Host mode)***. When CLKE is High, SDO is valid on the rising edge of SCLK.When CLKE is Low, SDO is valid on the falling edge of SCLK.
		ALOOP0	DI	**Analog Local Loopback Enable, Port 0 *(Hardware mode)***. When ALOOP is High, the RTIP/RRING inputs from the port 0 twisted-pair line are disconnected and the transmit data outputs (TTIP/TRING) are routed back into the receiver. For normal operation, hold ALOOP Low.
8	2	SCLK	DI	**Serial Clock *(Host mode)***. Shifts data into or out of the serial interface register of the selected port.
		TAOS0	DI	**Transmit All Ones Enable, Port 0 *(Hardware mode)***. When TAOS is High, the TPOS/TNEG input is ignored and the selected port transmits a stream of ones at the TCLK frequency. With no TCLK, the MCLK input becomes the transmit reference. For normal operation, hold TAOS Low. Refer to page 18.
9	3	$\overline{PS0}$	DI	**Port Select, Port 0 *(Host mode).*** Selects the serial interface registers of Port 0. For each read or write operation, $\overline{PS0}$ must transition from High to Low, and remain Low.
		LEN20	DI	**Line Length Equalizer 2, Port 0 *(Hardware mode)***. Determines the shape and amplitude of the transmit pulse. Refer to Table 2 on page 12
10	4	$\overline{INT0}$	DO	**Interrupt, Port 0 *(Host mode)***. Goes Low to flag the host processor that Port 0 has changed state. $\overline{INT0}$ is an open drain output and must be tied to VCC through a resistor.
		LEN10	DI	**Line Length Equalizer 1, Port 0 *(Hardware mode).*** Determines the shape and amplitude of the transmit pulse. Refer to Table 2 on page 12
11	5	GND	DI	**Unused (*Host mode*).** Must be tied to Ground.
		LEN00	DI	**Line Length Equalizer 0, Port 0 *(Hardware mode).*** Determines the shape and amplitude of the transmit pulse. Refer to Table 2 on page 12
12	6	MCLK	DI	**Master Clock.** 1.544 MHz for T1, 2.048 MHz for E1. Can be held Low if TCLK is present.
13	7	GND	S	**Ground.** Ground return for VCC power supply.
14	8	TTIP0	AO	**Transmit Tip, Port 0**. The TTIP and TRING pins are differential driver outputs designed to drive a 35-200 Ω load. Line matching resistors and transformers can be selected to give the desired pulse height.
15	9	TGND0	S	**Ground, Port 0 Transmit Driver.** Ground return for TVCC0 power supply.

1. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; S = Power Supply

Table 1. Pin Descriptions (Continued)

Pin PLCC	Pin QFP	Symbol	I/O[1]	Description
16	10	TVCC0	S	**+ 5 VDC Power Supply, Port 0 Transmit Driver.** TVCC0 must not vary from TVCC1 or VCC by more than ± 0.3 V.
17	11	TRING0	AO	**Transmit Ring, Port 0**. The TTIP and TRING pins are differential driver outputs designed to drive a 35-200 Ω load. Line matching resistors and transformers can be selected to give the desired pulse height.
18 19	12 13	MTIP0 MRING0	AI AI	**Monitor Tip and Ring, Port 0**. These pins monitor tip and ring outputs of either its own, or those of an adjacent LXT331 on the same board. If the application does not use this feature, tie one of these pins to a clock source and the other to a mid-level (referenced to the clock signal) voltage. The clock frequency can range from 100 kHz to the TCLK frequency.
20	14	DPM0	DO	**Driver Performance Monitor, Port 0**. Goes High to indicate the detection of 63 consecutive zeros. Goes Low upon the receipt of a one on the transmit monitor loop (MTIP/MRING).
21 22	15 16	RTIP0 RRING0	AI AI	**Receive Tip and Ring, Port 0**. RTIP and RRING comprise the receive line interface. This input pair should be connected to the line through a 1:1 transformer.
23	17	DFM0	DO	**Driver Fail Monitor, Port 0**. Goes High to indicate a driver output short condition.
24 25	18 19	RRING1 RTIP1	AI AI	**Receive Tip and Ring, Port 1**. Refer to RRING0 and RTIP0 pins.
26	20	DPM1	DO	**Driver Performance Monitor**, **Port 1**. Refer to DPM0 pin.
27 28	21 22	MRING1 MTIP0	AI	**Monitor Tip and Ring, Port 1**. Refer to MRING0 and MTIP0 pins.
29	23	TRING1	AO	**Transmit Ring, Port 1**. Refer to TRING0 pin.
30	24	TVCC1	S	**+ 5 VDC Power Supply, Port 1 Transmit Driver.** TVCC1 must not deviate from TVCC0 or VCC by more than ± 0.3 V.
31	25	TGND1	S	**Ground, Port 1 Transmit Driver.** Ground return for TVCC1 power supply.
32	26	TTIP1	AO	**Transmit Tip, Port 1**. Refer to TTIP0 pin.
33	27	VCC	S	+ 5 VDC Power Supply Input for All Circuits Except Transmit Drivers.
34	28	DFM1	DO	**Driver Fail Monitor, Port 1**. Refer to DFM0 pin.
35	29	SPE	DI	**Serial Port Enable *(Host mode)***. SPE must be clocked with MCLK, TCLK0 or TCLK1 to enable Host mode control through the serial port.
		LEN01	DI	**Line Length Equalizer 0, Port 1 *(Hardware mode).*** Determines the shape and amplitude of the transmit pulse. Refer to Table 2 on page 12
36	30	$\overline{\text{INT1}}$	DO	**Interrupt, Port 1 *(Host mode).*** Refer to $\overline{\text{INT0}}$ pin.
		LEN11	DI	**Line Length Equalizer 1, Port 1 *(Hardware mode).*** Determines the shape and amplitude of the transmit pulse. Refer to Table 2 on page 12
37	31	$\overline{\text{PS1}}$	DI	**Port Select, Port 1 *(Host mode)***. Refer to $\overline{\text{PS0}}$ pin.
		LEN21	DI	**Line Length Equalizer 2, Port 1 *(Hardware mode).*** Determines the shape and amplitude of the transmit pulse. Refer to Table 2 on page 12
38	32	SDO	DO	**Serial Data Output *(Host mode).*** Read data from the LXT331 registers are output on this pin. When CLKE is High, SDO is valid on the rising edge of SCLK. When CLKE is Low, SDO is valid on the falling edge of SCLK.
		TAOS1	DI	**Transmit All Ones Enable, Port 1 *(Hardware mode).*** Refer to TAOS0 pin.

1. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; S = Power Supply

Table 1. Pin Descriptions (Continued)

Pin PLCC	Pin QFP	Symbol	I/O[1]	Description
39	33	SDI	DI	**Serial Data Input *(Host mode)*.** Write data to the LXT331 registers are input on this pin. SDI is sampled on the rising edge of SCLK.
		ALOOP1	DI	**Analog Local Loopback Enable, Port 1 *(Hardware mode)*.** Refer to pin ALOOP0.
40 41	34 35	PMRK1 NMRK1	DO DO	**Receive Negative and Positive Marks, Port 1**. Refer to PMRK0 and NMRK0 pins.
42 43	36 37	TNEG1 TPOS1	DI DI	**Transmit Negative and Positive Data, Port 1**. Refer to TNEG0 and TPOS0 pins.
44	38	TCLK1	DI	**Transmit Clock, Port 1**. Refer to TCLK0 pin.

1. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; S = Power Supply

2.0 Functional Description

The LXT331 is a Dual Line Interface Unit (DLIU), which contains two ports. Refer to the simplified block diagram on page 1. The DLIU is designed for both 1.544 Mbps (DSX-1) and 2.048 Mbps (E1) applications. Both ports operate at the same frequency, which is determined by the TCLK input.

Each port's front end interfaces with two lines, one line for transmit, one line for receive. These two lines comprise a digital data loop for full-duplex transmission. Each port's back-end interfaces with a layer processor through bipolar data I/O channels.

The DLIU may either be controlled by a microprocessor via the serial port (Host mode), or by hardwired pins for stand-alone operation (Hardware mode).

2.1 Receiver

The two receivers in the LXT331 DLIU are identical. The following paragraphs describe the operation of a single receiver.

The input signal is received via a 1:1 transformer. The receiver requires fully differential inputs which are internally self-biased into 2.5 V. Recovered data is output at PMRK and NMRK. Refer to Test Specifications for receiver timing.

The receive signal is processed through an adaptive peak detector and data slicers. The peak detector samples the received signal and determines its maximum value. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For DSX-1 applications (line length inputs LEN0-LEN2 ≠ 000 or 001), the threshold is set to 70% (typical) of the peak value.

This threshold is maintained above the specified level for up to 15 successive zeros over the range of specified operating conditions. For E1 applications (LEN0-LEN2 = 000 or 001) the threshold is 50% (typical).

The receiver is capable of accurately recovering signals with up to +13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Maximum line length is 1500 feet of ABAM cable (approximately 6 dB of attenuation). Regardless of received signal level, the peak detectors are held above a minimum level of 0.3 V (typical) to provide immunity from impulsive noise. Built in pulse stretching circuitry maintains a minimum positive and negative mark pulse width (see Table 13 and Figure 15 on page 28).

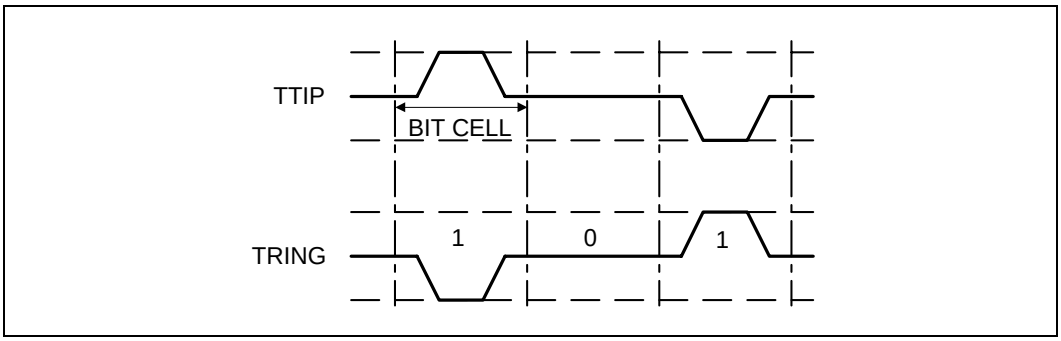
2.2 Transmitter

The two transmitters in the LXT331 DLIU are identical. The following paragraphs describe the operation of a single transmitter.

Transmit data is clocked serially into the device at TPOS/TNEG. Input synchronization is supplied by the transmit clock (TCLK). The TPOS/TNEG inputs are sampled on the falling edge of TCLK. If TCLK is held Low, the transmitter remains powered down and the TTIP/TRING outputs are held in a high-Z state (except in TAOS mode if MCLK is available). Each output driver is provided with

a separate power supply pin (TVCC0 or TVCC1). Current limiters on the output drivers provide short circuit protection. Refer to Test Specifications for TCLK timing characteristics. As shown in Figure 3, the LXT331 encodes transmit data using 50% Alternate Mark Inversion (AMI) line code.

Figure 3. 50% AMI Coding



2.2.1 Pulse Shape

The transmitted pulse shape is determined by Line Length equalizer control signals LEN0 through LEN2. Equalizer codes are hard-wired in Hardware mode as shown in Table 2. In Host mode, the LEN control codes are input through the serial interface. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. The line driver provides a constant Low output impedance of < 3 Ω (typical) regardless of whether it is driving marks or spaces or during transitions. This well-controlled impedance provides excellent return loss when used with external precision resistors (±1% accuracy). See Table 9 and Table 10 for recommended transformer specifications, turns ratios, series resistor (Rt) values, and typical return losses for various LEN codes. To minimize power consumption the DC blocking capacitor and the LXT331 can be connected directly to a 1:1.15 transformer without series resistors.

Pulses can be shaped for either 1.544 or 2.048 Mbps applications. 1.544 Mbps pulses for DSX-1 applications can be programmed to match line lengths from 0 to 655 feet of 22 AWG ABAM cable. A combination of 9.1 Ω resistors and a 1:2.3 transformer is recommended for maximum transmit return loss in DSX-1 applications. The LXT331 also matches FCC pulse mask specifications for CSU applications.

The LXT331 produces 2.048 Mbps pulses for both 75 Ω coaxial (2.37 V) or 120 Ω shielded twisted-pair (3.0 V) lines through an output transformer with a 1:2 turns ratio.

Refer to the “Application Information” on page 20 for details on interface circuitry.

2.2.2 Driver Performance Monitor

The LXT331 incorporates a Driver Performance Monitor (DPM) as shown in Figure 4 on page 13. The DPM output goes High on receipt of 63 consecutive zeros (at MTIP and MRING) and returns Low on receipt of a transition. A reset command also drives the output signal Low.

The LXT331 uses its MTIP and MRING pins to monitor its own TTIP and TRING outputs or those of an adjacent chip. Mark detection involves two criteria:

1. Voltage threshold: a pulse must trip a threshold voltage above or below (depending on its polarity) the input bias voltage level. The LXT331 bias voltage is 2.5 V and the threshold for a mark is 2.5 ± 0.79 V.

2. Pulse width: the monitor distinguishes between marks and noise pulses by the pulse width. LXT331 requires a mark pulse to be at least 120 ns wide (typical).

As shown in Figure 4 on page 13, there are two type of marks: “A” and “B”. C1 and C2 detect “A” marks while the AND gate (A1) ensures that both mark signals are present at the same time. If the pulse widths are adequate, i.e. both a positive mark on MTIP and a negative mark on MRING, the A1 output goes High. Likewise C3 and C4 detect “B” marks. If the pulse meets the minimum width requirement, the AND gate (A2) output goes High when there are both a negative mark on MTIP and a positive mark on MRING. The OR gate (O1) passes the mark, as the signal “zero”, on to the clock/counter circuit which controls the DPM output.

A latch samples the counter and goes High if the DPM circuit sees 63 consecutive zeros. Any mark resets the counter. The DPM signal goes High after the 63rd zero.

Table 2. Equalizer Control Inputs - Hardware Mode[1]

LEN2	LEN1	LEN0	Line Length[2]	Cable Loss[3]	Application	Frequency
Low	High	High	0 - 133 ft ABAM	0.6 dB	DSX-1	1.544 MHz
High	Low	Low	133-266 ft ABAM	1.2 dB		
High	Low	High	266-399 ft ABAM	1.8 dB		
High	High	Low	399-533 ft ABAM	2.4 dB		
High	High	High	533-655 ft ABAM	3.0 dB		
Low	Low	Low	ITU Recommendation G.703		E1 - Coax (75 Ω)	2.048 MHz
Low	Low	High			E1 - Twisted-pair (120 Ω)	
Low	High	Low	FCC Part 68, Option A		CSU	1.544 MHz

1. LEN0-2 inputs are shown as High or Low for Hardware mode. For Host mode serial inputs, High = 1 and Low = 0.
2. Line length from LXT331 to DSX-1 cross-connect point.
3. Maximum cable loss at 772 kHz.

2.2.3 Driver Failure Monitor

The transceiver incorporates an internal Driver Failure Monitor (DFM) that observes TTIP and TRING. Driver failure is detected with a capacitor that is charged as a function of driver output current, and discharged as a measure of the maximum allowable current. Shorted lines draw excess current, overcharging the cap. When the capacitor charge deviates outside the nominal charge window, a driver failure is reported. In Host mode the DFM bit is set in the serial word. In both Hardware and Host modes the DFM pin goes High. During a long string of spaces, a short-induced overcharge eventually bleeds off, clearing the DFM flag.

2.3 Control Modes

The LXT331 transceiver operates in either standalone Hardware mode (default) or Host mode. In Host mode a microprocessor controls the LXT331 via the serial I/O port (SIO) which provides common access to both LIUs. In Hardware mode, the transceiver is controlled through individual pins; a microprocessor is not required.

2.3.1 Host Mode Control

Host mode is selected when a clock is applied to the SPE pin. Each of the two LIUs contains a pair of data registers, one for command inputs and one for status outputs. An SIO transaction is initiated by a falling pulse on one of the two Port Select pins, $\overline{PS0}$ or $\overline{PS1}$. Only one LIU can be selected at a time. A High-to-Low transition on PS*n* is required for each subsequent access to the Host mode registers. If both $\overline{PS0}$ and $\overline{PS1}$ are active simultaneously, Port 0 has priority over Port1.

The LIU addressed by the $\overline{PSn}$ pulse responds by writing the incoming serial word (at the SDI pin) into its command register. Figure 5 on page 15 shows an SIO write operation. The 16-bit serial word consists of an 8-bit Command/Address byte and an 8-bit Data byte. If the command word contains a read request, the addressed LIU subsequently outputs the contents of its status register onto the SDO pin.

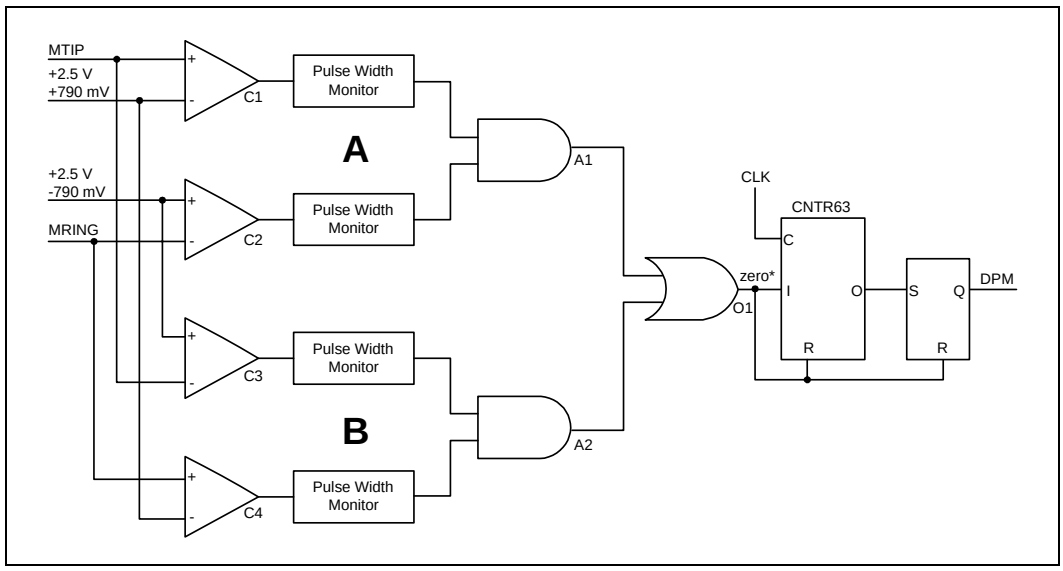
Figure 6 on page 16 shows an SIO read operation. The Clock Edge (CLKE) signal determines when the SDO output is valid (relative to SCLK) as follows:

If CLKE = High, SDO is valid on the rising edge of SCLK. If CLKE = Low, SDO is valid on the falling edge of SCLK. Refer to Test Specifications for SIO timing.

2.3.1.1 Serial Input Word

Figure 5 on page 15 shows the Serial Input data structure. The LXT331 is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. Bit 1 of the serial Address/ Command byte provides Read/Write (R/W) control when the chip is accessed. The R/W bit is set to logic 1 to read the data output byte from the chip, and set to logic 0 to write the input data byte to the chip.

Figure 4. LXT331 Driver Performance Monitor



The second 8 bits of a write operation (the Data Input byte) clear the Driver Performance Monitor (DPM) and Driver Fail Monitor (DFM) interrupts, reset the chip, and control diagnostic modes. The first and second bits (D0-1) clear and/or mask the DPM and DFM interrupts, and the last 3 bits (D5-7) control operating modes (normal and diagnostic) and chip reset. Refer to Table 3 for details on bits D5-7.

Table 3. SIO Input Bit Settings (See **Figure 5**)

Mode	TST bit D5	ALOOP bit D6	TAOS bit D7
Analog Loopback	0	1	0
Transmit All Ones	0	X	1
Reset/High Z	1	1	0

2.3.1.2 Serial Output Word

Figure 6 shows the Serial Output data structure. SDO is high impedance when SDI receives an Address/Command byte. If SDI receives a write command (R/$\overline{W}$ = 0), SDO remains in high impedance. If the command is a read (R/$\overline{W}$ = 1), then SDO becomes active after the last Command/Address bit (A6) and remains active for eight SCLK cycles. Typically the first bit out of SDO changes the state of SDO from high Z to a Low/High. This occurs approximately 100 ns after the eighth following edge of SCLK.

The output data byte reports DPM and DFM conditions, equalizer settings, and operating modes (normal or diagnostic). The first 5 bits (D0-4) report DPM and DFM status and the Line Length Equalizer settings. The last 3 bits (D5-7) report operating modes and interrupt status as defined in Table 4.

If the $\overline{INT}$ line for the respective port is High (no interrupt is pending), bits D5-7 report the operating modes listed in Table 4. If the $\overline{INT}$ line for the respective port is Low, the interrupt status overrides all other reports and bits D5-7 reflect the interrupt status as listed in Table 4.

2.3.1.3 Interrupt Handling

The Host mode provides two latched Interrupt output pins, $\overline{INT0}$ and $\overline{INT1}$, one for each LIU. An interrupt is triggered by a change in the DPM or DFM bit (D0=DPM, D1=DFM). As shown in Figure 7 on page 17, either or both interrupt generators can be masked by writing a 1 to the corresponding bit (D0 or D1) of the input data byte. When an interrupt occurrs, the $\overline{INT}$ output pin is pulled Low. The output stage of each $\overline{INT}$ pin consists of a pull-down device; thus an external pull-up resistor is required. Clear the interrupts as follows:

1. If one or both interrupt bits (DPM or DFM of the output data byte) are High, write a 1 to the corresponding bit of the input data byte to clear the interrupt. Leave a 1 in either bit position to effectively mask that interrupt. To re-enable the interrupt capability, reset either D0 or D1 or both to 0.
2. If neither DPM nor DFM is high, reset the chip to clear the interrupt. To reset the chip, set data input bits D5 and D6 = 1, and D7 = 0.

2.3.2 Hardware Mode Control

Hardware control is the default operating mode. The LXT331 operates in Hardware mode unless a clock is applied to the LEN21/SPE pin. In Hardware mode, the SIO pins are re-mapped to provide control functions. In Hardware mode, the PMRK/NMRK outputs are valid on the rising edge of RCLK.

Table 4. LXT331 Serial Data Output Bit Coding

Bit D5	Bit D6	Bit D7	Operating Modes
0	0	0	Reset has occurred, or no program input (i.e. normal operation).
0	0	1	TAOS active
0	1	0	ALOOP active
0	1	1	TAOS and ALOOP active
Bit D5	**Bit D6**	**Bit D7**	**Interrupt Status**
1	0	1	DFM has changed state since the last Clear DFM occurred
1	1	0	DPM has changed state since the last Clear DPM occurred
1	1	1	DPM and DFM have changed state since the last Clear DPM and DMF occurred

Figure 5. LXT331 SIO Write Operations

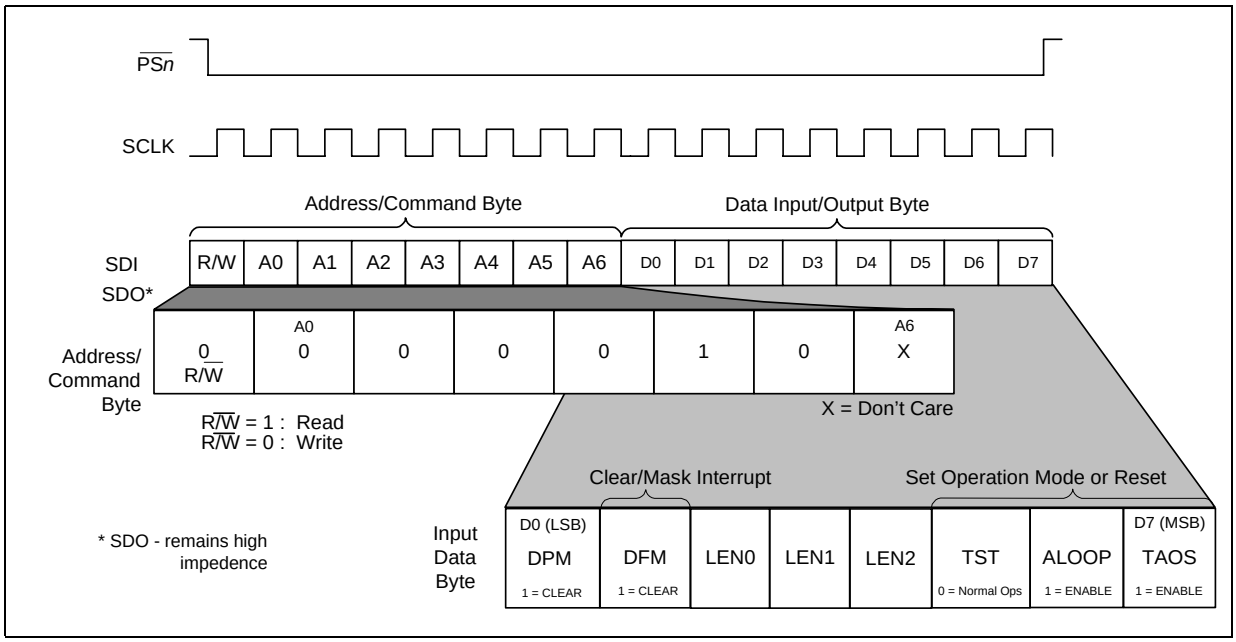


Figure 6. LXT331 SIO Read Operation

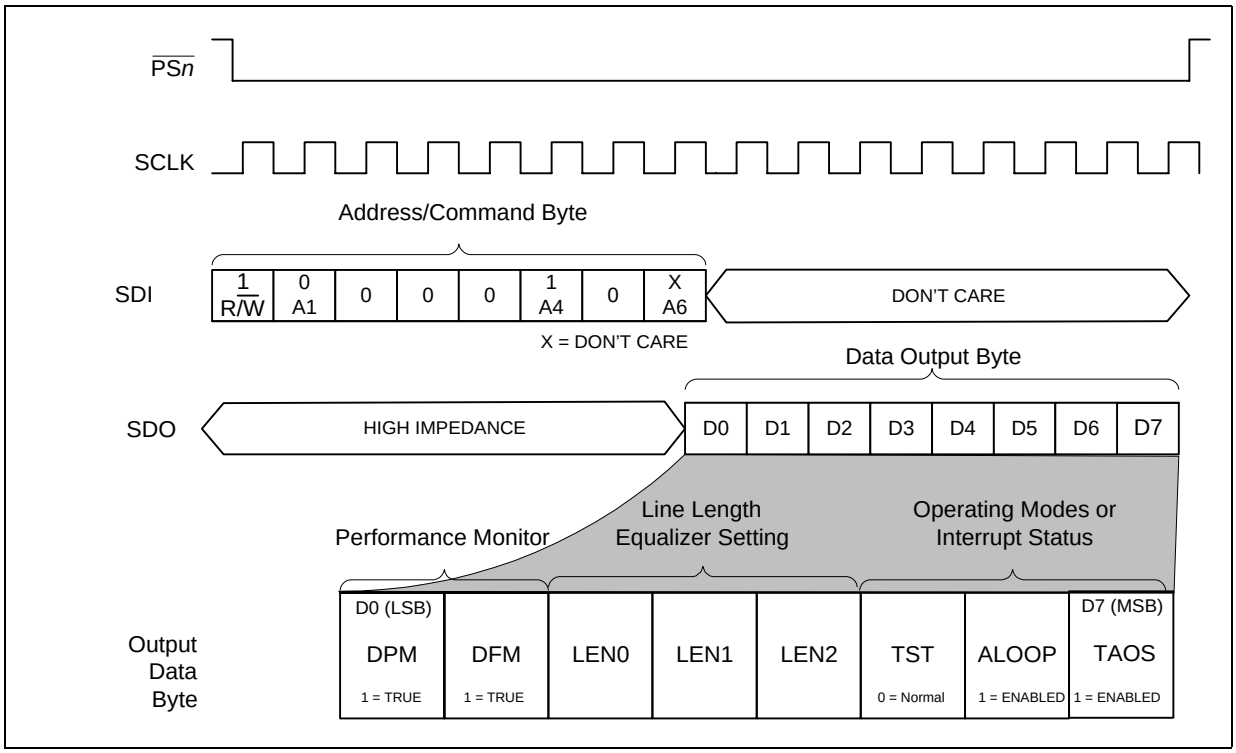
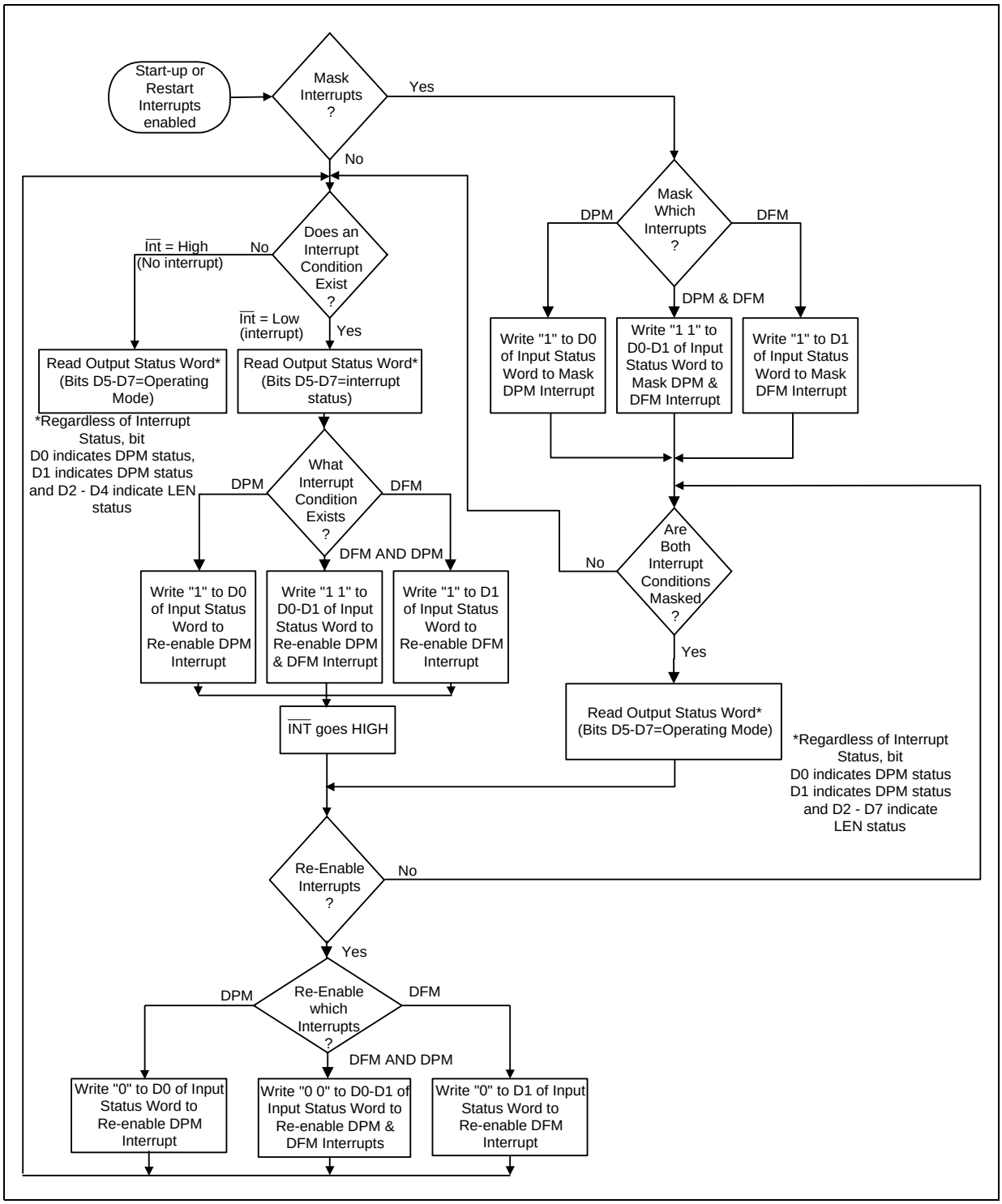


Figure 7. LXT331 Interrupt Handling



2.4 Diagnostic Mode Operation

The LXT331 offers two diagnostic modes. Analog Loopback (ALOOP) and Transmit All Ones (TAOS) are available under both Host and Hardware control modes.

In Host mode, diagnostic modes are selected by writing the appropriate SIO bits. In Hardware mode, diagnostic modes are selected by a combination of pin settings. The pins must be held at the specified levels for a minimum of 20 ns (typically). Table 5 lists Hardware Mode control settings for the various diagnostic modes.

Table 5. Hardware Mode Diagnostic Selection

Mode	LXT331 Pin		
	TRSTE	ALOOP	TAOS
Analog Loopback	L	H	L
Transmit All Ones	L	X	H
Reset/High Z	H	X	X

Transmit All Ones. See Figure 8. Transmit All Ones (TAOS) is selected when TAOS = 1. In TAOS mode the TPOS and TNEG inputs are ignored, but the transmitter remains locked to the TCLK input. When TAOS is selected, the transceiver transmits a continuous stream of 1s at the TCLK frequency. If TCLK is not supplied, MCLK is used as the transmit reference. TAOS and Analog Loopback can be selected simultaneously as shown in Figure 9.

Analog Loopback. See Figure 10. Analog Loopback (ALOOP) is selected when ALOOP = 1. In ALOOP mode the receive line input (RTIP/RRING) is blocked. The transmit outputs (TTIP and TRING) are looped back through the receiver input and output at PMRK and NMRK. The transmitter circuits are unaffected by ALOOP. Transmitting onto an improperly terminated line may produce unexpected pulse widths at PMRK and NMRK.

Reset / Tri-State. By holding the TRSTE pin High for at least 200 ns, all output drivers (both digital and analog) go to the high Z state and the chip logic is reset. The reset/high Z state is maintained for 6 µs after TRSTE returns Low.

Figure 8. Transmit All Ones Data Path

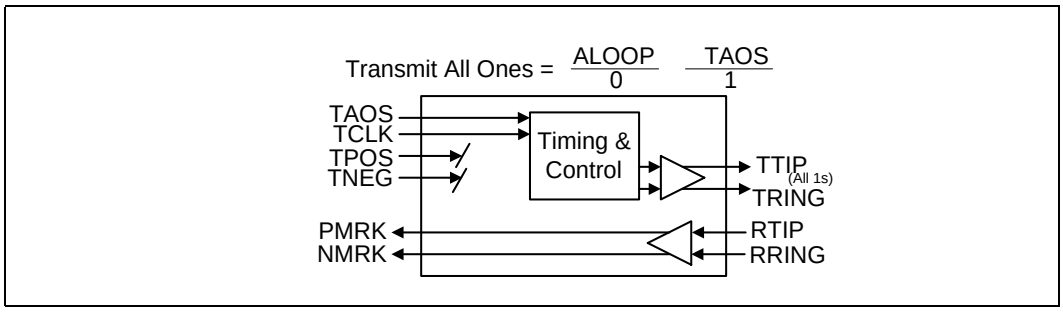


Figure 9. TAOS with Analog Loopback

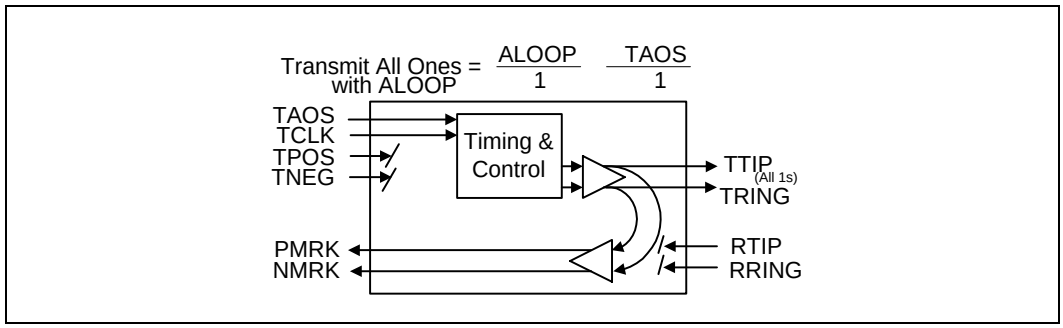
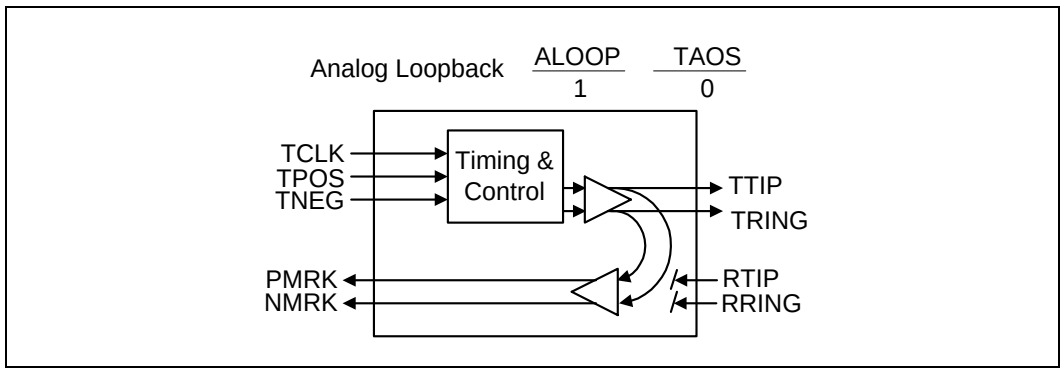


Figure 10. Analog Loopback



2.5 Initialization & Reset

Upon initial power up, the transceiver is held static until the power supply reaches approximately 3 V. Upon crossing this threshold, the device clears all internal registers. TCLK is the transmit reference, and MCLK is the bias reference. The PLLs are continuously calibrated.

The transceiver can be reset from the Host or Hardware mode. In Host mode, reset is commanded by writing 1s to TST and ALOOP, and a 0 to TAOS (bits D5, D6 and D7, respectively, of the SIO input data byte). In either mode, reset is commanded by holding the TRSTE pin High for approximately 200 ns. All output signals are tri-stated at this time. In Hardware mode, the falling edge of TRSTE initiates reset for the entire chip. Host mode resets the selected port SIO registers to 0. Reset is not generally required for the port to be operational.

3.0 Application Information

3.1 Power Requirements

The LXT331 is a low-power CMOS device. Three separate power pins are provided: one pin for each port's transmitter circuits (TVCC0 and TVCC1) and a pin for all remaining circuits (VCC). The LXT331 typically operates from a single +5 V power supply that is tied to all three VCC inputs. Note that all power pins must be within ±0.3 V of each other, and decoupled to their respective grounds separately. Isolation between the transmit and receive circuits is provided internally. During normal operation or analog loopback, the transmitter powers down when TCLK is not supplied.

3.1.1 Line Interface Requirements

Table 6 lists transformer values for 1.544 Mbps and 2.048 Mbps applications. Table 7 shows combinations of transformers, series resistors and the LEN control settings that produce a variety of return loss values.

Table 6. Recommended Transmit Transformer Values

Parameter	Value
Turns Ratio (T1)	1:2/1:1.15/1:2.3 (Tx)/ 1:1 (Rx)
Turns Ratio (E1)	1:2 (Tx) / 1: 1 (Rx)
Primary Inductance	1.2 mH minimum
Leakage Inductance	0.5 µH maximum
Interwinding Capacitance	25 pF maximum
DC Resistance (Primary)	1 Ω maximum
ET (Breakdown Voltage)	1 kV minimum

Table 7. Transmit Transformer Combinations

LEN	Xfmr Ratio[1]	Rt Value[2]	Rtn Loss[3]
For T1/DSX-1 100 Ω Twisted-Pair Applications:			
011-111	1:2	Rt = 9.1 Ω	14dB
011-111	1:2.3	Rt = 9.1 Ω	18dB
011-011	1:1.15	Rt = 0 Ω	1dB
For E1 120 Ω Twisted-Pair Applications:			
001	1:2	Rt = 15 Ω	18dB
000	1:2	Rt = 9.1 Ω	10dB

1. Transformer turns ratio accuracy is ± 2%.
2. Rt values are ± 1%.
3. Typical return loss, 51kHz - 3.072 MHz band, with a capacitor in parallel with the primary side of the transformer.

Table 7. Transmit Transformer Combinations

LEN	Xfmr Ratio[1]	Rt Value[2]	Rtn Loss[3]
For T1/DSX-1 100 Ω Twisted-Pair Applications:			
For E1 75 Ω Coaxial Applications:			
001	1:2	Rt = 14.3 Ω	10dB
000	1:2	Rt = 9.1 Ω	18dB

1. Transformer turns ratio accuracy is ± 2%.
2. Rt values are ± 1%.
3. Typical return loss, 51kHz - 3.072 MHz band, with a capacitor in parallel with the primary side of the transformer.

3.2 Line Protection

On the receive side, 1 kΩ series resistors protect the receiver against current surges coupled into the device. Due to the high receiver impedance (40 kΩ typical) the resistors do not affect the receiver sensitivity. On the transmit side, Schottky diodes D1-D4 protect the output driver. While not mandatory for normal operation, these protection elements are strongly recommended to improve the design's robustness.

3.2.1 1.544 Mbps T1 Applications

Figure 12 on page 23 shows a typical host mode T1 application. The serial interface pins are grouped at the top. Host mode is selected by applying clock (MCLK or TCLK) to the SPE pin.

When the TRSTE pin (shown at lower left) is pulled Low, the LXT331 operates normally. Pulling this pin High causes all outputs to go to a high impedance state.

Figure 12 on page 23 also shows a dual framer that recovers the clock from PMRK and NMRK.

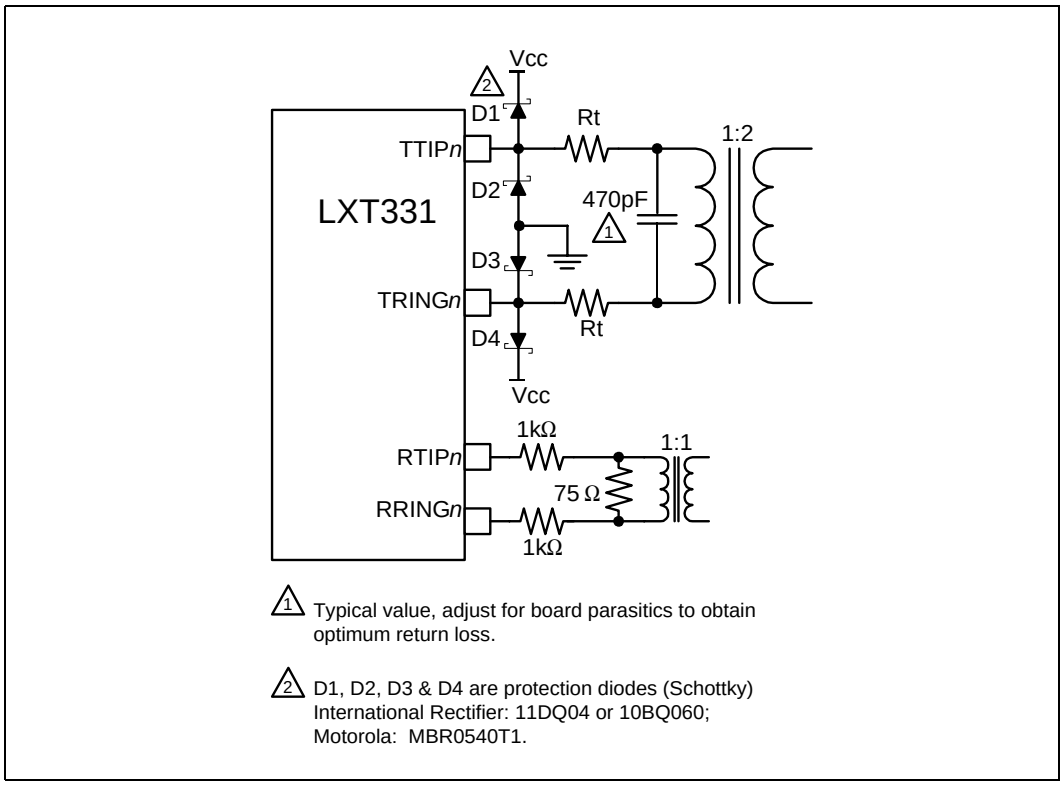
The DFM and DPM monitor output signals are available to drive optional external circuits. The transmitter power supply pins are tied to the common +5 VDC bus. Note that 68 µF decoupling capacitors are installed. The power supply for the remaining (non-driver) circuitry includes 1.0 µF and 0.1 µF decoupling capacitors. Note that all VCC pins must be within ±0.3 V of each other.

The line interface circuitry is identical for both LIU ports. The precision resistors, in line with the transmit transformer, provide optimal return loss. The recommended transformer/resistor combinations (on the transmit side) are listed in Table 7. 1:1 transformers are used on the receive side.

3.2.2 2.048 Mbps E1 Coax Applications

Figure 11 shows the line interface for a typical 2.048 Mbps E1/CEPT coaxial (75 Ω) application. The LEN code should be set to 000 for coax. With 9.1 Ω Rt resistors in line with 1:2 output transformers, the LXT331 produces 2.37 V peak pulses as required for coax applications.

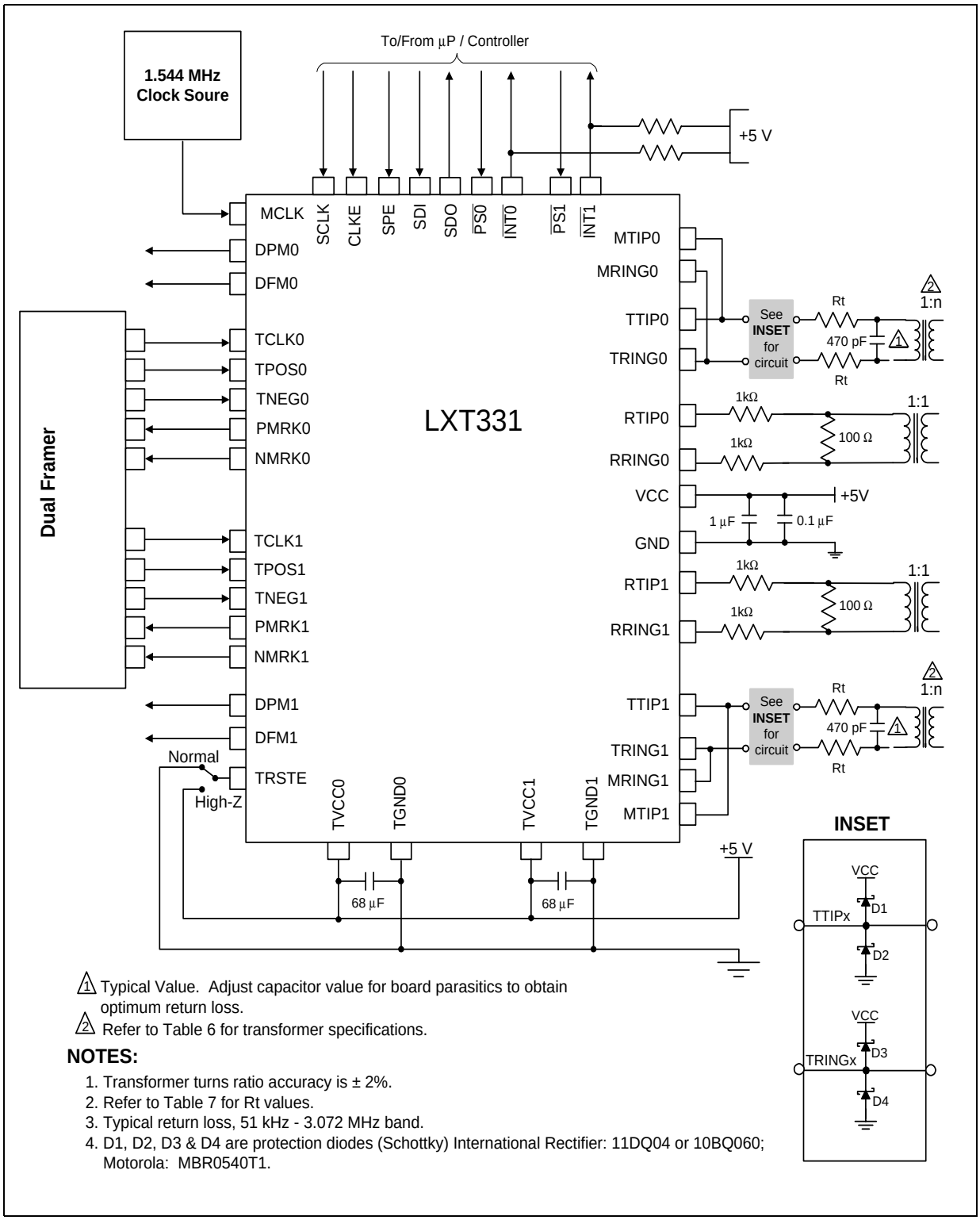
Figure 11. Line Interface for E1 Coax



3.2.3 2.048 Mbps E1 Twisted-Pair Applications

Figure 13 shows a typical 2.048 Mbps E1 twisted-pair (120 Ω) application. The line length equalizers are controlled by the hardwired LEN inputs. With the LEN code set to 001 and 15 Ω Rt resistors in line with the 1:2 output transformers, the LXT331 produces the 3.0 V peak pulses required for twisted-pair applications.

Figure 12. Typical LXT331 T1 Application (Host Control Mode, Bipolar I/O)



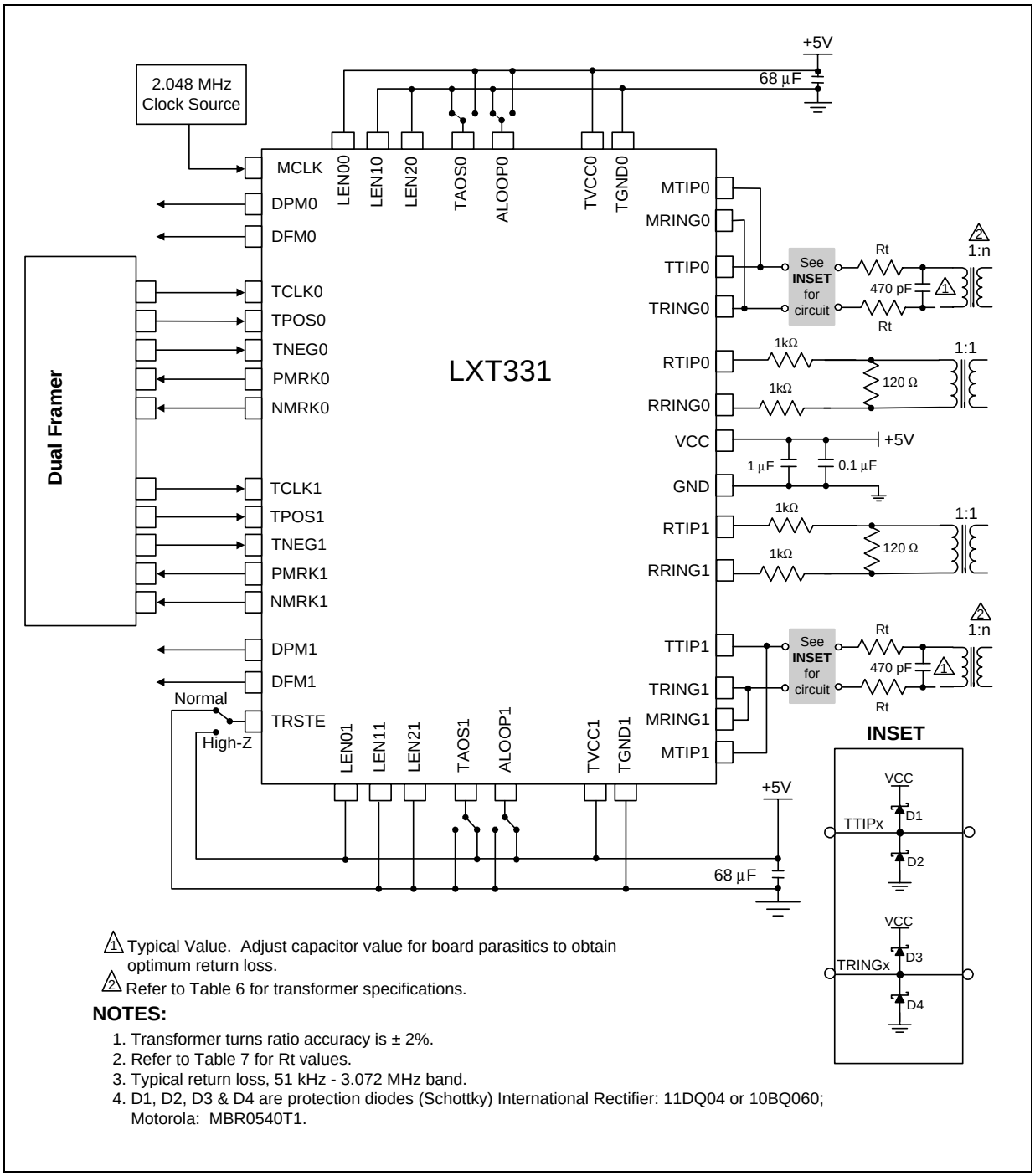
1 Typical Value. Adjust capacitor value for board parasitics to obtain optimum return loss.

2 Refer to Table 6 for transformer specifications.

NOTES:

1. Transformer turns ratio accuracy is ± 2%.
2. Refer to Table 7 for Rt values.
3. Typical return loss, 51 kHz - 3.072 MHz band.
4. D1, D2, D3 & D4 are protection diodes (Schottky) International Rectifier: 11DQ04 or 10BQ060; Motorola: MBR0540T1.

Figure 13. Typical LXT331 E1 120 Ω Twisted Pair Application (Hardware Control Mode)



1 Typical Value. Adjust capacitor value for board parasitics to obtain optimum return loss.

2 Refer to Table 6 for transformer specifications.

NOTES:

1. Transformer turns ratio accuracy is ± 2%.
2. Refer to Table 7 for Rt values.
3. Typical return loss, 51 kHz - 3.072 MHz band.
4. D1, D2, D3 & D4 are protection diodes (Schottky) International Rectifier: 11DQ04 or 10BQ060; Motorola: MBR0540T1.

4.0 Test Specifications

Note: The minimum and maximum values in Table 8 through Table 14 and Figure 14 through Figure 17 represent the performance specifications of the LXT331 and are guaranteed by test, except where noted by design.

Table 8. Absolute Maximum Ratings

Parameter	Sym	Min	Max	Unit
DC supply (referenced to GND)	VCC, TVCC0, TVCC1	-0.3	6.0	V
Input voltage, any pin [1]	VIN	GND - 0.3	Vcc + 0.3	V
Input current, any pin [2]	IIN	-10	10	mA
Storage temperature	TST	-65	150	°C

Caution: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed or implied at these extremes.

1. Excluding RTIP and RRING which must stay within - 6 V to VCC + 0.3 V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. TTIP0 & 1, TRING0 & 1, VCC, TVCC0 & 1 and TGND0 & 1 can withstand continuous current of 100 mA.

Table 9. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical[1]	Maximum	Unit
DC supply [2]	VCC, TVCC0, TVCC1	4.75	5.0	5.25	V
LXT331PE & QE ambient operating temperature	TA	-40	25	85	°C
LXT331PH & QH ambient operating temperature	TA	-5	25	85	°C

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Variation between TVCC0, TVCC1 and VCC must be less than 0.3 V.

Table 10. Electrical Characteristics (Over Recommended Operating Range)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Total power dissipation - T1 [2] (Maximum line length, 75 Ω load)	PP	-	550	680	mW	-40 to +85 °C
	PD	-	550	650	mW	0 to +85 °C
Total power dissipation - T1 [3] (Maximum line length, 43 Ω load)	PP	-	775	1000	mW	-40 to +85 °C
	PD	-	775	980	mW	0 to +85 °C
Total power dissipation - E1 [2]	PD	-	380	520	mW	100% ones density

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. 100% 1s density and maximum line length. Driving a line load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails. Digital outputs are driving a 50 pF capacitive load.
3. 100% 1s density and maximum line length. Driving a line load (corresponding to Rt value of 9.1 Ω and 1:2 transformer ratio) over operating range. include device and load. Digital input levels are within 10% of the supply rails. Digital outputs are driving a 50 pF capacitive load.
4. Functionality of pins depends on mode.
5. Output drivers will output CMOS logic levels into CMOS loads.
6. All digital input pins.
7. For MTIP0, MRING0, MTIP1 AND MRING1.

Table 10. Electrical Characteristics (Over Recommended Operating Range)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
High level input voltage [4,5]	VIH	2.0	-	-	V	
Low level input voltage [4,5]	VIL	-	-	0.8	V	
High level output voltage [4,5]	VOH	2.4	-	-	V	IOUT = - 400 µA
Low level output voltage [4,5]	VoL	-	-	0.4	V	IOUT = 1.6 mA
Input leakage current [6]	ILLD	0	-	± 10	µA	
Input leakage current [7]	ILLM	0	-	± 50	µA	
Three-state leakage current [4]	ISL	-	-	± 10	µA	
TTIP/TRING leakage current	ITR	-	-	1.2	mA	In power down and tri-state

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. 100% 1s density and maximum line length. Driving a line load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails. Digital outputs are driving a 50 pF capacitive load.
3. 100% 1s density and maximum line length. Driving a line load (corresponding to Rt value of 9.1 Ω and 1:2 transformer ratio) over operating range. include device and load. Digital input levels are within 10% of the supply rails. Digital outputs are driving a 50 pF capacitive load.
4. Functionality of pins depends on mode.
5. Output drivers will output CMOS logic levels into CMOS loads.
6. All digital input pins.
7. For MTIP0, MRING0, MTIP1 AND MRING1.

Table 11. Analog Specifications (Over Recommended Operating Range)

Parameter		Min	Typ[1]	Max	Unit	Test Conditions
AMI output pulse amplitudes	DSX-1	2.4	3.0	3.6	V	measured at the DSX
	E1 (120 Ω)	2.7	3.0	3.3	V	measured at line side
	E1 (75 Ω)	2.13	2.37	2.61	V	measured at line side
Transmit amplitude variation with supply [3]		-	1	2.5	%	
Recommended output load at TTIP and TRING		-	75	-	Ω	
Driver output impedance [3]		-	3	10	Ω	@ 772 kHz
Jitter added by the transmitter [2]	10 Hz - 8kHz [3]	-	0.005	0.01	UI	T1 Jitter Bands
	8 kHz - 40 kHz [3]	-	0.015	0.025	UI	
	10 Hz - 40 Hz [3]	-	0.02	0.025	UI	
	Broad band	-	0.03	0.05	UI	
Jitter added by the transmitter [2]	20 Hz - 100 kHz	-	-	0.05	UI	E1 Jitter Band
Output power levels [3] DSI 2 kHz BW	@ 772 kHz	12.6	-	17.9	dBm	
	@ 1544 kHz	-29	-	-	dB	
Positive-to-negative pulse imbalance		-	-	0.5	dB	
Differential input impedance		-	40	-	kΩ	
Sensitivity below DSX (0 dB = 2.4 V) (max 6 dB cable attenuation)		13.6	-	-	dB	
		500	-	-	mV	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Input signal at TCLK is jitter-free.
3. Not production tested, but guaranteed by design and other correlation methods.

Table 11. Analog Specifications (Over Recommended Operating Range) (Continued)

Parameter		Min	Typ[1]	Max	Unit	Test Conditions
Peak detector squelch level		-	226	-	mV	
Data decision threshold	DSX-1	63	70	77	% peak	
	E1	43	50	57	% peak	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Input signal at TCLK is jitter-free.
3. Not production tested, but guaranteed by design and other correlation methods.

Table 12. LXT331 Master Clock and Transmit Timing Characteristics (See **Figure 14**)

Parameter		Sym	Min	Typ[1]	Max	Unit
Master clock frequency	DSX-1	MCLK	-	1.544	-	MHz
	E1	MCLK	-	2.048	-	MHz
Master clock tolerance		MCLKt	-	± 50	-	ppm
Master clock duty cycle		MCLKd	10	-	90	%
Transmit clock frequency	DSX-1	TCLK	-	1.544	-	MHz
	E1	TCLK	-	2.048	-	MHz
Transmit clock tolerance		TCLKt	-	± 50	-	ppm
Transmit clock duty cycle		TCLKd	10	-	90	%
TPOS/TNEG to TCLK setup time		tSUT	25	-	-	ns
TCLK to TPOS/TNEG Hold time		tHT	25	-	-	ns

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 14. LXT331 Transmit Clock Timing

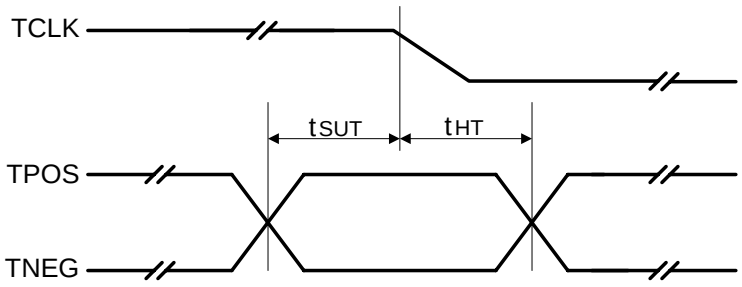


Table 13. LXT331 Receive Characteristics (See **Figure 15**)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Conditions
PMRK/NMRK pulse width	T1	tMPW	-	324	-	ns	
	E1	tMPW	-	244	-	ns	
Receiver throughput delay		tRXD	-	65	-	ns	3.0 V pulse

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 15. LXT331 Receive Timing

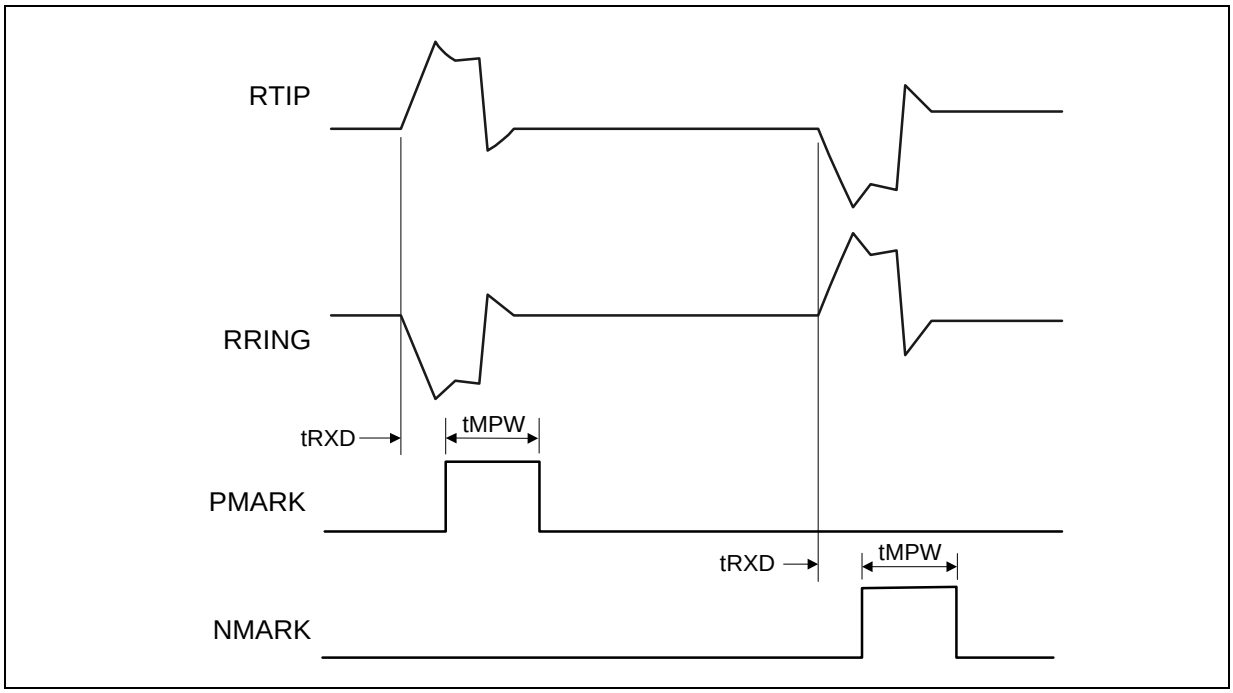


Table 14. LXT331 Serial I/O Timing Characteristics (See Figure 16 and Figure 17)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Rise/fall time - any digital output	tRF	-	-	100	ns	Load 1.6 mA, 50pF
SDI to SCLK setup time	tDC	50	-	-	ns	
SCLK to SDI hold time	tCDH	50	-	-	ns	
SCLK low time	tCL	240	-	-	ns	
SCLK high time	tCH	240	-	-	ns	
SCLK rise and fall time	tR, tF	-	-	50	ns	
PS to SCLK setup time	tPC	50	-	-	ns	
SCLK to PS hold time	tCPH	50	-	-	ns	
PS inactive time	tPWH	250	-	-	ns	
SCLK to SDO valid	tCDV	-	-	200	ns	
16th SCLK falling edge or PS rising edge to SDO high Z	tCDZ	-	100	-	ns	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 16. LXT331 Serial Input Timing Diagram

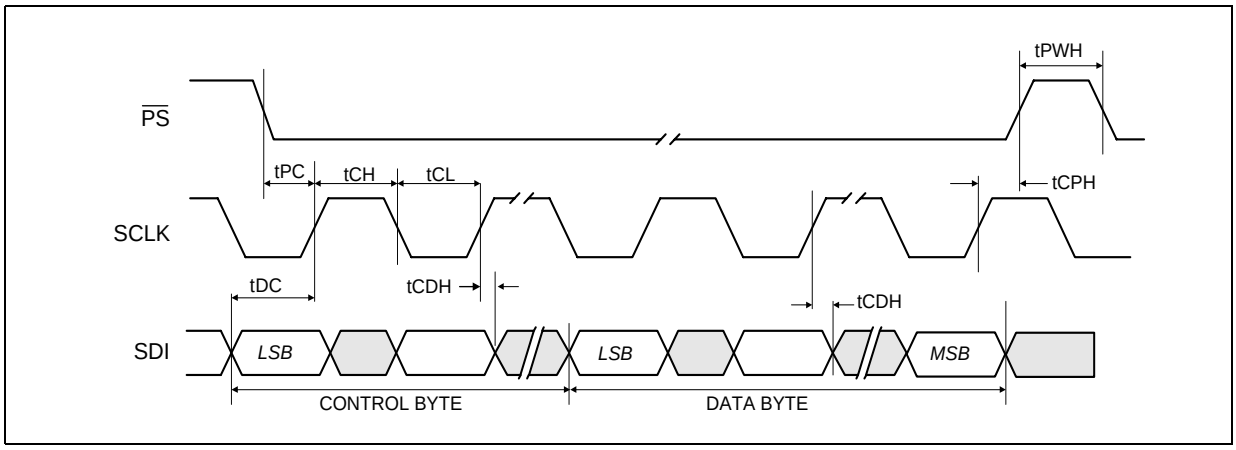
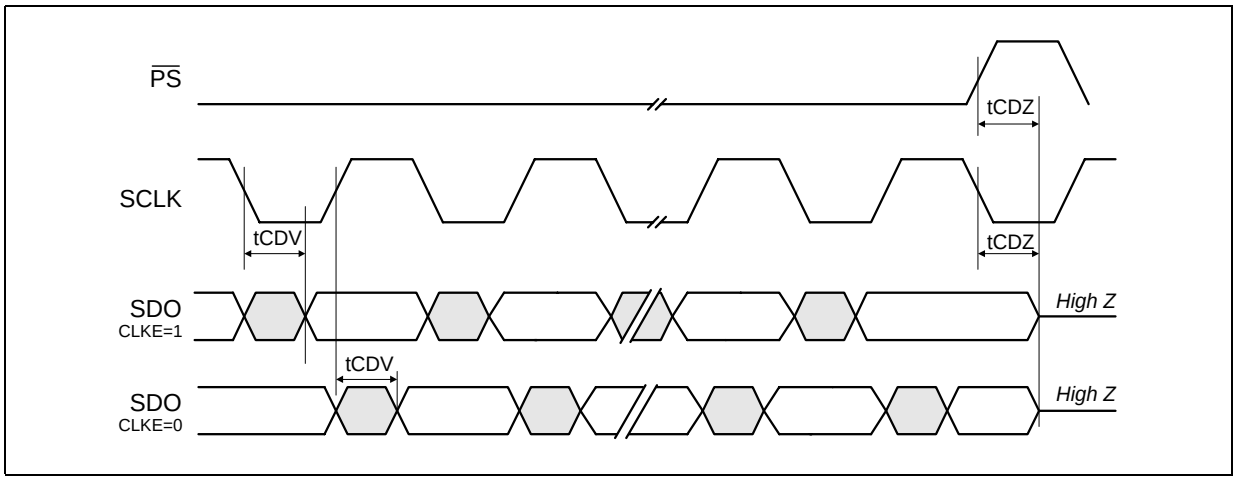
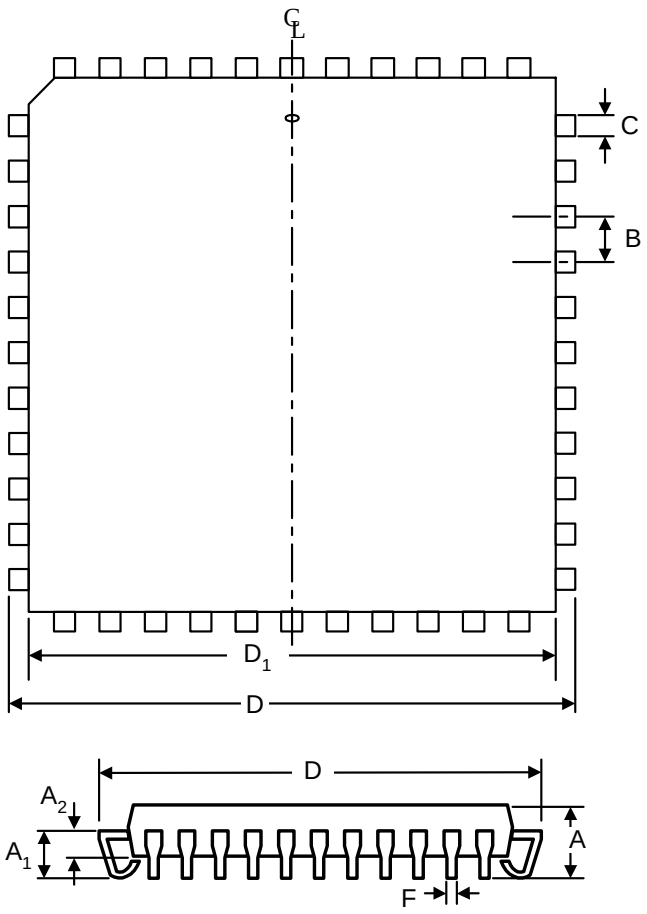


Figure 17. LXT331 Serial Output Timing Diagram



5.0 Mechanical Specifications

Figure 18. LXT331 PLCC Package Specification



Plastic Lead Chip Carrier (PLCC)

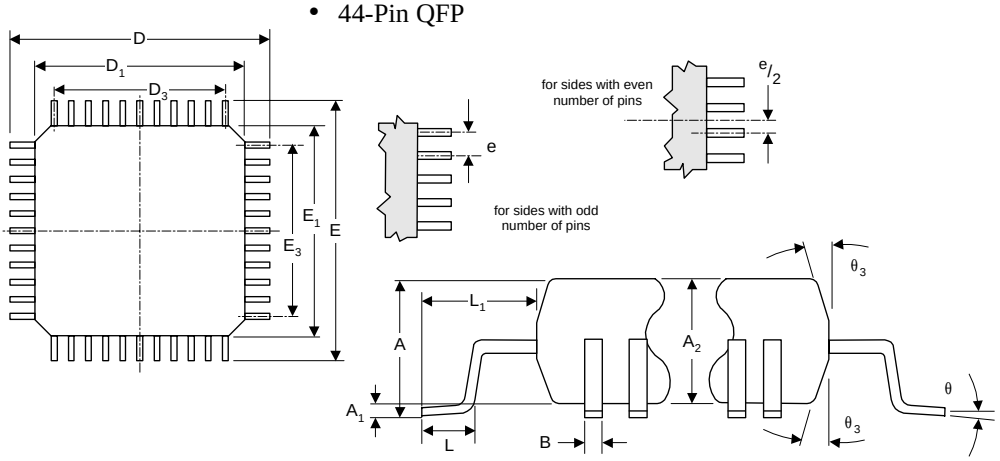
- Part Number LXT331PE
- Temperature Range -40°C to + 85°C
- Part Number LXT331PH
- Temperature Range -5°C to + 85°C
- 44-Pin PLCC

Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.165	0.180	4.191	4.572
A1	0.090	0.120	2.286	3.048
A2	0.062	0.083	1.575	2.108
B	0.050	–	1.270	–
C	0.026	0.032	0.660	0.813
D	0.685	0.695	17.399	17.653
D1	0.650	0.656	16.510	16.662
F	0.013	0.021	0.330	0.533

Figure 19. LXT331 QFP Package Specification

Quad Flat Pack

- Part Number LXT331QE
- Temperature Range -40°C to + 85°C
- Part Number LXT331QH
- Temperature Range -5°C to + 85°C
- 44-Pin QFP



Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	–	0.096	–	2.45
A1	0.010	–	0.25	–
A2	0.077	0.083	1.95	2.10
B	0.012	0.018	0.30	0.45
D	0.510	0.530	12.95	13.45
D1	0.390	0.398	9.90	10.10
D3	0.315 BSC[1] (nominal)		8.00 BSC[1] (nominal)	
E	0.510	0.530	12.95	13.45
E1	0.390	0.398	9.90	10.10
E3	0.315 BSC[1] (nominal)		8.00 BSC[1] (nominal)	
e	0.031 BSC[1] (nominal)		0.80 BSC[1] (nominal)	
L	0.029	0.041	0.73	1.03
L1	0.063 REF (nominal)		1.60 REF (nominal)	
q3	5°	16°	5°	16°
q	0°	7°	0°	7°

1. BSC—Basic Spacing between Centers