FEATURES

- Full Dielectric Isolation for High Reliability
- 60 dB typical Output Off Isolation at 10 Mhz
- Typical on resistance, R_{ON}, is 26 ohms
- CMOS Logic Circuitry for Low Power
- Excellent Noise Immunity & Extremely Low I_{SOL}
- On-chip Shift Register, and Latch Logic Circuitry
- Fully Flexible High Voltage Supply Combinations
- DC to 10 Mhz Analog Signal Frequency
- Excellent Latch-up Immunity

ABSOLUTE MAXIMUM RATINGS*

V_{DD} Logic Power Supply Voltage	0.5V to 18V
V_{PP}-V_{NN} Supply Voltage	300V
V_{PP} Positive High Voltage Supply	-0.5V to V_{NN} + 265V
V_{NN} Negative High Voltage Supply	-235V
Logic Input Voltage	0.5V to V_{DD} + 0.3V
Peak Analog Pulser Current / Channel	3.0A
Storage Temperature	-65° to + 150 °C
Analog Pulser Range	V_{AP} - V_{NN} = 0V to 240V
Power Dissipation	Plastic Package 0.8W
	Ceramic Package 2.0W

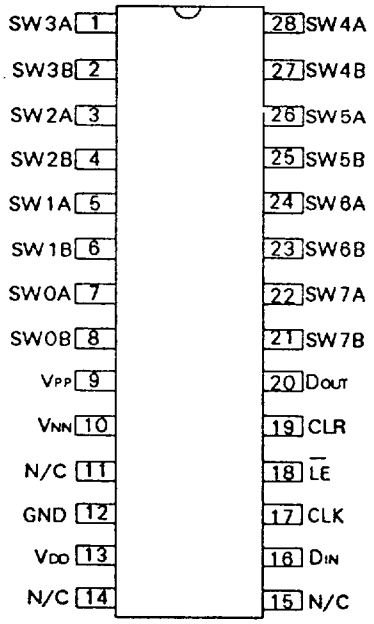
* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

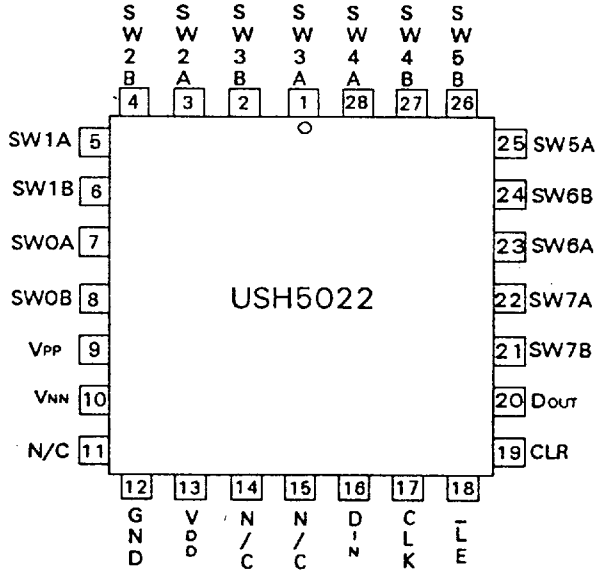
GENERAL DESCRIPTION

The USH5022 is an 8-channel high voltage analog switch which utilizes Universal's Proprietary full oxide isolation process for switching high voltage analog signals. This device can be used in ultrasound imaging systems and other high voltage applications which requires flexible high voltage switching controlled by internal CMOS logic signals.

The USH5022 combines high voltage bidirectional DMOS switches with low power CMOS logic to provide efficient control of high voltage analog signals. Input data is shifted into an 8-bit latch. To minimize any clock feedthrough noise, Latch Enable Bar should be left high until all bits are clocked in. The CL signal is active high and resets all the eight latches.

The USH5022-1, for example, is suitable for various combinations of high voltage supplies e.g., +40V / -230V, or +135V / -135V, or +260V / -10V applications.





V_{PP} - Vnn	28-lead Ceramic LCC	28-lead Ceramic Side-Brazed	28-lead Plastic DIP	28-lead PLCC	Operating Temperatures
270V	USH5022-AIL28	USH5022-AIC28	USH5022-AIP28	USH5022-AIK28	0°C to 70°C
220V	USH5022-Bil28	USH5022-BIC28	USH5022-BIP28	USH5022-BIK28	0°C to 70°C
160V	USH5022-CIL28	USH5022-CIC28	USH5022-CIP28	USH5022-CIK28	0°C to 70°C

ELECTRICAL CHARACTERISTICS

(over recomended operating conditions, V_{PP} = + 110V, V_{NN} = 110V and V_{DD} = 15V unless otherwise noted)*

DC CHARACTERISTICS

PARAMETERS	SYM	0°C		25°C			70°C		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
Small Signal R_{ON}	R_{ONS}		30		24	28		30	ohms	I_{SW} = 5mA
Small Signal R_{ON}	R_{ONS}		20		20	22		23	ohms	I_{SW} = 200mA
Delta R_{ON}	D R_{ONS}		20		10	20		20	%	I_{SW} = 5mA
Large Signal R_{ON}	R_{ONL}		90		28	40		100	ohms	V_{AP} = V_{PP}-10V I_{SW}=5mA
Switch Off Leakage/SW	I_{SOL}		1		0.5	1		1	uA	V_{AP} = V_{PP}-10V/V_{NN}+10V
DC Offset Switch Off	I_{DCOFF}		1		1	1		1	mV	R_L = 100K
DC Offset Switch On	I_{DCON}		1		1	1		1	mV	R_L = 100K
Pos. HV Supply Current	I_{PPQOFF}		10		50				uA	ALL SWITCHES OFF
Neg. HV Supply Current	I_{NNQOFF}		-10		-50				uA	ALL SWITCHES OFF
Pos. HV Supply Current	I_{PPQON}		10		50				uA	ALL SWITCHES ON I_{SW}=5mA
Neg. HV Supply Current	I_{NNQON}		-10		-50				uA	ALL SWITCHES ON I_{SW}=5mA
Analog Pulse Pk Current	I_{PAP}		2		1.5	2		2	A	V_{AP} Duty Cycle < 0.1%
Output Switch Frequency	f_{SW}		50		50			50	Khz	Duty Cycle = 50%
I_{PP} Ave. Supply Current	I_{PPAV}		5		6.5			7.5	mA	f_{SW} = 50Khz
I_{NN} Ave. Supply Current	I_{NNAV}		5		6.5			7.5	mA	f_{SW} = 50Khz
V_{DD} Ave. Current	I_{DDAV}		6		6			6	mA	f_{CLK} = 3Mhz
V_{DD} Quiescent Current	I_{DDQ}		10		1.8	5		10	uA	
Data Out Source Current	I_{SOR}		1.8			1.8		1.8	mA	V_{OUT} = V_{DD}-0.7V
Data Out Sink Current	I_{SINK}		-1.8		-1.8			-1.8	mA	V_{OUT} = 0.7V

AC CHARACTERISTICS

PARAMETERS	SYM	0°C		25°C			70°C		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
Set Up Time Before LE Rises	t_{SD}	150		150			150		ns	
LE Pulse Width	t_{WLE}	50		50			50		ns	
Clock to Dout Delay Time	t_{DO}		300			300		300	ns	
Din to Clock Set Up Time	t_{SU}	30		30			30		ns	
Din to Clock Hold Time	t_H	30		30			30		ns	
Logic Input Rise & Fall Time	t_R/t_F	10	200	10	10	200	10	200	ns	
Max. Logic Clock Frequency	f_{CLK}		5			5		5	Mhz	
CLK to HVOUT Turn On Time	t_{ON}		5		2	5		5	us	R_L = 10K ohm
CLK to HVOUT Turn Off Time	t_{OFF}		5		3	5		5	us	R_L = 10K ohm
Channel - Channel Cross-talk	K_{CR}	-60		-60	-65		-60		dB	f_{VIN} = 5Mhz/50 ohm load
Single Channel Off-Isolation	K_O	-45		-45	-50		-45		dB	f_{VIN} = 5Mhz/50 ohm load
Max. Positive Noise Glitch	V_{GP}		500			500		500	mV	680 ohms//220 pf load
Max. Negative Noise Glitch	V_{GN}		-1.2			-1.2		-1.2	V	680 ohms//220 pf load
Logic Input Cap.	C_A				3				pf	0V, 1Mhz
Switch Off Cap. to GND	$C_{SG(OFF)}$		10		8	10		10	pf	0V, 1Mhz
Switch On Cap. to GND	$C_{SG(ON)}$		30		18	30		30	pf	0V, 1Mhz

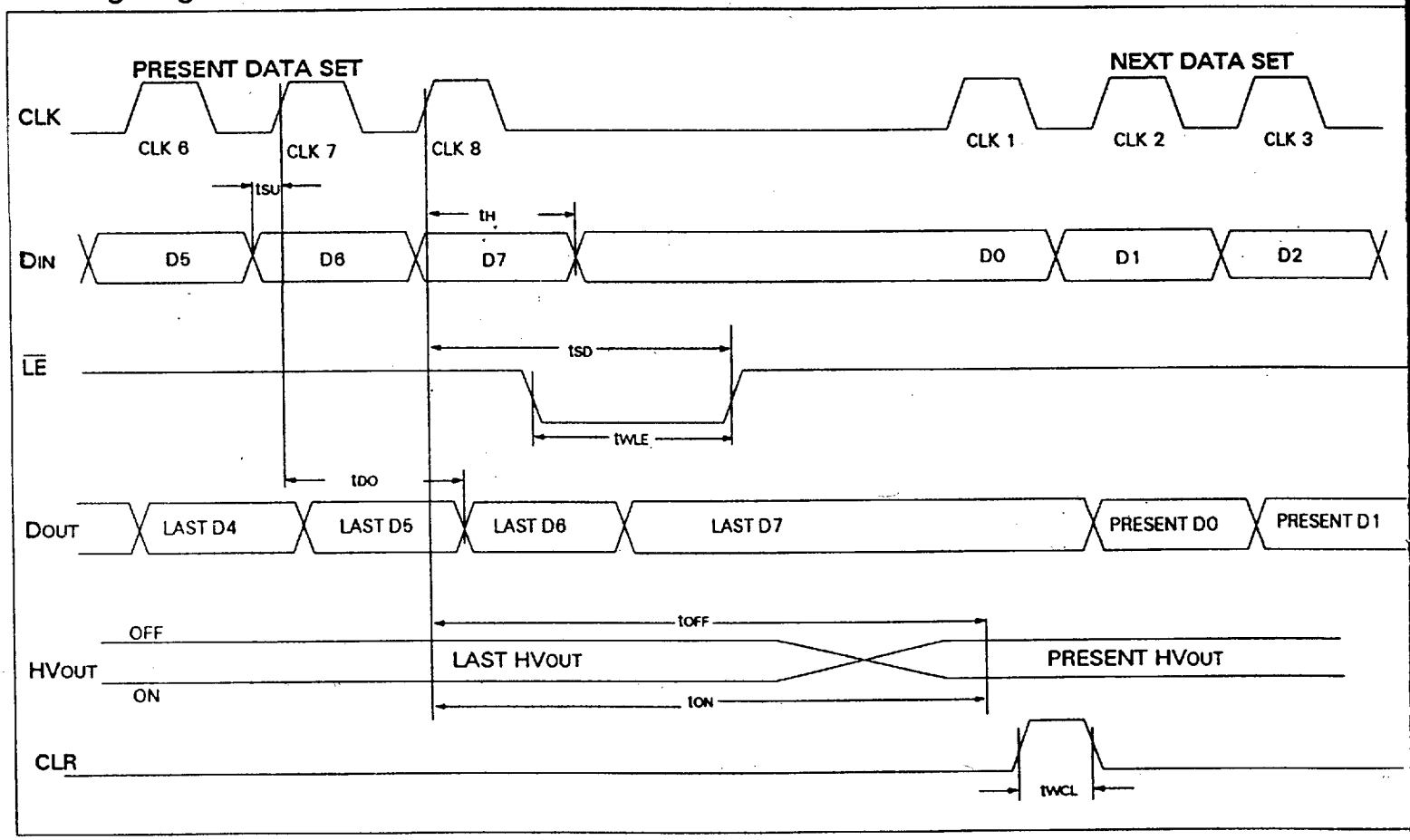
NOTE 1: V_{APDVDT} VALUE OF 12V/ns is the max output signal value that can be achieved with the USH5022-AI-K28

NOTE 2: CROSSTALK IS -60 dB (min) @ F_{VIN} = 5MHz/50 ohm LOAD, & IS -50dB(min) @ F_{VIN} = 15 MHz/50 ohm LOAD

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Device			Other Conditions
		USH5022-1	USH5022-2	USH5022-3	
V_{DD}	Logic Power Supply Voltage	10V to 15.5V	10V to 15.5V	10V to 15.5V	
V_{PP} - Mode A	Positive High Voltage Supply	40V	40V	40V	
V_{NN} - Mode A	Negative High Voltage Supply	-230V	-160V	-120V	
V_{PP} - Mode B	Positive High Voltage Supply	135V	110V	80V	
V_{NN} - Mode B	Negative High Voltage Supply	-135V	-110V	-80V	
V_{PP} - Mode C	Positive High Voltage Supply	260V	210V	40V	
V_{NN} - Mode C	Negative High Voltage Supply	-10V	-10V	-10V	
V_{IH}	Logic Input High Level	V_{DD}-2V<V_{IH}<V_{DD}	V_{DD}-2V<V_{IH}<V_{DD}	V_{DD}-2V<V_{IH}<V_{DD}	10V < V_{DD} < 15V
V_{IL}	Logic Input Low Level	0V<V_{IL}<2V	0V<V_{IL}<2V	0V<V_{IL}<2V	10V < V_{DD} < 15V
Power Sequence	GND, V_{DD}, V_{NN}, V_{PP}	SAME	SAME	SAME	V_{NN} > -10V

Timing Diagram



TRUTH TABLE

D0	D1	D2	D3	D4	D5	D6	D7	LE	CLR	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	HOLDS PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	OFF	PFF	OFF	OFF	OFF	OFF	OFF	OFF

Notes:
1. The eight switches operate independently.
2. Serial data is clocked in on the L→H transition CLK.
3. The switches go to a state retaining their present condition at the rising edge of LE. When LE is low the shift register data flows through the latch.
4. Dout is high when switch 7 is on.
5. Shift register clocking has no effect on the switch states if LE is high.
6. The clear input overrides all other pins.

Description of Operation

The USH5022 is a High Voltage Integrated Circuit (HIVIC) which contains eight independent high voltage bidirectional switches and the CMOS logic necessary to interface them to a CMOS environment. This HIVIC is designed to switch various analog signals into capacitive loads, and it is designed to conduct current pulses of 2A with 0.1% duty cycle.

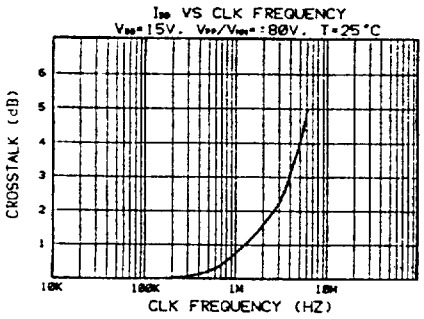
The switches (SW0 - SW7) are controlled by the serial data on (DIN), the shift register clock input (CLK), and the data transfer enable (LE). (See the Timing Diagram and the Truth Table) Serial data on line DIN is clocked into the eight-staged static shift registers.

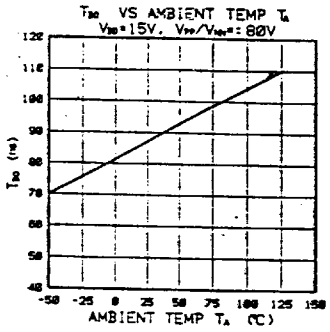
The data in the shift register is transferred to the latches by the latch enable LE. When LE is low the shift register data flows through the latch and controls the state of the switch.

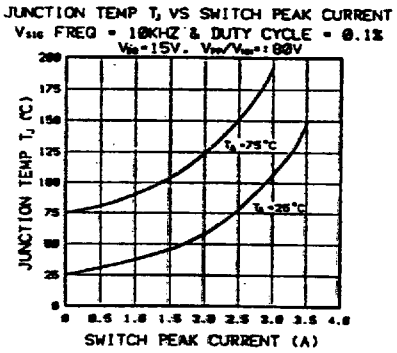
Pin Definitions

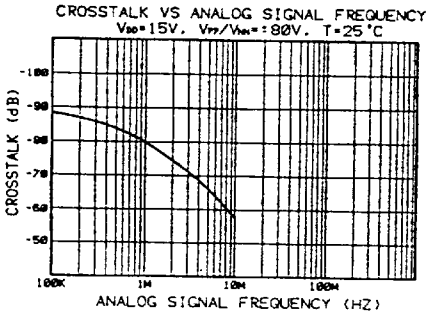
DIN	Serial Data Input to Shift Register
CLK	Serial Shift Clock
LE	Parallel Transfer Enable from Shift Registers to Latches
DOUT	Serial Data Out of Eighth Stage of Shift Register.
SW0 - 7	Eight Pairs of High Voltage Lines For Analog Signal Switching.
VPP	Positive High Voltage Supply for the Level Shift Circuit.
VNN	Negative High Voltage Supply for the Level Shift Circuits.
VCC	Logic Supply Pin
CLR	Clear pin

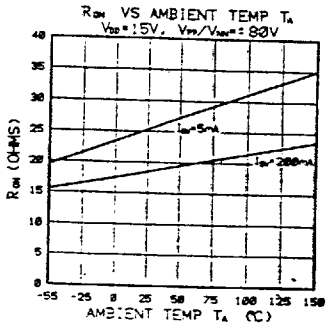
Typical Performance Curves

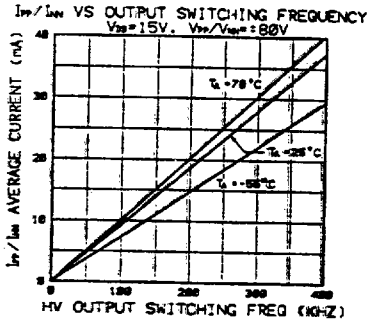


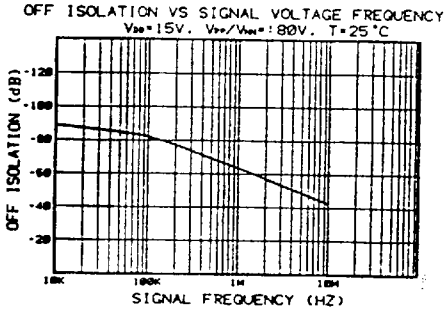


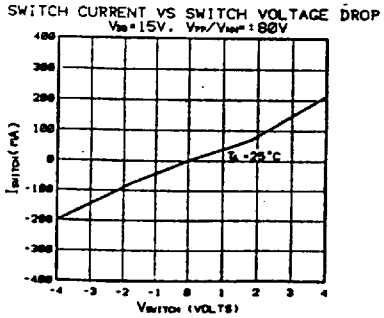


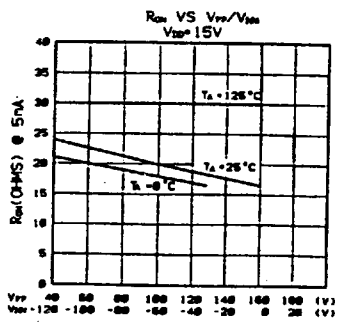












Logic Diagram