



# STiH251

## Advanced STB decoder with integrated DVB-T2 and DVB-T demodulator

Data brief

### Features

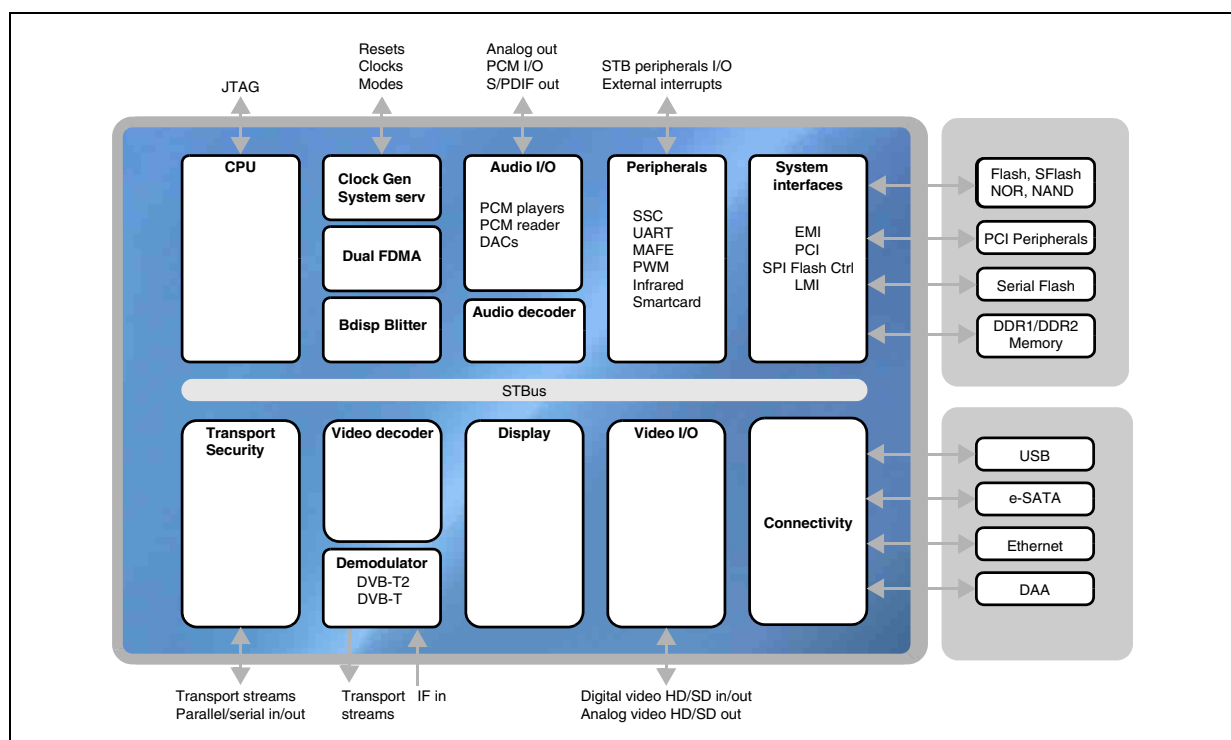
- Integrated DVB-T2 and DVB-T demodulator
  - User-selectable mode
  - Compatible with low to high IF tuners
  - ADC for RF signal strength indicator
- Advanced high-definition video decoding (H264/VC-1/MPEG2)
- Advanced standard-definition video decoding (H264/VC-1/MPEG2/AVS)
- Advanced multi-channel audio decoding (MPEG 1, 2, MP3, DD/DD+, AAC/AAC+, WMA9/WMA9Pro)
- Linux, Windows CE and OS21 compatible applications CPU
- 32-bit DDR1/DDR2 compatible local memory interface

- Multi-stream, DVR capable transport stream processing
- Extensive connectivity (dual USB hosts, e-SATA, Ethernet MAC/MII/RMII and PCI)
- Advanced security and DRM support including SVP, MS-DRM and DTCP-IP

### Description

The STiH251 uses state-of-the-art process technology to provide a fully featured HD AVC, DVB-T2 and DVB-T demodulator/decoder IC.

It is a highly integrated system-on-chip, suitable for STB markets across terrestrial, and terrestrial/IP hybrid networks worldwide.



# 1 Introduction

The STiH251 is designed to be optimized, both in cost and performance, with the most advanced can tuners and silicon tuners available on the market and is compliant with DVB-T2 and DVB-T standards. The STiH251 front end has one of the lowest power consumptions on the market today. This has been made possible thanks to technology and clock rate management. This also has the advantage of improving channel acquisition and re-acquisition efficiency.

The STiH251 is delivered with a full suite of low-level drivers and application software, with detailed user manuals and reference design schematics to enable seamless integration in complex digital TV systems such as iDTV, set-top boxes or PCTV dongles.

Features	Benefits
Combines a configurable DVB-T2 and DVB-T demodulator with STB decoding and display functions	This highly integrated SoC helps to reduce board area and manufacturing cost, allowing low cost and small size STBs to be designed for DVB-T2 and DVB-T networks
Applications CPU, 32K I cache, 32K D cache	Superscalar performance from a single CPU core, using standard tools and operating systems (Linux, OS21)
STMicroelectronics' video decoding system with ST231 processor	Decoding of advanced high definition standards for MPEG2, H264, VC-1 broadcast, with the performance and flexibility for web-based content decoding such as Flash <sup>®</sup> , DivX <sup>™</sup> , MJPEG and Real <sup>®</sup>
Dual USB 2.0 hosts, e-SATA, Ethernet MAC with MII/RMII and TMII, PCI	Extensive high speed connectivity for the widest range of STB peripherals, such as Flash drives, external HDDs, home network controllers (for example MoCA <sup>®</sup> , Wi-Fi), DOCSIS <sup>®</sup> modem and so on
Low power process, design and architecture	Best in class, low power standby mode, to meet emerging energy standards for STBs. Dynamic configuration of power to individual sub-systems enables power-efficient active standby modes
Advanced 2D graphics and display subsystem which also supports 3D user interface effects and 1080p60 display output	Allows visually appealing user interfaces and video rich navigation to be offered to consumers, while high quality progressive output can be watched on the latest high definition displays

## 2 Revision history

**Table 1. Document revision history**

Date	Revision	Changes
16-Dec-2010	1	Initial release.
16-Mar-2011	2	Reference to DVB-C removed

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