SmartFusion2 System-on-Chip FPGAs

Microsemi's SmartFusion®2 SoC FPGAs integrate fourth generation flash-based FPGA fabric, an ARM® Cortex™-M3 processor, and high performance communications interfaces on a single chip. The SmartFusion2 family is the industry's lowest power, most reliable and highest security programmable logic solution. This next generation SmartFusion2 architecture offers up to 3.6X gate count implemented with 4-input look-up table (LUT) fabric with carry chains, giving 2X performance, and includes multiple embedded memory options and math blocks for digital signal processing (DSP). The 166 MHz ARM Cortex-M3 processor is enhanced with an embedded trace macrocell (ETM), memory protection unit (MPU), 8 Kbyte instruction cache, and additional peripherals including controller area network (CAN), Gigabit Ethernet, and high speed universal serial bus (USB). High speed serial interfaces include peripheral component interconnect express (PCIe), 10 Gbps attachment unit interface (XAUI) / XGMII extended sublayer (XGXS) + native serialization/deserialization (SERDES) communication, while double data rate 2 (DDR2)/DDR3 memory controllers provide high speed memory interfaces.

SmartFusion2 Family

Reliability

- Single Event Upset (SEU) Immune
  - Zero FIT FPGA Configuration Cells
- Single Error Correct Double Error Detect (SECDED) Protection on the Following:
  - Ethernet Buffers
  - CAN Message Buffers
  - Cortex-M3 Embedded Scratch Pad Memory (eSRAMs)
  - USB Buffers
  - PCIe Buffer
  - DDR Memory Controllers with Optional SECDED Modes
- Buffers Implemented with SEU Resistant Latches on the Following:
  - DDR Bridges (MSS, MDDR, FDDR)
  - Instruction Cache
  - MMUART FIFOs
  - SPI FIFOs
- NVM Integrity Check at Power-Up and On-Demand
- No External Configuration Memory Required—Instant-On, Retains Configuration When Powered Off

Security

- Design Security Features (available on all devices)
  - Intellectual Property (IP) Protection via Unique Security Features and Use Models New to the PLD Industry
  - Encrypted User Key and Bitstream Loading, Enabling Programming in Less-Trusted Locations
  - Supply-Chain Assurance Device Certificate
  - Enhanced Anti-Tamper Features
  - Zeroization
- Data Security Features (available on premium devices)
  - Non-Deterministic Random Bit Generator (NRBG)
  - User Cryptographic Services (AES-256, SHA-256, Elliptical Curve Cryptographic (ECC) Engine)
  - User Physically Unclonable Function (PUF) Key Enrollment and Regeneration
  - CRI Pass-Through DPA Patent Portfolio License
  - Hardware Firewalls Protecting Microcontroller Subsystem (MSS) Memories

Low Power

- Low Static and Dynamic Power
  - Flash*Freeze Mode for Fabric
- For the M2S050 Device:
  - < 1 mW in Flash*Freeze Mode
  - 10 mW in Standby Mode
- Based on 65 nm Nonvolatile Flash Process

High-Performance FPGA

- Efficient 4-Input LUTs with Carry Chains for High Performance and Low Power
- Up to 236 Blocks of Dual-Port 18 Kbit SRAM (Large SRAM) with 400 MHz Synchronous Performance (x18, x9, x4, x2, x1)
- Up to 240 Blocks of Three-Port 1 Kbit SRAM with 2 Read Ports and 1 Write Port (micro SRAM)
- High Performance DSP Signal Processing
  - Up to 240 Fast Math Blocks with 18 x 18 Signed Multiplication, 17 x 17 Unsigned Multiplication and 44-Bit Accumulator

Microcontroller Subsystem (MSS)

- Hard 166 MHz 32-Bit ARM Cortex-M3 Processor
  - 1.25 DMIPS/MHz
  - 8 Kbyte Instruction Cache
  - Embedded Trace Macrocell (ETM)
  - Memory Protection Unit (MPU)
  - Single Cycle Multiplication, Hardware Divide
  - JTAG Debug (4 wires), Serial Wire Debug (SWD, 2 wires), and Serial Wire Viewer (SWV) Interfaces
- 64 KB Embedded SRAM (eSRAM)
- Up to 512 KB Embedded Nonvolatile Memory (eNVM)
- Triple Speed Ethernet (TSE) 10/100/1000 Mbps MAC
- USB 2.0 High Speed On-The-Go (OTG) Controller with ULPI Interface
- CAN Controller, 2.0B Compliant, Conforms to ISO11898-1, 32 Transmit and 32 Receive Buffers
- Two Each: SPI, I^2C, Multi-Mode UARTs (MMUART) Peripherals
- Hardware Based Watchdog Timer
- 1 General Purpose 64-Bit (or two 32-bit) Timer(s)
- Real-Time Calendar/Counter (RTC)
- DDR Bridge (4 Port Data R/W Buffering Bridge to DDR Memory) with 64-Bit AXI Interface
- Non-Blocking, Multi-Layer AHB Bus Matrix Allowing Multi-Master Scheme Supporting 10 Masters and 7 Slaves
- Two AHB/APB Interfaces to FPGA Fabric (master/slave capable)
- Two DMA Controllers to Offload Data Transactions from the Cortex-M3 Processor
  - 8-Channel Peripheral DMA (PDMA) for Data Transfer Between MSS Peripherals and Memory
  - High Performance DMA (HPDMA) for Data Transfer Between eSRAM and DDR Memories

Clocking Resources

- Clock Sources
  - Up to Two High Precision 32 KHz to 20 MHz Main Crystal Oscillator
  - 1 MHz Embedded RC Oscillator
  - 50 MHz Embedded RC Oscillator
- Up to 8 Clock Conditioning Circuits (CCCs) with Up to 8 Integrated Analog PLLs
  - Output Clock with 8 Output Phases and 45° Phase Difference (Multiply/Divide, and Delay Capabilities)
  - Frequency: Input 1 to 200 MHz, Output 20 to 400 MHz

High Speed Serial Interfaces

- Up to 16 SERDES Lanes, Each Supporting:
  - XGXS/XAUI Extension (to implement a 10 Gbps (XGMII) Ethernet PHY interface)
  - Native SERDES Interface Facilitates Implementation of Serial RapidIO in Fabric or an SGMII Interface to the Ethernet MAC in MSS
  - PCI Express (PCIe) Endpoint Controller

    x1, x2, x4 Lane PCI Express Core with 16-bit PIPE Interface (Gen1/Gen2)

    256 Bytes Maximum Payload Size

    64-/32-Bit AXI/AHB Master and Slave Interfaces to the Application Layer

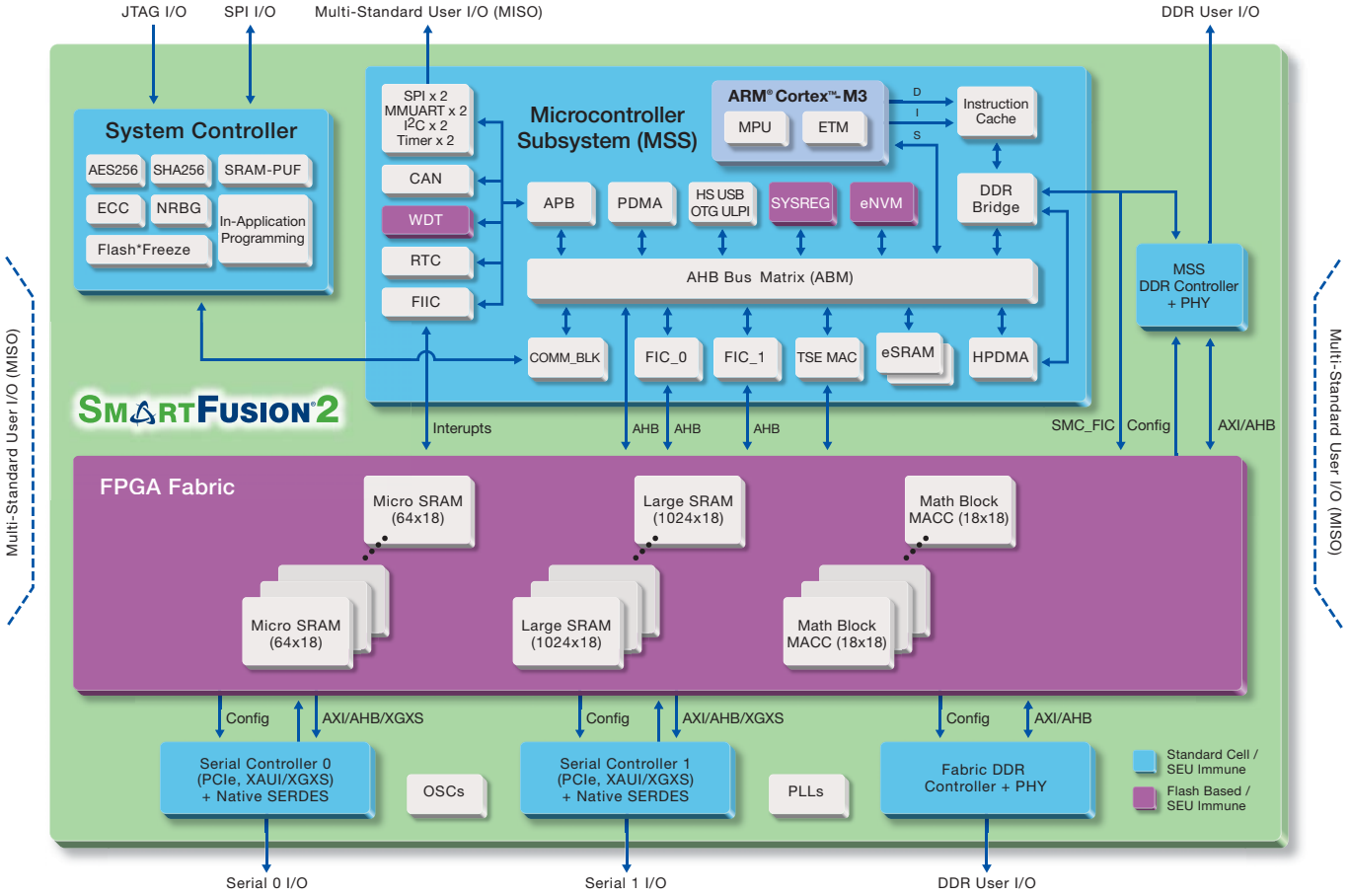
High Speed Memory Interfaces

- Up to 2 High Speed DDRx Memory Controllers
  - MSS DDR (MDDR) and Fabric DDR (FDDR) Controllers
  - Supports LPDDR/DDR2/DDR3
  - Maximum 333 MHz Clock Rate
  - SECDED Enable/Disable Feature
  - Supports Various DRAM Bus Width Modes, x16, x18, x32, x36
  - Supports Command Reordering to Optimize Memory Efficiency
  - Supports Data Reordering, Returning Critical Word First for Each Command
- SDRAM Support

Operating Voltage and I/Os

- 1.2 V Core Voltage
- Multi-Standard User I/Os (MSIO/MSIOD)
  - LVTTL/LVCMOS 3.3 V
  - LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V
  - DDR (SSTL2_1, SSTL2_2)
  - DDR2 (SSTL18_1, SSTL18_2)
  - LVDS, MLVDS, Mini-LVDS, RSDS Differential Standards
  - PCI
  - LVPECL (receiver only)
- DDR I/Os (DDRIO)
  - DDR, DDR2, DDR3, LPDDR, SSTL2, SSTL18, HSTL
  - LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V

SmartFusion2 SoC FPGA Block Diagram



Acronyms

AES	Advanced Encryption Standard
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
AXI	Advanced eXtensible Interface
COMM_BLK	Communication Block
DDR	Double Data Rate
DPA	Differential Power Analysis
ECC	Elliptical Curve Cryptography
EDAC	Error Detection And Correction
ETM	Embedded Trace Macrocell
FDDR	DDR2/3 controller in FPGA fabric
FIC	Fabric Interface Controller
FIIC	Fabric Interface Interrupt Controller
HS USB OTG	High Speed USB 2.0 On-The-Go
IAP	In-Application Programming
MACC	Multiply-Accumulate
MDDR	DDR2/3 Controller in MSS
MMUART	Multi-Mode UART
MPU	Memory Protection Unit
MSS	Microcontroller Subsystem
SECDED	Single Error Correct Double Error Detect
SEU	Single Event Upset
SHA	Secure Hashing Algorithm
SMC_FIC	Soft Memory Controller
TSE	Triple Speed Ethernet (10/100/1000 Mbps)
ULPI	UTMI + Low Pin Interface
UTMI	USB 2.0 Transceiver Macrocell Interface
WDT	Watchdog Timer
XAUI	10 Gbps Attachment Unit Interface
XGMII	10 Gigabit Media Independent Interface
XGXS	XGMII Extended Sublayer

Table 1 • SmartFusion2 SoC FPGA Product Family

	Features	M2S005	M2S010	M2S025	M2S050	M2S080	M2S120
FPGA	Logic Modules (4-Input LUT)	4,956	9,744	23,988	48,672	82,232	120,348
	LSRAM 18K Blocks	10	21	31	69	160	236
	uSRAM 1K Blocks	11	22	34	72	160	240
	Total RAM (Bits)	191K	400K	592K	1,314K	3,040K	4,500K
	Math Blocks	11	22	34	72	160	240
	PLLs and CCCs	2	2	4	6	8	8
MSS	Cortex-M3 Processor + Instruction Cache	Yes	Yes	Yes	Yes	Yes	Yes
	eNVM (Bytes)	128K	256K	256K	256K	512K	512K
	eSRAM (Bytes)	64K	64K	64K	64K	64K	64K
	eSRAM (Bytes non-SECDED)	80K	80K	80K	80K	80K	80K
	CAN 2.0 A and B	1	1	1	1	1	1
	Triple speed Ethernet 10/100/1000	1	1	1	1	1	1
	USB 2.0 High Speed On-The-Go	1	1	1	1	1	1
	Multi-Mode UART	2	2	2	2	2	2
	SPI	2	2	2	2	2	2
	I2C	2	2	2	2	2	2
	Timer	2	2	2	2	2	2
Memory, Serial I/F	DDR Controllers	1x18	1x18	1x18	2x36	2x36	2x36
	SERDES Channels	0	4	4	8	8	16
	PCIe Endpoint × 4	0	1	1	2	2	4
User I/O	3.3 V Multi-Standard User I/Os (MSIOs)	123	123	159	139	292	292
	MSIOD I/Os	28	40	40	62	106	106
	DDRIO I/Os	66	70	90	176	176	176
	Total User I/Os	217	233	289	377	574	574
	SERDES I/Os	0	16	16	32	64	64
	Total User I/Os + SERDES I/Os	217	249	305	409	638	638

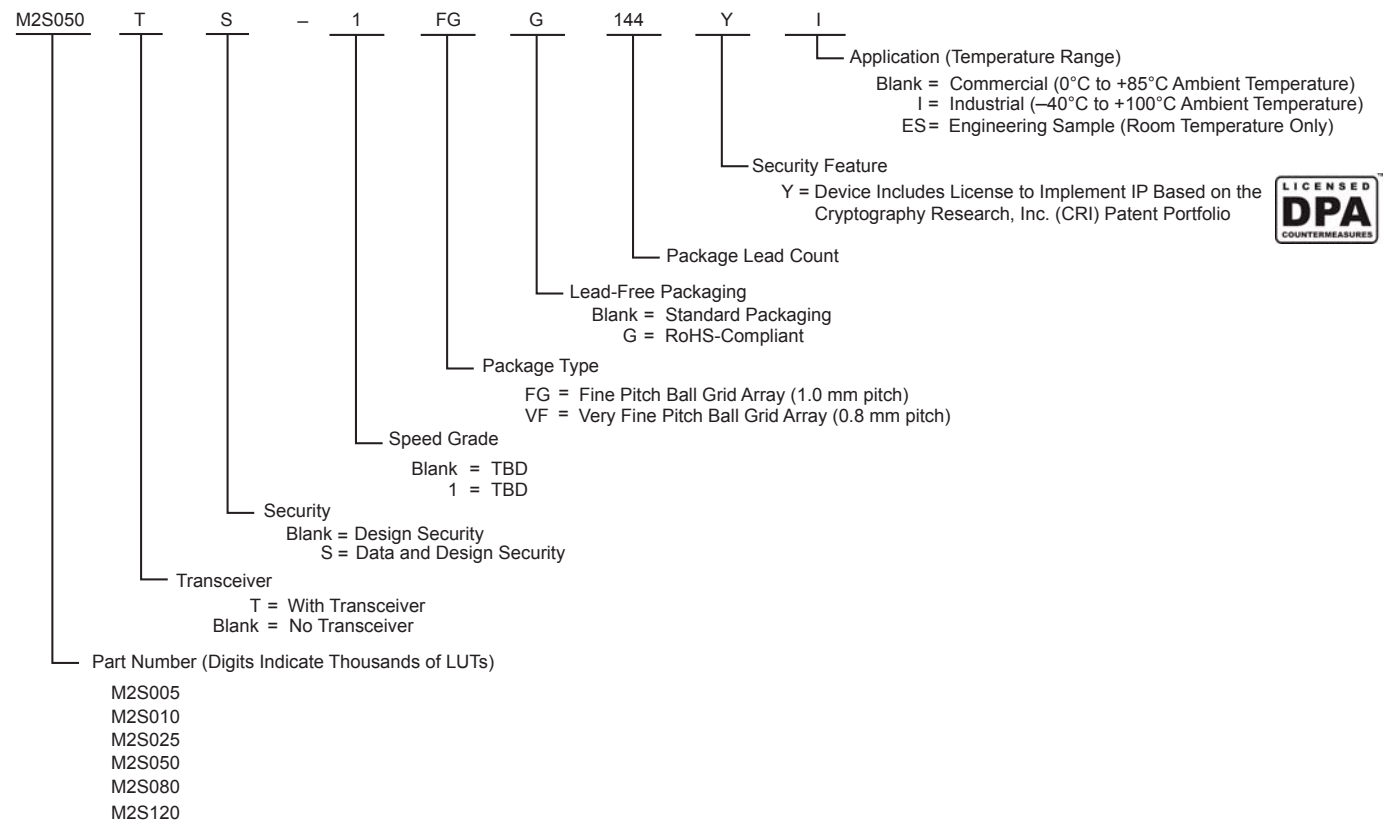
I/Os Per Package

Table 2 • I/Os per Package and Package Options

Package Options	VF400		FG484		FG896		FC1152	
Pin Count	400		484		896		1,152	
Ball Pitch (mm)	0.8		1.0		1.0		1.0	
Length × Width (mm\mm)	17 × 17		23 × 23		31 × 31		35 × 35	
	I/Os	XCVRs	I/Os	XCVRs	I/Os	XCVRs	I/Os	XCVRs
M2S005	160	–	217	–	–	–	–	–
M2S010	160	4	233	4	–	–	–	–
M2S025	160	4	267	4	–	–	–	–
M2S050	160	4	267	4	377	8	–	–
M2S080	–	–	–	–	–	–	574	8
M2S120	–	–	–	–	–	–	574	16

Note: User I/Os do not include the SERDES and JTAG pins.

SmartFusion2 Ordering Information



SmartFusion2 Valid Part Numbers

Table 3 • SmartFusion2 Valid Part Numbers for Devices with Design Security

Commercial		Industrial	
Std. Speed Grade	**–1 Speed Grade**	**–1 Speed Grade**	**–1 Speed Grade, Data Security**
M2S005-VF400	M2S005-1VF400	M2S005-1VF400I	M2S005S-1VF400I
M2S010-VF400	M2S010-1VF400	M2S010-1VF400I	M2S010S-1VF400I
M2S025-VF400	M2S025-1VF400	M2S025-1VF400I	M2S025S-1VF400I
M2S050-VF400	M2S050-1VF400	M2S050-1VF400I	M2S050S-1VF400I
M2S005-FG484	M2S005-1FG484	M2S005-1FG484I	M2S005S-1FG484I
M2S010-FG484	M2S010-1FG484	M2S010-1FG484I	M2S010S-1FG484I
M2S025-FG484	M2S025-1FG484	M2S025-1FG484I	M2S025S-1FG484I
M2S050-FG484	M2S050-1FG484	M2S050-1FG484I	M2S050S-1FG484I
M2S050-FG896	M2S050-1FG896	M2S050-1FG896I	M2S050S-1FG896I
M2S080-FC1152	M2S080-1FC1152	M2S080-1FC1152I	M2S080S-1FC1152I
M2S120-FC1152	M2S120-1FC1152	M2S120-1FC1152I	M2S120S-1FC1152I
Transceivers	**Transceivers**	**Transceivers**	**Transceivers**
M2S010T-VF400	M2S010T-1VF400	M2S010T-1VF400I	M2S010TS-1VF400I
M2S025T-VF400	M2S025T-1VF400	M2S025T-1VF400I	M2S025TS-1VF400I
M2S050T-VF400	M2S050T-1VF400	M2S050T-1VF400I	M2S050TS-1VF400I
M2S010T-FG484	M2S010T-1FG484	M2S010T-1FG484I	M2S010TS-1FG484I
M2S025T-FG484	M2S025T-1FG484	M2S025T-1FG484I	M2S025TS-1FG484I
M2S050T-FG484	M2S050T-1FG484	M2S050T-1FG484I	M2S050TS-1FG484I
M2S050T-FG896	M2S050T-1FG896	M2S050T-1FG896I	M2S050TS-1FG896I
M2S080T-FC1152	M2S080T-1FC1152	M2S080T-1FC1152I	M2S080TS-1FC1152I
M2S120T-FC1152	M2S120T-1FC1152	M2S120T-1FC1152I	M2S120TS-1FC1152I

SmartFusion2 Device Status

Family Devices	Status
M2S050T	Advance

Contact your local Microsemi SoC Products Group representative for device availability:
http://www.microsemi.com/soc/contact/default.aspx.

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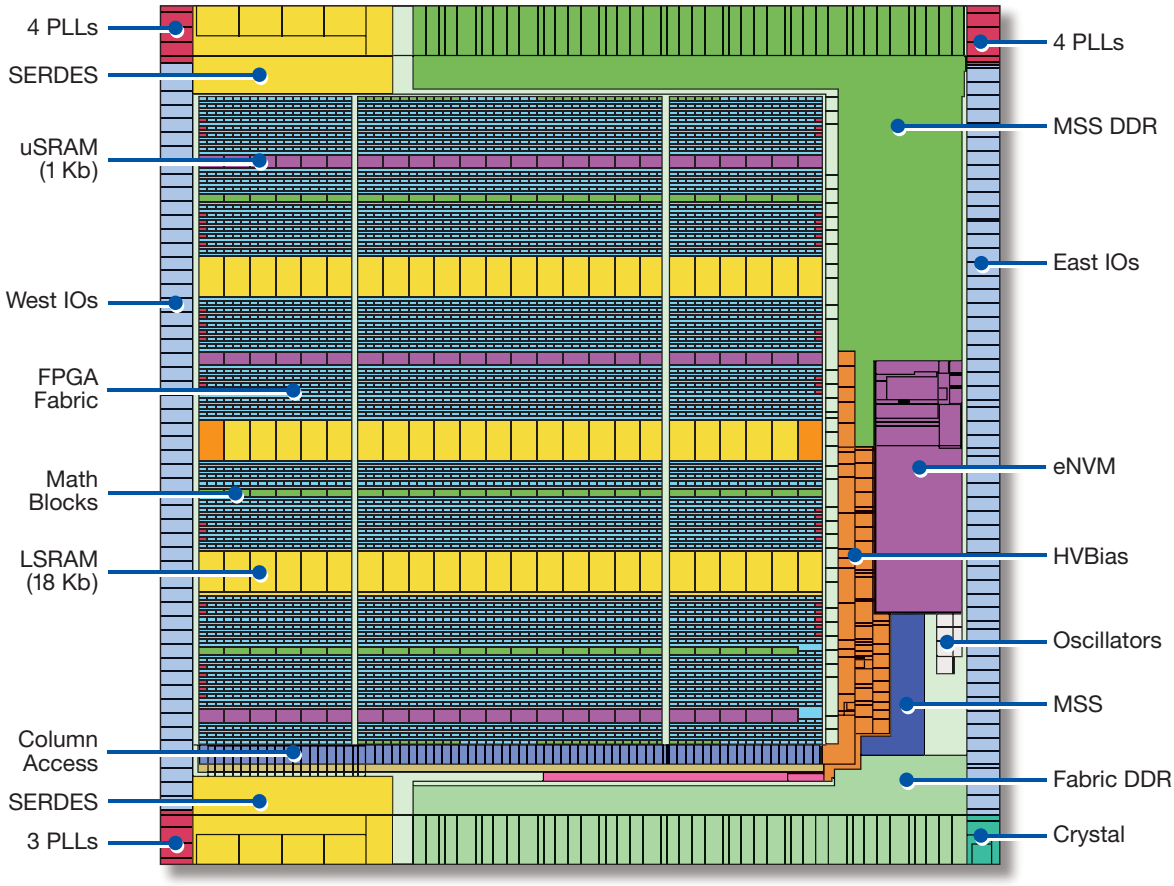
1 – SmartFusion2 Device Family Overview

Microsemi's SmartFusion2 SoC FPGAs integrate fourth generation flash-based FPGA fabric, an ARM Cortex-M3 processor and high performance communications interfaces on a single chip. The SmartFusion2 family is the industry's lowest power, highest reliability and most secure programmable logic solution. This next generation SmartFusion2 architecture offers up to 3.6X gate count implemented with 4-input look-up table (LUT) fabric with carry chains, giving 2X performance, and includes multiple embedded memory options and math blocks for DSP. The 166 MHz ARM Cortex-M3 processor is enhanced with ETM and 8 Kbyte instruction cache, and additional peripherals including CAN, Gigabit Ethernet, and high speed USB. High speed serial interfaces enable PCIe, XAUI / XGXS + Native SERDES communication while DDR2/DDR3 memory controllers provide high speed memory interfaces.

SmartFusion2 Chip Layout



Reliability

SmartFusion2 flash-based fabric has zero FIT configuration rate due to its single event upset (SEU) immunity, which is critical in reliability applications. The flash fabric also has the advantage that no external configuration memory is required, making the device instant-on; it retains configuration when powered off. To complement this unique FPGA capability, SmartFusion2 adds reliability to many other aspects of the device. Single Error Correct Double Error Detect (SECDED) protection is implemented on the Cortex-M3 embedded scratch pad memory, Ethernet, CAN and USB buffers, and is optional on the DDR memory controllers. This means that if a one-bit error is detected, it will be corrected. Errors of more than one bit are detected only and not corrected. SECDED error signals are brought to the FPGA fabric to allow the user to monitor the status of these protected internal memories. Other areas of the architecture are implemented with latches, which are not subject to SEUs. Therefore, no correction is needed in these locations: DDR Bridges (MSS, MDDR, FDDR), Instruction Cache and MMUART, SPI, and PCIe FIFOs.

Highest Security Devices

Building further on the intrinsic security benefits of flash nonvolatile memory technology, the SmartFusion2 family incorporates essentially all the legacy security features that made the original SmartFusion, Fusion®, IGLOO®, and ProASIC®3 third-generation flash FPGAs and cSoCs the gold standard for secure devices in the PLD industry. In addition, the fourth-generation flash-based SmartFusion2 SoC FPGAs add many unique design and data security features and use models new to the PLD industry.

Design Security vs. Data Security

When classifying security attributes of programmable logic devices (PLDs), a useful distinction is made between design security and data security.

Design Security

Design security is protecting the intent of the owner of the design, such as keeping the design and associated bitstream keys confidential, preventing design changes (insertion of Trojan Horses, for example), and controlling the number of copies made throughout the device life cycle. Design security may also be known as intellectual property (IP) protection. It is one aspect of anti-tamper (AT) protection. Design security applies to the device from initial production, includes any updates such as in-the-field upgrades, and can include decommissioning of the device at the end of its life, if desired. Good design security is a prerequisite for good data security.

The following are the main design security features supported:

- User key and bitstream loading in less-trusted locations
  - Encrypted key loading using device-unique built-in factory key
- Methods to verify devices are programmed correctly, even if done in less-trusted locations
- Supply-chain assurances to eliminate counterfeiting
- Differential power analysis (DPA) and enhanced anti-tamper features to address non-invasive, semi-invasive, and invasive attacks
- Ability to zeroize (destroy) all sensitive stored data in the event of tampering
- The M2S080 and M2S120 also have the following features:
  - Elliptic Curve Cryptography (ECC) for securely loading user keys
  - An SRAM-type Physically Unclonable Function (SRAM-PUF) for device authentication

Data Security

Data security is protecting the information the FPGA is storing, processing, or communicating in its role in the end application. If, for example, the configured design is implementing the key management and encryption portion of a secure military radio, data security could entail encrypting and authenticating the radio traffic, and protecting the associated application-level cryptographic keys. Data security is closely related to the terms information assurance (IA) and information security.

All SmartFusion2 devices incorporate enhanced design security, making them the most secure programmable logic devices ever made. Select SmartFusion2 models also include an advanced set of on-chip data security features that make designing secure information assurance applications easier and better than ever before.

The following are the main data security features supported:

- Non-deterministic random bit generator (NRBG) service
- User Cryptographic services (e.g., AES-128/-256, SHA-256, and HMAC)
- Hardware firewalls protecting MSS memories
- Cryptography Research Inc. (CRI) pass-through Differential Power Analysis (DPA) Patent Portfolio license
- The M2S080 and M2S120 also have the following features:
  - Elliptic Curve Cryptography (ECC) cryptographic computation services
  - User PUF key enrollment and regeneration for advanced design and data security applications

Low Power

Microsemi's flash-based FPGA fabric results in extremely low power design implementation with static power on the M2S050 device as low as 10 mW. Flash*Freeze (F*F) technology provides an ultra-low power static mode (Flash*Freeze mode) for SmartFusion2 devices, with power less than 1 mW. F*F mode entry retains all the SRAM and register information and the exit from F*F mode achieves rapid recovery to active mode.

High Performance FPGA Fabric

Built on 65 nm process technology, the SmartFusion2 FPGA fabric is composed of 4 building blocks: the logic module, the large SRAM, the micro SRAM and the Math block. The logic module is the basic logic element and has advanced features:

- A fully permutable 4-input LUT (look-up table) optimized for lowest power
- A dedicated carry chain based on carry look-ahead technique
- A separate flip-flop which can be used independently from the LUT

The 4-input look-up table can be configured either to implement any 4-input combinatorial function or to implement an arithmetic function where the LUT output is XORed with carry input to generate the sum output.

Dual-Port Large SRAM (LSRAM)

Large SRAM (RAM1Kx18) is targeted for storing large memory for use with various operations. Each LSRAM block can store up to 18,432 bits. Each RAM1Kx18 block contains two independent data ports: Port A and Port B. The LSRAM is synchronous for both Read and Write operations. Operations are triggered on the rising edge of the clock. The data output ports of the LSRAM have pipeline registers which have control signals that are independent of the SRAM's control signals.

Three-Port Micro SRAM (uSRAM)

Micro SRAM (RAM64x18) is the second type of SRAM which is embedded in the fabric of SmartFusion2 devices. RAM64x18 uSRAM is a 3-port SRAM; it has two read ports (Port A and Port B) and one write

port (Port C). The two read ports are independent of each other and can perform Read operations in both synchronous and asynchronous modes. The write port is always synchronous. The uSRAM block is approximately 1 Kb (1,152 bits) in size. These uSRAM blocks are primarily targeted for building embedded FIFOs to be used by any embedded fabric masters.

Math Blocks for DSP Applications

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. SmartFusion2 implements a custom 18x18 Multiply-Accumulate (18x18 MACC) block for efficient implementation of complex DSP algorithms such as finite impulse response (FIR) filters, infinite impulse response (IIR) filters, and fast Fourier transform (FFT) for filtering and image processing applications.

Each Math block has the following capabilities:

- Supports 18x18 signed multiplications natively (a[17:0] x b[17:0])
- Supports dot product; the multiplier computes:

  $(A[8:0] \times B[17:9] + A[17:9] \times B[8:0]) \times 2^9$
- Built-in addition, subtraction, and accumulation units to combine multiplication results efficiently

In addition to the basic MACC function, DSP algorithms typically need small amounts of RAM for coefficients and larger RAMs for data storage. SmartFusion2 micro RAMs are ideally suited to serve the needs of coefficient storage while the large RAMs are used for data storage.

Microcontroller Subsystem (MSS)

The microcontroller subsystem (MSS) contains a high-performance integrated Cortex-M3 processor, running at up to 166 MHz. The MSS contains an 8 Kbyte instruction cache to provide low latency access to internal eNVM and external DDR memory. The MSS provides multiple interfacing options to the FPGA fabric in order to facilitate tight integration between the MSS and user logic in the fabric.

ARM Cortex-M3 Processor

The MSS uses the latest revision (r2p1) of the ARM Cortex-M3 processor. Microsemi's implementation includes the optional embedded trace macrocell (ETM) features for easier development and debug and the memory protection unit (MPU) for real-time operating system support.

Cache Controller

In order to minimize latency for instruction fetches when executing firmware out of off-chip DDR or on-chip eNVM, an 8 kbyte, 4-way set associative instruction cache is implemented. This provides zero wait state access for cache hits and is shared by both I and D Code buses of the Cortex-M3 processor. In the event of cache misses, cache lines are filled, replacing existing cache entries based on a least recently used (LRU) algorithm.

There is a configurable option available to operate the cache in a locked mode, whereby a fixed segment of code from either the DDR or eNVM is copied into the cache and locked there, so that it is not replaced when cache misses occur. This would be used for performance-critical code.

It is also possible to disable the cache altogether, which is desirable in systems requiring very deterministic execution times.

The cache is implemented with SEU tolerant latches.

DDR Bridge

The DDR bridge is a data bridge between four AHB bus masters and a single AXI bus slave. The DDR bridge accumulates AHB writes into write combining buffers prior to bursting out to external DDR memory. The DDR bridge also includes read combining buffers, allowing AHB masters to efficiently read data from the external DDR memory from a local buffer. The DDR bridge optimizes reads and writes from multiple masters to a single external DDR memory. Data coherency rules between the four masters and

the external DDR memory are implemented in hardware. The DDR Bridge contains three write combining / read buffers and one read buffer. All buffers within the DDR bridge are implemented with SEU tolerant latches and are not subject to the single event upsets (SEUs) that SRAM exhibits. SmartFusion2 devices implement three DDR bridges in the MSS, FDDR, and MDDR subsystems.

AHB Bus Matrix (ABM)

The AHB bus matrix (ABM) is a non-blocking, AHB-Lite multi-layer switch, supporting 10 master interfaces and 7 slave interfaces. The switch decodes access attempts by masters to various slaves, according to the memory map and security configurations. When multiple masters are attempting to access a particular slave simultaneously, an arbiter associated with that slave decides which master gains access, according to a configurable set of arbitration rules. These rules can be configured by the user to provide different usage patterns to each slave. For example, a number of consecutive access opportunities to the slave can be allocated to one particular master, to increase the likelihood of same type accesses (all reads or all writes), which makes more efficient usage of the bandwidth to the slave.

System Registers

The MSS System registers are implemented as an AHB slave on the AHB bus matrix. This means the Cortex-M3 processor or a soft master in the FPGA fabric may access the registers and therefore control the MSS. The System registers can be initialized by user-defined flash configuration bits on power-up. Each register also has a flash bit to enable write protecting the contents of the registers. This allows the MSS system configuration to be reliably fixed for a given application.

Fabric Interface Controller (FIC)

The FIC block provides two separate interfaces between the MSS and the FPGA fabric: the MSS Master (MM) and Fabric Master (FM). Each of these interfaces can be configured to operate as AHB-Lite or APB3. Depending on device density, there are up to two FIC blocks present in the MSS (FIC_0 and FIC_1).

Embedded SRAM (eSRAM)

The MSS contains two blocks of 32 KB eSRAM, giving a total of 64 KB. Having the eSRAM arranged as two separate blocks allows the user to take advantage of the Harvard architecture of the Cortex-M3 processor. For example, code could be located in one eSRAM, while data, such as the stack, could be located in the other.

The eSRAM is designed for Single Error Correct Double Error Detect (SECDED) protection. When SECDED is disabled, the SRAM usually used to store SECDED data may be reused as an extra 16 KB of eSRAM.

Embedded NVM (eNVM)

The MSS contains up to 512 KB of eNVM (64 bits wide). Accesses to the eNVM from the Cortex-M3 processor are cacheable.

DMA Engines

Two DMA engines are present in the MSS: high performance DMA and peripheral DMA.

High Performance DMA (HPDMA)

The high-performance DMA (HPDMA) engine provides efficient memory to memory data transfers between an external DDR memory and internal eSRAM. This engine has two separate AHB-Lite interfaces—one to the MDDR bridge and the other to the AHB bus matrix. All transfers by the HPDMA are full word transfers.

Peripheral DMA (PDMA)

The peripheral DMA engine (PDMA) is tuned for offloading byte-intensive operations, involving MSS peripherals, to and from the internal eSRAMs. Data transfers can also be targeted to user logic/RAM in the FPGA fabric.

APB Configuration Bus

On every SmartFusion2 device memory, an APB configuration bus is present to allow the user to initialize the SERDES ASIC blocks, the fabric DDR memory controller, and user instantiated peripherals in the FPGA fabric.

Peripherals

A large number of communications and general purpose peripherals are implemented in the MSS.

USB Controller

The MSS contains a high speed USB 2.0 On-The-Go (OTG) controller with the following features:

- Operates either as the function controller of a high-speed / full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions.
- Complies with the USB 2.0 standard for high-speed functions and with the *On-The-Go* supplement to the USB 2.0 specification.
- Supports OTG communications with one or more high-speed, full-speed, or low-speed devices.

TSE Ethernet MAC

The Triple Speed Ethernet (TSE) MAC supports IEEE 802.3 10/100/1000Mbps Ethernet operation. The following PHY interfaces are directly supported by the MAC:

- RMII
- GMII
- MII
- TBI

The Ethernet MAC hardware implements the following functions:

- 4 KB internal transmit FIFO and 8 KB internal receive FIFO
- IEEE 802.3X full-duplex flow control
- DMA of Ethernet frames between internal FIFOs and system memory (such as eSRAM or DDR)
- Cut-through operation
- SECDED protection on internal FIFOs

SGMII PHY Interface

SGMII mode is implemented by means of configuring the MAC for 10-bit interface (TBI) operation, allocating one of the high-speed serial channels to SGMII and by implementing custom logic in the fabric.
10 Gbps Ethernet

Support for 10 Gbps Ethernet is achieved by programming the SERDES interface to XAUI mode. In this mode, a soft 10G EMAC with XGMII interface can be directly connected to the SERDES. interface.

Communication Block (COMM_BLK)

The COMM block provides a UART-like communications channel between the MSS and the System Controller. System services are initiated through the COMM block. System services such as *Enter Flash*Freeze Mode* are initiated though this block.

SPI

The serial peripheral interface controller is compliant with the Motorola SPI, Texas Instruments synchronous serial, and National Semiconductor MICROWIRE™ formats. In addition, the SPI supports interfacing to large SPI flash and EEPROM devices by way of the slave protocol engine. The SPI controller supports both Master and Slave modes of operation.

The SPI controller embeds two 4×32 (depth × width) FIFOs for receive and transmit. These FIFOs are accessible through RX data and TX data registers. Writing to the TX data register causes the data to be written to the transmit FIFO. This is emptied by transmit logic. Similarly, reading from the RX data register causes data to be read from the receive FIFO.

Multi-Mode UART (MMUART)

SmartFusion2 devices contain two identical multi-mode universal asynchronous/synchronous receiver/transmitter (MMUART) peripherals that provide software compatibility with the popular 16550 device. They perform serial-to-parallel conversion on data originating from modems or other serial devices, and perform parallel-to-serial conversion on data from the Cortex-M3 processor to these devices.

The following are the main features supported:

- Fractional baud rate capability
- Asynchronous and synchronous operation
- Full programmable serial interface characteristics
  - Data width is programmable to 5, 6, 7, or 8 bits
  - Even, odd, or no-parity bit generation/detection
  - 1,1½, and 2 stop bit generation
- 9-bit address flag capability used for multidrop addressing topologies

I^2C

SmartFusion2 devices contain two identical master/slave I^2C peripherals that perform serial to-parallel conversion on data originating from serial devices, and perform parallel-to-serial conversion on data from the ARM Cortex-M3 processor, or any other bus master, to these devices. The following are the main features supported:

- I^2C v2.1
  - 100 Kbps
  - 400 Kbps
- Dual-slave addressing
- SMBus v2.0
- PMBus v1.1

Clock Sources: On-Chip Oscillators, PLLs, and CCCs

SmartFusion2 devices have two on-chip RC oscillators—a 1 MHz RC oscillator and a 50 MHz RC oscillator—and up to two main crystal oscillators (32 KHz–20 MHz). These are available to the user for generating clocks to the on-chip resources and the logic built on the FPGA fabric array. The second crystal oscillator available on the SmartFusion2 devices is dedicated for RTC clocking. These oscillators (except the RTC crystal oscillator) can be used in conjunction with the integrated user phase-locked loops (PLLs) and FAB_CCCs to generate clocks of varying frequency and phase. In addition to being available to the user, these oscillators are also used by the system controller, power-on reset circuitry, MSS during Flash*Freeze mode, and the RTC.

SmartFusion2 devices have up to eight fabric CCC (FAB_CCC) blocks and a dedicated PLL associated with each CCC to provide flexible clocking to the FPGA fabric portion of the device. The user has the freedom to use any of the eight PLLs and CCCs to generate the fabric clocks and the internal MSS clock from the base fabric clock (CLK_BASE). There is also a dedicated CCC block for the MSS (MSS_CCC) and an associated PLL (MPLL) for MSS clocking and de-skewing the CLK_BASE clock. The fabric alignment clock controller (FACC), part of the MSS CCC, is responsible for generating various aligned clocks required by the MSS for correct operation of the MSS blocks and synchornous communication with the user logic in the FPGA fabric.

High Speed Serial Interfaces

SERDES Interface

SmartFusion2 has up to four 5 Gbps SERDES transceivers, each supporting the following:

- 4 SERDES/PCS lanes
- The native SERDES interface facilitates implementation of Serial RapidIO (SRIO) in fabric or an SGMII interface for the Ethernet MAC in MSS

PCI Express (PCIe)

PCIe is a high speed, packet-based, point-to-point, low pin count, serial interconnect bus. The SmartFusion2 family has two hard high-speed serial interface blocks. Each SERDES block contains a PCIe (PCI Express) system block. The PCIe system is connected to the SERDES block and following are the main features supported:

- Supports x1, x2 and x4 lane configuration
- Endpoint configuration only
- PCI Express Base Specification Revision 2.0
- 2.5 and 5.0 Gbps compliant
- Embedded Receive (2 KB), Transmit (1 KB) and Retry (1 KB) buffer dual-port RAM implementation
- 256 bytes maximum payload size
- 64-bit AXI or 32-bit/64-bit AHBL Master and Slave interface to the application layer
- 32-bit APB interface to access configuration and status registers of PCIe system
- Up to 3 x 64 bit base address registers
- 1 virtual channel (VC)
- Intel's PIPE interface (8-bit/16-bit) to interface between the PHY MAC and PHY (SERDES)
- Fully compliant PHY PCS sub-layer (125/250 MHz)

XAUI/XGXS Extension

The XAUI/XGXS extension allows the user to implement a 10 Gbps (XGMII) Ethernet PHY interface by connecting the Ethernet MAC fabric interface through an appropriate soft IP block in the fabric.

High Speed Memory Interfaces: DDRx Memory Controllers

There are up to two DDR subsystems, MDDR (MSS DDR) and FDDR (Fabric DDR) present in SmartFusion2 devices. Each subsystem consists of a DDR controller, PHY and a wrapper. The MDDR has an interface from the MSS and fabric and FDDR provides an interface from the fabric.

The following are the main features supported by FDDR and MDDR:

- Support for LPDDR, DDR2, and DDR3 memories
- Support for SDRAM memories
- Simplified DDR command interface to standard AMBA AXI/AHB interface
- Up to 667 Mbps (333 MHz double data rate) performance
- Supports 1, 2, or 4 ranks of memory
- Supports different DRAM Bus width modes: x16, x18, x32, and x36
- Supports DRAM burst length of 2, 4, or 8 in full bus-width mode; supports DRAM burst length of 2, 4, 8, or 16 in half bus-width mode
- Supports memory densities up to 4 GB
- Supports a maximum of 8 memory banks
- SECDED enable/disable feature
- Embedded physical interface (PHY)
- Read and Write buffers in fully associative CAMs, configurable in powers of 2, up to 64 Reads plus 64 Writes
- Support for dynamically changing clock frequency while in self-refresh.
- Supports command reordering to optimize memory efficiency
- Supports data reordering, returning critical word first for each command

MDDR Subsystem

The MDDR subsystem has two interfaces to the DDR. One is an AXI 64-bit bus from the DDR bridge within the MSS. The other is a multiplexed interface from the FPGA fabric, which can be configured as either a single AXI 64-bit bus or two 32-bit AHB-Lite buses. There is also a 16-bit APB configuration bus, which is used to initialize the majority of the internal registers within the MDDR subsystem after reset. This APB configuration bus can be mastered by the MSS directly or by a master in the FPGA fabric.

FDDR Subsystem

The FDDR subsystem has one interface to the DDR. This is a multiplexed interface from the FPGA fabric, which can be configured as either a single AXI 64-bit bus or two 32-bit AHB-Lite buses. There is also a 16-bit APB configuration bus, which is used to initialize the majority of the internal registers within the FDDR subsystem after reset. This APB configuration bus can be mastered by the MSS directly or by a master in the FPGA fabric.

Microsemi

2 – SmartFusion2 DC and Switching Characteristics

General Specifications

Operating Conditions

Table 2-1 • **Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
T_J	Junction temperature	Commercial	0	25	85	°C	
	Junction temperature	Industrial	–40	25	100	°C	
VDD	DC core supply voltage		1.14	1.2	1.26	V	
VPP	Power supply for charge pumps (for normal opeartion and programming)	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
PLLx_VDDA	Analog power supply for PLL0 to PLL5	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
PLL_PCIE_x_VDDA	Auxiliary power supply voltage by core to macro	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
PLL_MDDR_VDDA	Analog power supply for PLL MDDR	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
PLL_FDDR_VDDA	Analog power supply for PLL FDDR	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
PCIExVDD	PCIe/PCS power supply		1.14	1.2	1.26	V	
PCIExVDDIO[L/R]	Tx/Rx analog I/O voltage supply		1.14	1.2	1.26	V	
PCIExVDDPLL[L/R]	Anlog power supply for SERDES PLL of PCIe		2.375	2.5	2.625	V	
VDDIx	1.2 V DC supply voltage		1.14	1.2	1.26	V	
	1.5 V DC supply voltage		1.425	1.5	1.575	V	
	1.8 V DC supply voltage		1.71	1.8	1.89	V	
	2.5 V DC supply voltage		2.375	2.5	2.625	V	
	3.3 V DC supply voltage		3.15	3.3	3.45	V	
	LVDS differential I/O		2.375	2.5	3.45	V	
	B-LVDS, M-LVDS, Mini-LVDS, RSDS differential I/O		2.375	2.5	2.625	V	
	LVPECL differential I/O		3.15	3.3	3.45	V	
VREFx	Reference voltage supply for FDDR (bank 0) and MDDR (bank 5)		0.49 * VDDI0	0.5 * VDDI0	0.51 * VDDI0	V	
VCCENVM	Embedded nonvolatile memory supply	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	

Table 2-2 • **FPGA and Embedded Flash Programming, Storage and Operating Limits**

Product Grade	Storage Temperature	Programming Temperature	Element	Grade Programming Cycles	Retention
Commercial	Min. T_J = 0°C Max. T_J = 85°C	Min. T_J = 0°C Max. T_J = 85°C	FPGA	500	20 years
		Min. T_J = 0°C Max. T_J = 85°C	Embedded Flash	< 1,000	20 years
				< 10,000	10 years
Industrial	Min. T_J = –40°C Max. T_J = 100°C	Min. T_J = 0°C Max. T_J = 85°C	FPGA	500	20 years
		Min. T_J = –40°C Max. T_J = 100°C	Embedded Flash	< 1,000	20 years
				< 10,000	10 years

Power Supply Sequencing and Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every SmartFusion2 SoC FPGA. These circuits ensure easy transition from powered-off state to powered-up state of the device. The SmartFusion2 system controller is responsible for systematic power-on reset whenever the device is powered on or reset. All the I/Os are held in a high-impedance state by the system controller until all power supplies are at their required levels and the system controller has completed the reset sequence. The power-on reset circuitry in SmartFusion2 devices requires the VDD supply to ramp at a predefined rate. Four ramp rate options are available during design generation: 50 µs, 100 µs, 1 ms, and 100 ms.

Thermal Characteristics

Introduction

The temperature variable in the SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - \theta_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

where

θ_{JA} = Junction-to-air thermal resistance
θ_{JB} = Junction-to-board thermal resistance
θ_{JC} = Junction-to-case thermal resistance
T_J = Junction temperature
T_A = Ambient temperature
T_B = Board temperature (measured 1.0 mm away from the package edge)
T_C = Case temperature
P = Total power dissipated by the device

Table 2-3 • **Package Thermal Resistance**

Product	θ_{JA}			θ_{JC}	θ_{JB}	Units
	Still Air	1.0 m/s	2.5 m/s			
M2S050T-FG896	14.7	12.5	10.9	7.2	4.9	°C/W

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

The maximum power dissipation allowed is calculated using EQ 4.

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 100°C. EQ 5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2S050T-FG896 package at commercial temperature and in still air, where

θ_{JA} = 14.7°C/W (taken from Table 2-3 on page 2-3).

T_A = 85°C

$$\text{Maximum Power Allowed} = \frac{100°C - 85°C}{14.7°C/W} = 1.088\ W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

Calculating Power Dissipation

Quiescent Supply Current

Table 2-4 • **Quiescent Supply Current Characteristics**

Parameter	Modes	M2S050T VDD = 1.2 V	Units
IDC1	Active mode	7.5	mA
IDC2	Standby mode	7.5	mA
IDC3	Flash*Freeze mode	0.387	mA

I/O Power

Table 2-5 • **Summary of I/O Input Buffer Power (per pin) Using Default Software Setting with Technology Selected**

	MSIO I/O Bank		MSIOD I/O Bank		DDR I/O Bank		
	Static Power PDC8 (mW)	Dynamic Power PAC9 (µW/MHz)	Static Power PDC8 (mW)	Dynamic Power PAC9 (µW/MHz)	Static Power PDC8 (mW)	Dynamic Power PAC9 (µW/MHz)	Notes
Single Ended I/O Standards							
1.2 V LVCMOS (JESD8-11)	0.00	11.72	0.00	11.72	0.00	11.72	
1.5 V LVCMOS (JESD8-11)	0.00	8.32	0.00	8.32	0.00	8.32	
1.8 V LVCMOS	0.00	10.69	0.00	10.69	0.00	10.69	
2.5 V LVCMOS	0.00	4.14	0.00	4.14	0.00	4.14	
3.3 V LVTTL / 3.3 V LVCMOS	0.00	5.47	–	–	–	–	
3.3 V PCI/PCIX	0.00	1.82	–	–	–	–	
Memory Interface and Voltage Reference Standard							
HSTL 1.5 V	2.21	5.57	2.21	5.57	2.21	5.57	
HSTL 1.5 V – True differential	1.25	47.38	1.25	47.38	1.25	47.38	
SSTL2/DDR	10.02	42.68	10.02	42.68	10.02	42.68	
SSTL2/DDR – True differential	4.39	12.35	4.39	12.35	4.39	12.35	
SSTL18/DDR2	3.88	3.81	3.88	3.81	3.88	3.81	
SSTL18/DDR2 – True differential	1.97	56.80	1.97	56.80	1.97	56.80	
SSTL15/DDR3	–	–	–	–	2.20	18.00	
SSTL15/DDR3 – True differential	–	–	–	–	1.23	46.81	
LPDDR	–	–	–	–	3.88	4.46	
LPDDR – True differential	–	–	–	–	1.97	5.08	
Differential Standards							
LVDS	5.74	17.65	5.74	17.65	–	–	
B-LVDS	5.65	8.76	5.65	8.76	–	–	
M-LVDS	5.65	8.76	5.65	8.76	–	–	
RSDS	5.74	0.93	5.74	0.93	–	–	
Mini-LVDS	TBD	TBD	TBD	TBD	–	–	
LVPECL	TBD	TBD	–	–	–	–	

Table 2-6 • **Summary of I/O Output Buffer Power (per pin)**
Default Software Setting with Technology selected

	MSIO I/O Bank		MSIOD I/O Bank		DDR I/O Bank		
	Static Power	Dynamic Power	Static Power	Dynamic Power	Static Power	Dynamic Power	
	PDC9 (mW)	PAC9 (µW/MHz)	PDC9 (mW)	PAC9 (µW/MHz)	PDC9 (mW)	PAC9 (µW/MHz)	Notes
Single Ended I/O Standards							
1.2 V LVCMOS (JESD8-11)	0.00	16.74	0.00	16.74	0.00	16.74	
1.5 V LVCMOS (JESD8-11)	0.00	26.31	0.00	26.31	0.00	26.31	
1.8 V LVCMOS	0.00	38.23	0.00	38.23	0.00	38.23	
2.5 V LVCMOS	0.00	75.35	0.00	75.35	0.00	75.35	
3.3 V LVTTL / 3.3 V LVCMOS	0.00	137.04	–	–	–	–	
3.3 V PCI/PCIX	0.00	TBD	–	–	–	–	
Memory Interface and Voltage Reference Standard							
HSTL 1.5 V Class I	6.45	60.17	6.45	60.17	6.45	60.17	
HSTL 1.5 V Class I – True differential	12.90	80.30	12.90	80.30	12.90	80.30	
HSTL 1.5 V Class II	–	–	–	–	12.56	104.21	
HSTL 1.5 V Class II – True differential	–	–	–	–	25.08	87.09	
SSTL2 Class I / DDR Reduced Drive	18.12	76.44	18.12	76.44	18.12	76.44	
SSTL2 Class I / DDR Reduced Drive – True differential	36.16	218.81	36.16	218.81	36.16	218.81	
SSTL2 Class II / DDR Full Drive	37.20	317.68	37.20	317.68	37.20	317.68	
SSTL2 Class II / DDR Full Drive – True differential	74.41	110.90	74.41	110.90	74.41	110.90	
SSTL18 Class I / DDR2 Reduced Drive	9.06	15.09	9.06	15.09	9.06	15.09	
SSTL18 Class I / DDR2 Reduced Drive – True differential	18.09	56.33	18.09	56.33	18.09	56.33	
SSTL18 Class II / DDR2 Full Drive	18.63	170.66	18.63	170.66	18.63	170.66	
SSTL18 Class II / DDR2 Full Drive – True differential	37.28	9.12	37.28	9.12	37.28	9.12	
SSTL15 Class I / DDR3 Reduced Drive	–	–	–	–	11.28	62.13	
SSTL15 Class I / DDR3 Reduced Drive – True differential	–	–	–	–	22.52	131.80	
SSTL15 Class II / DDR3 Full Drive	–	–	–	–	12.15	47.65	
SSTL15 Class II / DDR3 Full Drive – True differential	–	–	–	–	24.29	142.98	
LPDDR Reduced Drive	–	–	–	–	18.62	331.33	
LPDDR Reduced Drive – True differential	–	–	–	–	37.28	9.12	
LPDDR Full Drive	–	–	–	–	9.06	46.40	
LPDDR Full Drive – True differential	–	–	–	–	18.09	56.33	
Differential Standards							
LVDS	13.48	63.84	13.48	63.84	–	–	
B-LVDS	18.37	30.73	–	–	–	–	
M-LVDS	18.37	30.73	–	–	–	–	
RSDS	8.50	82.76	8.50	82.76	–	–	
Mini-LVDS	TBD	TBD	TBD	TBD	–	–	

Power Consumption of Various Internal Resources

Table 2-7 • **Different Components Contributing to Dynamic Power Consumption in SmartFusion2 Devices**

Param.	Definition	Power Supply		Device	Units	Notes
		Name	Domain	M2S050T		
PAC1	Global Clock contribution of a GB	VDD	1.2 V	3.50	µW/MHz	
PAC2	Global Clock contribution of a RGB	VDD	1.2 V	0.87	µW/MHz	
PAC3	Global Clock contribution of a sequential module.	VDD	1.2 V	0.02	µW/MHz	
PAC4	Clock contribution of a sequential module.	VDD	1.2 V	0.01	µW/MHz	
PAC5	Data contribution of a sequential module.	VDD	1.2 V	0.06965	µW/MHz	
PAC6	Average contribution of a combinatorial module.	VDD	1.2 V	0.709	µW/MHz	
PAC7	Average contribution of a combinatorial module with carry chain.	VDD	1.2 V	0.821657	µW/MHz	
PAC8	Average contribution of a routing net.	VDD	1.2 V	0.87	µW/MHz	
PAC9	Contribution of an I/O input pin (standard dependent)	VDDI	Table 2-5 on page 2-5	Table 2-5 on page 2-5	–	
PAC10	Contribution of an I/O output pin (standard dependent)	VDDI	Table 2-6 on page 2-6	Table 2-6 on page 2-6	–	
PAC11	Average contribution of a uSRAM block during a read operation.	VDD	1.2 V	2.39	µW/MHz	
PAC12	Average contribution of a uSRAM block during a write operation.	VDD	1.2 V	7.01	µW/MHz	
PAC13	Average contribution of a LSRAM block during a read operation.	VDD	1.2 V	19.85	µW/MHz	
PAC14	Average contribution of a LSRAM block during a write operation.	VDD	1.2 V	24.85	µW/MHz	
PAC15	CCC contribution	VDD	1.2 V	8.00	mW	
PAC16	Main Crystal Oscillator contribution	VDD	1.2 V	55.51	µW/MHz	
PAC17	1 MHz RC Oscillator contribution	VDD	1.2 V	37.2	mW	
PAC18	50 MHz RC Oscillator contribution	VDD	1.2 V	7.30	mW	
PAC19	Math Block contribution	VDD	1.2 V	TBD	mW	
PAC20	MSS Dynamic Power Contribution with MDDR/USB/Ethernet OFF, Clock Frequency = 100 MHz	VDD	1.2 V	91.986	mW	1
PAC21	MSS Dynamic Power Contribution with USB/Ethernet OFF, Clock Frequency = 100 MHz, MDDR mode–MSS Bridge	VDD	1.2 V	137.43	mW	1

Notes:

1. *For a different use of MSS peripherals and resources, refer to SmartPower.*
2. *Dynamic power contribution of FDDR does not include the DDRIO power. Use I/O power for calculation of I/O power. For a different use of the FDDR, refer to SmartPower.*
3. *For a different use of the SERDES block, refer to SmartPower.*

Table 2-7 • Different Components Contributing to Dynamic Power Consumption in SmartFusion2 Devices (continued)

Param.	Definition	Power Supply		Device	Units	Notes
		Name	Domain	M2S050T		
PAC22	FDDR Dynamic Power Contribution with frequency = 100 MHz, DDR Clock Multiplier = 2	VDD	1.2 V	108.81	mW	2
PAC23	SERDES Dynamic Power Contribution configured as PCIe_GEN1 with 1 Lane at 125 MHz	VDD	1.2 V	91.70	mW	3

Notes:

1. *For a different use of MSS peripherals and resources, refer to SmartPower.*
2. *Dynamic power contribution of FDDR does not include the DDRIO power. Use I/O power for calculation of I/O power. For a different use of the FDDR, refer to SmartPower.*
3. *For a different use of the SERDES block, refer to SmartPower.*

Table 2-8 • Different Components Contributing to the Static Power Consumption in SmartFusion Devices

Param.	Definition	Power Supply			Device	Units
		Name	Domain	Mode	M2S050T	
PDC1	Core static power contribution in Active Operating mode	VDD	1.2 V	Active	9.000	mW
PDC2	Core static power contribution in Standby Operating mode	VDD	1.2 V	Standby	9.000	mW
PDC3	Core static power contribution in Flash*Freeze Operating mode	VDD	1.2 V	Flash*Freeze	0.465	mW
PDC4	LSRAM static power contribution in Flash*Freeze configured in "Sleep" State	VDD	1.2 V	Flash*Freeze	1.250	uW
PDC5	LSRAM static power contribution in Flash*Freeze configured in "Suspended" State	VDD	1.2 V	Flash*Freeze	10.140	uW
PDC6	USRAM static power contribution in Flash*Freeze configured in "Sleep" State	VDD	1.2 V	Flash*Freeze	0.500	uW
PDC7	USRAM static power contribution in Flash*Freeze configured in "Suspend" State	VDD	1.2 V	Flash*Freeze	4.970	uW
PDC8	I/O Input static power contribution in Active Operating mode	VDDI	VDDI	Active	See Table 2-5 on page 2-5	uW
PDC9	I/O Output static power contribution in Active Operating mode	VDDI	VDDI	Active	See Table 2-6 on page 2-6	uW

Power Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero IDE software. The power calculation methodology described below uses the following variables:

- The number of PLLs/CCCs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as the logic module—guidelines are provided in Table 2-9 on page 2-13.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-10 on page 2-13.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-10 on page 2-13.

The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

Active, Standby and Flash*Freeze Mode

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

Active Mode

$P_{STAT} = PDC1 + (N_{INPUTS} * PDC7) + (N_{OUTPUTS} * PDC8) + (N_{PLLS} * PDC9)$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{PLLS} is the number of PLLs available in the device.

Standby Mode

$P_{STAT} = PDC2$

Flash*Freeze Mode

P_{STAT} = PDC3 + PDC4 + PDC 6 when both LSRAM and uSRAM are configured in Sleep state

P_{STAT} = PDC3 + PDC5 + PDC 7 when both LSRAM and uSRAM are configured in Suspend state

Total Dynamic Power Consumption—P_{DYN}

Active Mode

$P_{DYN} = P_{CLOCK} + P_{LOGIC} + P_{IOS} + P_{MEMORY} + P_{CCC} + P_{MATH} + P_{MSS} + P_{FDDR} + P_{SERDES}$

Flash*Freeze Mode

$P_{DYN} = PDC3 + P_{MEMORY}$

Standby Mode

$P_{DYN} = PDC2$

Global Clock Dynamic Power Contribution—P_{CLOCK}

Active Mode

P_{CLOCK} = (PAC1 + N_{ROWS} * PAC2 + $N_{S\text{-}CELL}$ * PAC3) * F_{CLK}

Where:

N_{ROWS} is the number of global rows used in the design—guidelines are provided in the "Fabric Global Routing Resources" chapter of the *SmartFusion2 FPGA Fabric Architecture User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of Registers used in the design.

Standby and Flash*Freeze Mode

P_{CLOCK} = 0 W

Logic Module Dynamic Power Contribution—P_{LOGIC}

Active Mode

P_{LOGIC} = P_{SEQ} + P_{LUT} + P_{NET}

Standby and Flash*Freeze Mode

P_{LOGIC} = 0 W

Registers Dynamic Power Contribution—P_{SEQ}

P_{SEQ} = $N_{S\text{-}CELL}$ * PAC4 * F_{CLK} + $N_{S\text{-}CELL}$ * PAC5 * F_{CLK} * α1/2

Where:

$N_{S\text{-}CELL}$ is the number of registers used in the design.

α1 is the toggle rate of the LUT outputs—guidelines are provided in Table 2-9 on page 2-13.

F_{CLK} is the global clock signal frequency.

LUTs Dynamic Power Contribution—P_{LUT}

P_{LUT}= (N_{LUT} * PAC6 + N_{CC} * PAC7) * F_{CLK} * α1/2

Where:

N_{LUT} is the number of LUT-4 used as combinatorial modules in the design.

N_{CC} is the number of LUT-4 used with the carry chain in the design.

α1 is the toggle rate of the LUT outputs—guidelines are provided in Table 2-9 on page 2-13.

F_{CLK} is the global clock signal frequency.

Routing Net Dynamic Power Contribution—P_{NET}

P_{NET} = ($N_{S\text{-}CELL}$ + N_{LUT} + N_{CC}) * (α1 / 2) * PAC8 * F_{CLK}

Where:

$N_{S\text{-}CELL}$ is the number of registers used in the design.

N_{LUT} is the number of LUT-4 used as combinatorial modules in the design.

N_{CC} is the number of LUT-4 used with the carry chain in the design.

α1 is the toggle rate of the LUT outputs—guidelines are provided in Table 2-9 on page 2-13.

F_{CLK} is the global clock signal frequency.

I/O Dynamic Contribution—P_{IOS}

Active Mode

P_{IOS} = P_{INPUTS} + $P_{OUTPUTS}$

Standby and Flash*Freeze Mode

P_{IOS} = 0 W

I/O Input Buffer Dynamic Contribution—P_{INPUTS}

PINPUTS = NINPUTS * (α2 / 2) * β1 * PAC9 * FCLK

Where:

N_{INPUTS} is the number of I/O input buffers used in the design.

α2 is the I/O buffer toggle rate—guidelines are provided in Table 2-9 on page 2-13.

β1 is the I/O buffer enable rate—guidelines are provided in Table 2-10 on page 2-13.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Dynamic Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha2 / 2) * \beta1 * PAC10 * F_{CLK}$

Where:

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α2 is the I/O buffer toggle rate—guidelines are provided in Table 2-9 on page 2-13.

β1 is the I/O buffer enable rate—guidelines are provided in Table 2-10 on page 2-13.

F_{CLK} is the global clock signal frequency.

FPGA Fabric SRAM Dynamic Contribution—P_{MEMORY}

Active Mode

$P_{MEMORY} = P_{USRAM} + P_{LSRAM}$

Flash*Freeze Mode

P_{MEMORY} = PDC4 + PDC6 for RAM in "Sleep" State

P_{MEMORY} = PDC5 + PDC7 for RAM in "Suspend" State

Standby Mode

P_{MEMORY} = 0 W

FPGA Fabric uSRAM Dynamic Contribution—P_{USRAM}

$P_{uSRAM} = (N_{uSRAM\_BLK} * PAC13 * \beta2 * F_{uSRAM\text{-}RDCLK}) + (N_{uSRAM\_BLK} * PAC14 * \beta3 * F_{uSRAM\text{-}WRTCLK})$

Where:

Nu_{SRAM_BLK} is the number of uRAM blocks used in the design.

$F_{uSRAM\text{-}RDCLK}$ is the uSRAM memory read clock frequency.

$F_{uSRAM\text{-}WRTCLK}$ is the uSRAM memory write clock frequency.

β2 is the RAM enable rate for read operations—guidelines are provided in Table 2-10 on page 2-13.

β3 the RAM enable rate for write operations—guidelines are provided in Table 2-10 on page 2-13.

FPGA Fabric Large SRAM Dynamic Contribution—P_{LSRAM}

$P_{LSRAM} = (N_{LSRAM\_BLK} * PAC13 * \beta2 * F_{LSRAM\text{-}RDCLK}) + (N_{LSRAM\_BLK} * PAC14 * \beta3 * F_{LSRAM\text{-}WRTCLK})$

Where:

N_{LSRAM_BLK} is the number of Large SRAM blocks used in the design.

$F_{LSRAM\text{-}RDCLK}$ is the Large SRAM memory read clock frequency.

$F_{LSRAM\text{-}WRTCLK}$ is the Large SRAM memory write clock frequency.

β2 is the RAM enable rate for read operations—guidelines are provided in Table 2-10 on page 2-13.

β3 the RAM enable rate for write operations—guidelines are provided in Table 2-10 on page 2-13.

PLL/CCC Dynamic Contribution—P_{PLL}

Active Mode

P_{PLL} = PAC15

Flash*Freeze/Standby Mode

P_{PLL} = 0 W

External Main Crystal Oscillator Dynamic Contribution—$P_{XTL-OSC}$

Active Mode

$P_{XTL-OSC}$ = PAC16 * F_{CLK}

Where:

F_{CLK} is the output frequency of the oscillator.

Flash*Freeze/Standby Mode

$P_{XTL-OSC}$ = 0 W

On-Chip 25/50MHz RC Oscillator Dynamic Contribution—$P_{50RC-OSC}$

Active Mode/Standby Mode

$P_{50RC-OSC}$ = 0 W

Flash*Freeze

When used by MSS:

$P_{50RC-OSC}$ = PAC18

When not used by MSS:

$P_{50RC-OSC}$ = 0 W

Math Block Dynamic Power Contribution—P_{MATH}

Active Mode

P_{MATH} = PAC19 * N_{MATH_BLK} * $F_{MATHCLK}$

N_{MATH_BLK} is the number of math blocks used in the design.

$F_{MATHCLK}$ is the math block clock frequency.

Flash*Freeze/Standby Mode

P_{MATH} = 0 W

Microcontroller Subsystem Dynamic Power Contribution—P_{MSS}

Active Mode

With MDDR OFF:

P_{MSS} = PAC20

With MDDR ON:

P_{MSS} = PAC21

Flash*Freeze/Standby Mode

P_{MSS} = 0 W

FDDR Dynamic Power Contribution—P_{FDDR}

Active Mode

PFDDR = PAC22

FDDR Dynamic power contributions do not include the power contributions of the DDR I/O. This should be accounted for in the I/O power calculations.

Flash*Freeze/Standby Mode

P_{FDDR} = 0 W

SERDES Contribution—P_{SERDES}

Active Mode

P_{SERDES} = PAC23

Flash*Freeze/Standby Mode

P_{SERDES} = 0 W

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that the net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100%, as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . 0.78125%) / 8.

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When non-tristate output buffers are used, the enable rate should be 100%.

Table 2-9 • **Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α1	Toggle rate of Logic Module outputs	10%
α2	I/O buffer toggle rate	10%

Table 2-10 • **Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β1	I/O output buffer enable rate	Toggle rate of the logic driving the output buffer
β2	FPGA fabric SRAM enable rate for read operations	12.50%
β3	FPGA fabric SRAM enable rate for write operations	12.50%
β4	eNVM enable rate for read operations	< 5%

Average Fabric Temperature and Voltage Derating Factors

***Table 2-11* • Average Temperature and Voltage Derating Factors for Fabric Timing Delays (normalized to T_J = 100°C, worst-case VDD = 1.14 V)**

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.14	TBD	TBD	TBD	TBD	TBD	TBD
1.2	TBD	TBD	TBD	TBD	TBD	TBD
1.26	TBD	TBD	TBD	TBD	TBD	TBD

Timing Model

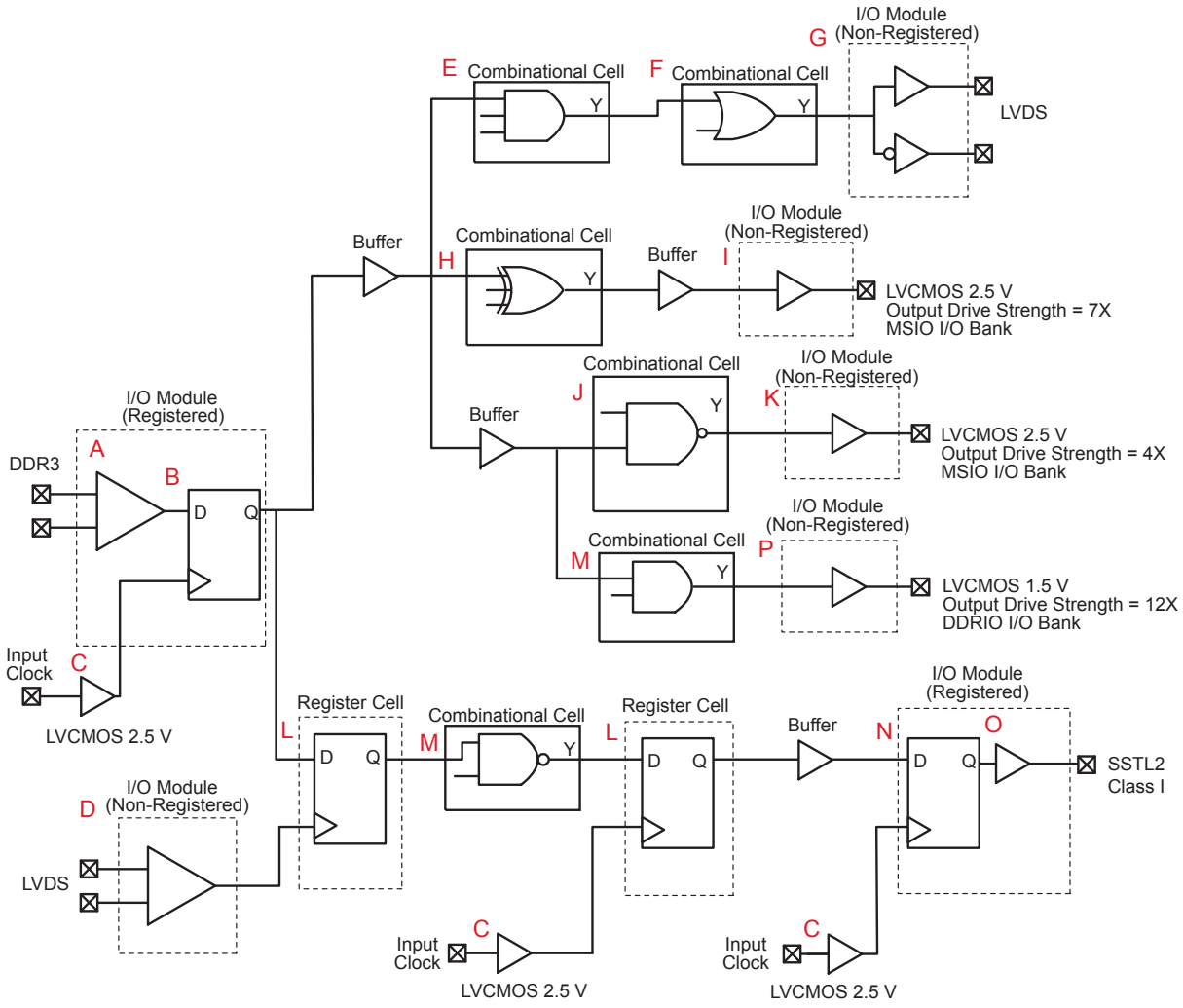


Figure 2-1 • **Timing Model**

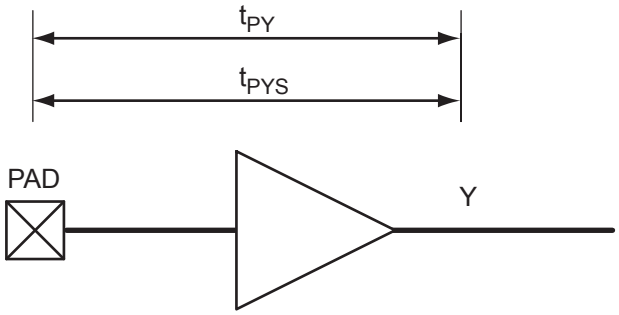
***Table 2-12* • Timing Model Parameters**

Index	Parameter	Description	Value	Units	Notes
A	tPY	Propagation Delay of DDR3 Receiver	TBD	ns	Table 2-51 on page 2-51
B	tICLKQ	Clock-to-Q of the Input Data Register	TBD	ns	Table 2-73 on page 2-65
	tISUD	Setup Time of the Input Data Register	TBD	ns	Table 2-73 on page 2-65
C	tRCKH	Input High Delay for Global Clock	TBD	ns	Table 2-79 on page 2-76
	tRCKL	Input Low Delay for Global Clock	TBD	ns	Table 2-79 on page 2-76
D	tPY	Input Propagation Delay of LVDS Receiver	TBD	ns	Table 2-57 on page 2-55
E	tDP	Propagation Delay of a three input AND Gate	0.22	ns	Table 2-77 on page 2-73
F	tDP	Propagation Delay of a OR Gate	0.172	ns	Table 2-77 on page 2-73
G	tDP	Propagation Delay of a LVDS Transmitter	TBD	ns	Table 2-58 on page 2-55
H	tDP	Propagation Delay of a three input XOR Gate	0.24	ns	Table 2-77 on page 2-73
I	tDP	Propagation Delay of LVCMOS 2.5 V Transmitter, Drive strength of 8X on the MSIO Bank	2.481	ns	Table 2-25 on page 2-25
J	tDP	Propagation Delay of a two input MUX gate	0.172	ns	Table 2-77 on page 2-73
K	tDP	Propagation Delay of LVCMOS 2.5 V Transmitter, Drive strength of 4X on the MSIO Bank	2.382	ns	Table 2-25 on page 2-25
L	tCLKQ	Clock-to-Q of the Data Register	0.114	ns	Table 2-78 on page 2-75
	tSUD	Setup Time of the Data Register	0.267	ns	Table 2-78 on page 2-75
M	tDP	Propagation Delay of a two input AND gate	0.172	ns	Table 2-77 on page 2-73
N	tOCLKQ	Clock-to-Q of the Output Data Register	TBD	ns	Table 2-73 on page 2-65
	tOSUD	Setup Time of the Output Data Register	TBD	ns	Table 2-73 on page 2-65
O	tDP	Propagation Delay of SSTL2, Class I Transmitter on the MSIO Bank	TBD	ns	Table 2-46 on page 2-44
P	tDP	Propagation Delay of LVCMOS 1.5 V Transmitter, Drive strength of 15X on the DDRIO Bank	TBD	ns	Table 2-33 on page 2-31

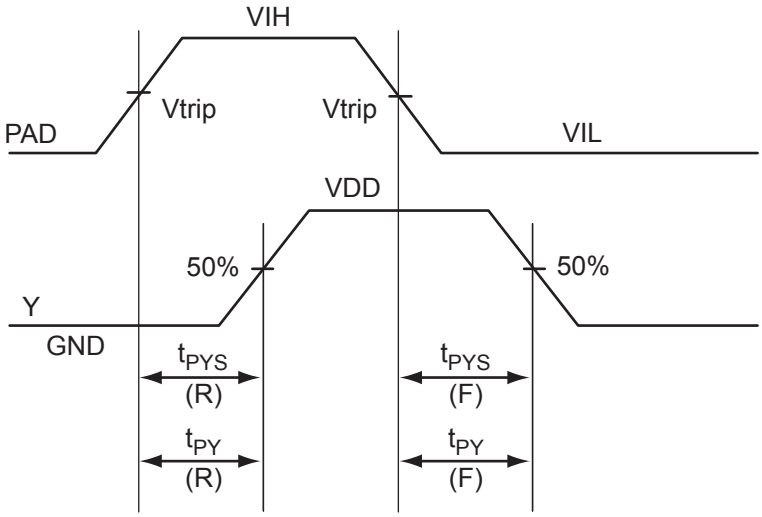
User I/O Characteristics

There are three types of I/Os supported in the SmartFusion2 FPGA Family: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the "I/Os" section of the *SmartFusion2 FPGA Fabric Architecture User's Guide*.

Input Buffer and AC Loading

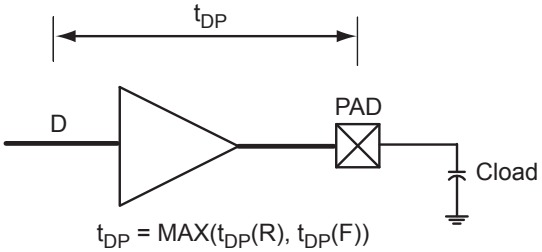


$t_{PY} = MAX(t_{PY}(R), t_{PY}(F))$
$t_{DIN} = MAX(t_{DIN}(R), t_{DIN}(F))$



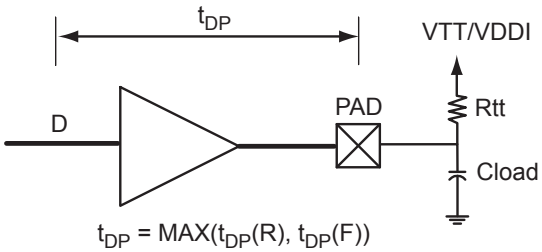
Output Buffer and AC Loading

Single-Ended I/O Test Setup



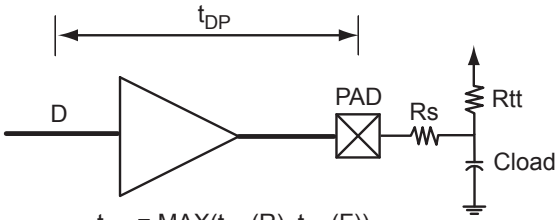
$t_{DP} = MAX(t_{DP}(R), t_{DP}(F))$

HSTL/PCI Test Setup



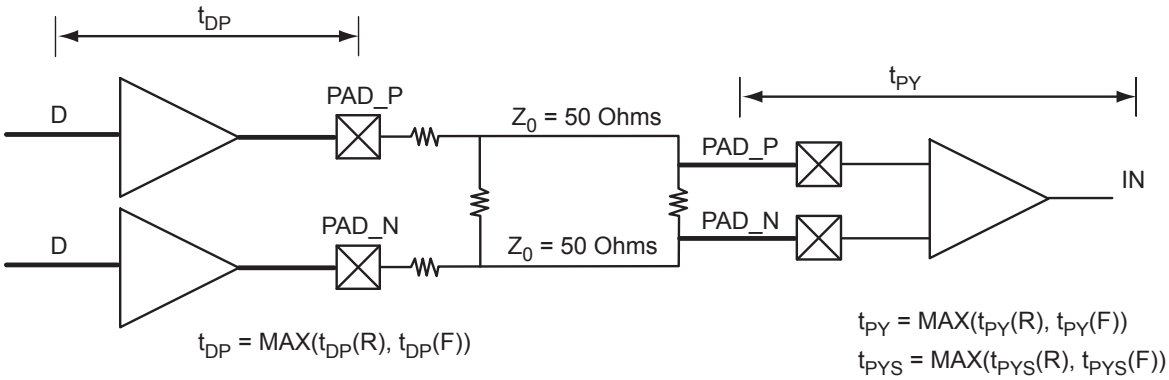
$t_{DP} = MAX(t_{DP}(R), t_{DP}(F))$

Voltage-Referenced, Singled-Ended I/O Test Setup



$t_{DP} = MAX(t_{DP}(R), t_{DP}(F))$

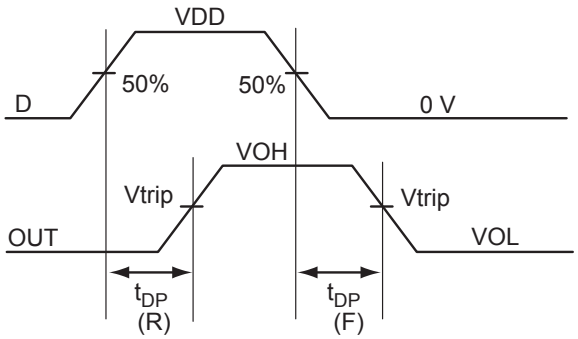
Differential I/O Test Setup



$t_{DP} = MAX(t_{DP}(R), t_{DP}(F))$

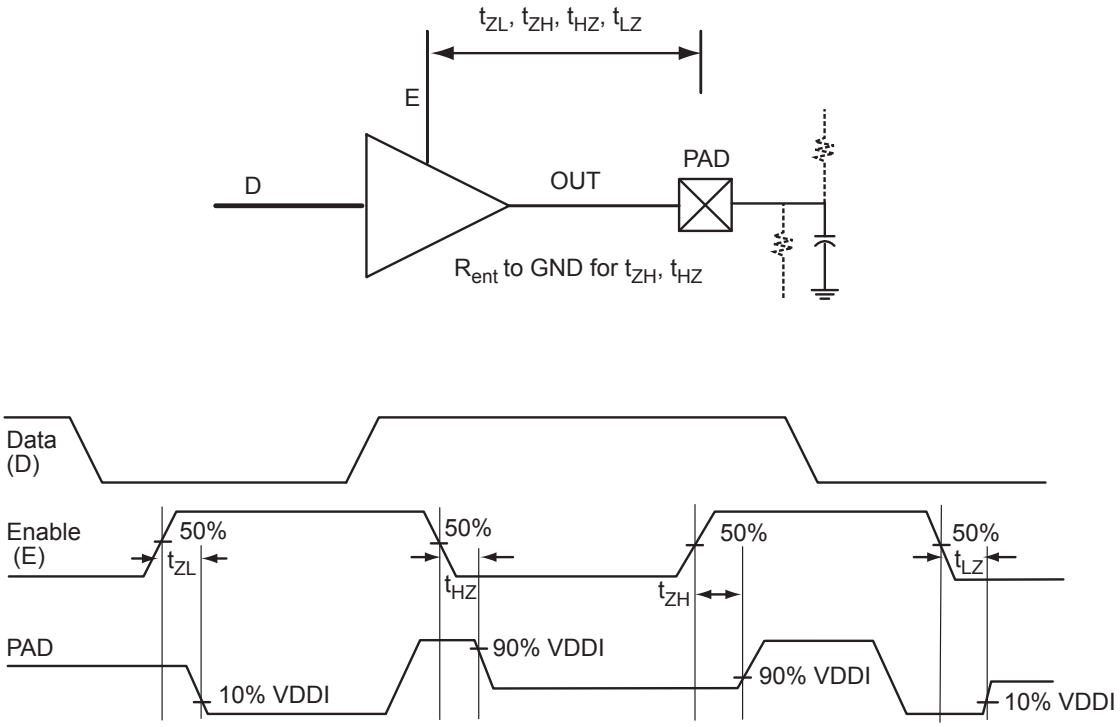
$t_{PY} = MAX(t_{PY}(R), t_{PY}(F))$

$t_{PYS} = MAX(t_{PYS}(R), t_{PYS}(F))$



Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The methodology of characterization is illustrated by the enable path test point below.



Detailed I/O Characteristics

***Table 2-13* • Input Capacitance**

Symbol	Definition	Conditions	Minimum	Maximum	Units
C_{IN}	Input capacitance	VIN = 0, f = 1.0 MHz	–	10	pF

***Table 2-14* • I/O Weak Pull-Up/Pull-Down Resistances for DDRIO I/O Bank Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level**

VDDI Domain	DDRIO I/O Bank				Notes
	R(WEAK PULL-UP) at VOH (Ω)		R(WEAK PULL-DOWN) at VOL (Ω)		
	Min.	Max.	Min.	Max.	
3.3 V	N/A	N/A	N/A	N/A	–
2.5 V	10.6 K	17.3 K	10.5 K	18.1 K	1, 2
1.8 V	1.11 K	19.3 K	11.2 K	20.9 K	1, 2
1.5 V	10 K	13.4 K	9.99 K	13.4 K	1, 2
1.2 V	10.3 K	14.5 K	10.3 K	14.7 K	1, 2

Notes:

1. *R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX)*
2. *R(WEAK PULL-UP) = (VDDImax - VOHspec)/I(WEAK PULL-UP MIN)*

***Table 2-15* • I/O Weak Pull-Up/Pull-Down Resistances for MSIO I/O Bank Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level**

VDDI Domain	MSIO IO Bank				Notes
	R(WEAK PULL-UP) at VOH (Ω)		R(WEAK PULL-DOWN) at VOL (Ω)		
	Min.	Max.	Min.	Max.	
3.3 V	9.9 K	14.7 K	10.1 K	15.3 K	–
2.5 V	10.1 K	15.1 K	10.1 K	15.7 K	1, 2
1.8 V	10.4 K	16.2 K	10.4 K	17.3 K	1, 2
1.5 V	10.7 K	17.3 K	10.8 K	18.9 K	1, 2
1.2 V	11.3 K	19.7 K	11.5 K	22.7 K	1, 2

Notes:

1. *R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX)*
2. *R(WEAK PULL-UP) = (VDDImax - VOHspec)/I(WEAK PULL-UP MIN)*

Table 2-16 • I/O Weak Pull-Up/Pull-Down Resistances for MSIOD I/O Bank
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level

VDDI Domain	R(WEAK PULL-UP) at VOH (Ω)		R(WEAK PULL-DOWN) at VOL (Ω)		Notes
	Min.	Max.	Min.	Max.	
3.3 V	N/A	N/A	N/A	N/A	–
2.5 V	9.6 K	14.1 K	9.5 K	13.9 K	1, 2
1.8 V	9.7 K	14.7 K	9.7 K	14.5 K	1, 2
1.5 V	9.9 K	15.3 K	9.8 K	15 K	1, 2
1.2 V	10.3 K	16.7 K	10 K	16.2 K	1, 2

Notes:

1. *R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX)*
2. *R(WEAK PULL-UP) = (VDDImax - VOHspec)/I(WEAK PULL-UP MIN)*

Table 2-17 • Schmitt Trigger Input Hysteresis
Hysteresis Voltage Value for Schmitt Trigger Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typical, unless otherwise noted)
3.3 V LVTTL / LVCMOS / PCI / PCI-X	0.05 × VDDI (worst-case)
2.5 V LVCMOS	0.05 × VDDI (worst-case)
1.8 V LVCMOS	0.1 × VDDI (worst-case)
1.5 V LVCMOS	60 mV
1.2 V LVCMOS	20 mV

Single-Ended I/O Standards

Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in SmartFusion2 SoC FPGAs are LVCMOS12, LVCMOS15, LVCMOS18, and LVCMOS25 and LVCMOS33.

3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 2-18 • **LVTTL/LVCMOS 3.3 V DC Voltage Specification**

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	
LVTTL/LVCMOS 3.3 V DC Input Voltage Specification							
VIH (DC)	DC input logic High		2.0	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.8	V	
IIH (DC)	Input current High		–	–	10	mA	
IIL (DC)	Input current Low		–	–	10	mA	
LVCMOS 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		VDDI – 0.4	–	–	V	1
VOL	DC output logic Low		–	–	0.4	V	1
LVTTL 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		0.4	–	–	V	
VOL	DC output logic Low		–	–	2.4	V	
LVTTL/LVCMOS 3.3 V AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 10 pF / 500 Ohm Load, maximum drive/slew	–	–	600	Mbps	
LVTTL/LVCMOS 3.3 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	1.4	–	V	
Rent	Resistance for enable path (tZH, tZL, tHZ, tLZ)		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (tZH, tZL, tHZ, tLZ)		–	5	–	pF	
Cload	Capacitive loading for data path (tDP)		–	5	–	pF	

Notes:

1. *The VOH/VOL test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.*

Table 2-19 • LVTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications

Output Drive Selection / MSIO I/O Bank	VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA	Notes
1	VDDI – 0.4	0.4	2	2	
2	VDDI – 0.4	0.4	4	4	
3	VDDI – 0.4	0.4	8	8	
4	VDDI – 0.4	0.4	12	12	
6	VDDI – 0.4	0.4	16	16	
8	VDDI – 0.4	0.4	20	20	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 3.0 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 2-20 • LVCMOS 3.3 V Receiver Characteristics

	On Die Termination (ODT)	TDIN		TSCH_DIN		Units
		–1	Std.	–1	Std.	
LVCMOS 3.3 V (For MSIO I/O bank)	None	2.46	2.893	2.408	2.833	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 2-21 • LVCMOS 3.3 V Transmitter Characteristics

Output Drive Selection	Slew Control	TDOUT		TENZL		TENZH		TENHZ		TENLZ		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 3.3 V (for MSIO I/O bank)												
1	–	3.274	3.853	3.459	4.069	3.269	3.845	3.608	4.244	3.419	4.022	ns
2	–	2.418	2.845	2.914	3.427	4.35	5.116	3.064	3.604	4.5	5.293	ns
3	–	2.221	2.614	4.195	4.935	4.695	5.523	4.345	5.112	4.845	5.7	ns
4	–	2.128	2.505	5.135	6.041	5.105	6.005	5.285	6.218	5.255	6.182	ns
6	–	2.147	2.526	5.776	6.795	5.451	6.412	5.926	6.972	5.601	6.589	ns
8	–	2.228	2.622	5.958	7.009	5.691	6.695	6.108	7.186	5.841	6.872	ns

LVCMOS 2.5 V

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in SmartFusion2 FPGAs in compliance to the JEDEC specification JESD8-5A.

Minimum and Maximum DC Input and Output Levels Specification

Table 2-22 • LVCMOS 2.5 V DC Voltage Specification

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply Voltage		2.375	2.5	2.625	V	
LVCMOS 2.5 V DC Input Voltage Specification							
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O bank)		1.7	–	2.625	V	
VIH (DC)	DC input logic High (for MSIO I/O bank)		1.7	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.7	V	
IIH (DC)	Input current High		–	–	–	mA	
IIL (DC)	Input current Low		–	–	–	mA	
LVCMOS 2.5 V DC Output Voltage Specification							
VOH	DC output logic High		VDDI – 0.4	–	–	V	1
VOL	DC output logic Low		–	–	0.4	V	1
LVCMOS 2.5 V AC Specifications							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: 5 pF load, maximum drive/slew	–	–	250	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	410	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	420	Mbps	
	Supported output driver calibrated impedance (for DDRIO I/O bank)			75, 60, 50, 33, 25, 20		Ohms	
LVCMOS 2.5 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path			1.2		V	
Rent	Resistance for enable path (tZH, tZL, tHZ, tLZ)			2K		Ohms	
Cent	Capacitive loading for enable path (tZH, tZL, tHZ, tLZ)			5		pF	
Cload	Capacitive loading for data path (tDP)			5		pF	

Notes:

1. *The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.*

Table 2-23 • LVCMOS 2.5 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA	Notes
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min.	Max.			
1	2	2	VDDI – 0.4	0.4	2	2	
2	3	4	VDDI – 0.4	0.4	4	4	
3	4	5	VDDI – 0.4	0.4	6	6	
4	6	7	VDDI – 0.4	0.4	8	8	
5	8	10	VDDI – 0.4	0.4	12	12	
7	N/A	14	VDDI – 0.4	0.4	16	16	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 3.0 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 2-24 • LVCMOS 2.5 V Receiver Characteristics

	On Die Termination (ODT)	TDIN		TSCH_DIN		Units
		–1	Std.	–1	Std.	
LVCMOS 2.5 V (for DDRIO I/O bank)	N/A	TBD	TBD	TBD	TBD	ns
LVCMOS 2.5 V (for MSIO I/O bank)	N/A	2.594	3.052	2.561	3.013	ns
LVCMOS 2.5 V (for MSIOD I/O bank)	N/A	TBD	TBD	TBD	TBD	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 2-25 • LVCMOS 2.5 V Transmitter Characteristics

Output Drive Selection	Slew Control (0 lowest, 3 highest)	TDOUT		TENZL		TENZH		TENHZ		TENZH		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 2.5 V (for DDRIO I/O bank with FIED CODES)												
2	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
4	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
5	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns

***Table 2-25* • LVCMOS 2.5 V Transmitter Characteristics (continued)**

Output Drive Selection	Slew Control (0 lowest, 3 highest)	TDOUT		TENZL		TENZH		TENHZ		TENZH		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
7	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
10	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
14	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
LVCMOS 2.5 V (for MSIO I/O bank)												
1	None	3.534	4.158	3.816	4.489	3.742	4.402	3.888	4.574	3.814	4.487	ns
2	None	2.651	3.118	3.898	4.586	4.625	5.441	3.971	4.672	4.698	5.527	ns
3	None	2.463	2.898	4.794	5.639	4.994	5.875	4.867	5.725	5.067	5.961	ns
4	None	2.382	2.802	5.724	6.734	5.417	6.373	5.797	6.82	5.49	6.459	ns
5	None	2.405	2.829	5.883	6.921	5.593	6.58	5.956	7.007	5.666	6.666	ns
7	None	2.481	2.918	6.281	7.389	5.871	6.907	6.354	7.475	5.944	6.993	ns
LVCMOS 2.5 V (for MSIOD I/O bank)												
2	None	2.367	2.786	5.054	5.946	4.749	5.587	5.158	6.069	4.853	5.71	ns
3	None	1.978	2.328	5.533	6.509	5.159	6.069	5.637	6.632	5.263	6.192	ns
4	None	1.843	2.169	5.927	6.973	5.495	6.465	6.031	7.096	5.599	6.588	ns
6	None	1.757	2.067	6.33	7.447	5.795	6.818	6.434	7.57	5.899	6.941	ns
8	None	1.77	2.083	6.607	7.773	5.998	7.056	6.711	7.896	6.102	7.179	ns

1.8 V LVCMOS

LVCMOS 1.8 is a general standard for 1.8 V applications and is supported in SmartFusion2 FPGAs in compliance to the JEDEC specification JESD8-7A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 2-26 • LVCMOS 1.8 V DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply Voltage		1.710	1.8	1.89	V	
LVCMOS 1.8 V DC Input Voltage Specification							
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O bank)		0.65 * VDDI	–	1.89	V	
VIH (DC)	DC input logic High (for MSIO I/O bank)		0.65 * VDDI	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.35 * VDDI	V	
IIH (DC)	Input current High		–	–	10	mA	
IIL (DC)	Input current Low		–	–	10	mA	
LVCMOS 1.8 V DC Output Voltage Specification							
VOH	DC output logic High		VDDI – 0.45	–	–	V	
VOL	DC output logic Low		–	–	0.45	V	
LVCMOS 1.8 V AC Specifications							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: 5 pF load, maximum drive/slew	–	–	200	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	295	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	320	Mbps	
	Supported output driver calibrated impedance (for DDRIO I/O bank)			75, 60, 50, 33, 25, 20		Ohms	
LVCMOS 1.8 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	0.9	–	V	
Rent	Resistance for enable path (tZH, tZL, tHZ, tLZ)		–	2k	–	Ohms	
Cent	Capacitive loading for enable path (tZH, tZL, tHZ, tLZ)		–	5	–	pF	
Cload	Capacitive loading for data path (tDP)		–	5	–	pF	

Table 2-27 • LVCMOS 1.8 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA	Notes
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min.	Max.			
2	2	2	VDDI – 0.4	0.45	2	2	
3	3	3	VDDI – 0.4	0.45	4	4	
4	5	4	VDDI – 0.4	0.45	6	6	
5	6	5	VDDI – 0.4	0.45	8	8	
6	8	7	VDDI – 0.4	0.45	10	10	
7	N/A	8	VDDI – 0.4	0.45	12	12	
N/A	N/A	10	VDDI – 0.4	0.45	16	16	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.71 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 2-28 • LVCMOS 1.8 V Receiver Characteristics

		TDIN		TSCH_DIN		Units
	On Die Termination (ODT)	–1	Std.	–1	Std.	
LVCMOS 1.8 V (for DDRIO I/O bank)	0	TBD	TBD	TBD	TBD	ns
	50	TBD	TBD	TBD	TBD	ns
	75	TBD	TBD	TBD	TBD	ns
	150	TBD	TBD	TBD	TBD	ns
LVCMOS 1.8 V (for MSIO I/O bank)	0	3.241	3.813	3.248	3.82	ns
	50	3.377	3.973	3.381	3.977	ns
	75	3.332	3.92	3.342	3.932	ns
	150	3.285	3.865	3.297	3.879	ns
LVCMOS 1.8 V (for MSIOD I/O bank)	0	TBD	TBD	TBD	TBD	ns
	50	TBD	TBD	TBD	TBD	ns
	75	TBD	TBD	TBD	TBD	ns
	150	TBD	TBD	TBD	TBD	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 2-29 • LVCMOS 1.8 V Transmitter Characteristics

Output Drive Selection	Slew Control (0 lowest, 3 highest)	TDOUT		TENZL		TENZH		TENHZ		TENLZ		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 1.8 V (for DDRIO I/O bank)												
2	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
3	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
4	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns

Table 2-29 • **LVCMOS 1.8 V Transmitter Characteristics (continued)**

Output Drive Selection	Slew Control (0 lowest, 3 highest)	TDOUT		TENZL		TENZH		TENHZ		TENLZ		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
5	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
7	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
8	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
10	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
LVCMOS 1.8 V (for MSIO I/O bank)												
2	None	3.486	4.101	4.621	5.436	5.107	6.008	4.607	5.419	5.093	5.991	ns
3	None	3.244	3.816	5.351	6.295	5.518	6.492	5.337	6.278	5.504	6.475	ns
4	None	3.148	3.703	6.32	7.436	5.963	7.015	6.306	7.419	5.949	6.998	ns
5	None	3.189	3.752	8.577	7.738	6.131	7.213	6.563	7.721	6.117	7.196	ns
6	None	3.241	3.812	6.956	8.184	6.344	7.464	6.942	8.167	6.33	7.447	ns
7	None	3.319	3.904	7.076	8.324	6.44	7.577	7.062	8.307	6.426	7.56	ns
LVCMOS 1.8 V (For MSIOD I/O bank)												
2	None	2.789	3.282	5.321	6.26	4.98	5.86	5.383	6.333	5.042	5.933	ns
3	None	2.332	2.744	5.846	6.878	5.42	6.377	5.908	6.951	5.482	6.45	ns
5	None	2.1	2.472	6.497	7.644	5.945	6.994	6.559	7.717	6.007	7.067	ns
6	None	2.099	2.47	6.755	7.947	6.142	7.227	6.817	8.02	6.204	7.3	ns
8	None	2.136	2.513	7.046	8.29	6.355	7.477	7.108	8.363	6.417	7.55	ns

1.5 V LVCMOS

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in SmartFusion2 FPGAs in compliance to the JEDEC specification JESD8-11A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 2-30 • LVCMOS 1.5 V DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply Voltage		1.425	1.5	1.575	V	
LVCMOS 1.5 V DC Input Voltage Specification							
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O banks)		0.65 * VDDI	–	1.575	V	
VIH (DC)	DC input logic High (for MSIO I/O bank)		0.65 * VDDI	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.35 * VDDI	V	
IIH (DC)	Input current High		–	–	10	mA	
IIL (DC	Input current Low		–	–	10	mA	
LVCMOS 1.5 V DC Output Voltage Specification							
VOH	DC output logic High		VDDI * 0.75	–	–	V	
VOL	DC output logic Low		–	–	VDDI * 0.25	V	
LVCMOS 1.5 V AC Specifications							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: 5 pF load, maximum drive/slew	–	–	130	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	80	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	170	Mbps	
	Supported output driver calibrated impedance (for DDRIO I/O bank)			75, 60, 50, 40		Ohms	
LVCMOS 1.5 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point		–	0.75	–	V	
Rent	Resistance for enable path (tZH, tZL, tHZ, tLZ)		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (tZH, tZL, tHZ, tLZ)		–	5	–	pF	
Cload	Capacitive loading for data path (tDP)		–	5	–	pF	

Table 2-31 • LVCMOS 1.5 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)			
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min.	Max.	IOH (at VOH) mA	IOL (at VOL) mA	Notes
2	3	2	VDDI * 0.75	VDDI * 0.25	2	2	
4	5	4	VDDI * 0.75	VDDI * 0.25	4	4	
5	7	6	VDDI * 0.75	VDDI * 0.25	6	6	
7	N/A	8	VDDI * 0.75	VDDI * 0.25	8	8	
N/A	N/A	10	VDDI * 0.75	VDDI * 0.25	10	10	
N/A	N/A	12	VDDI * 0.75	VDDI * 0.25	12	12	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.425 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 2-32 • LVCMOS 1.5 V Receiver Characteristics

		TDIN		TSCH_DIN		
	On Die Termination (ODT)	–1	Std.	–1	Std.	Units
LVCMOS 1.5 V (for DDRIO I/O bank)	0	TBD	TBD	TBD	TBD	ns
	50	TBD	TBD	TBD	TBD	ns
	75	TBD	TBD	TBD	TBD	ns
	150	TBD	TBD	TBD	TBD	ns
LVCMOS 1.5 V (for MSIO I/O bank)	0	3.817	4.49	3.844	4.522	ns
	50	4.13	4.858	4.164	4.898	ns
	75	4.01	4.717	4.044	4.757	ns
	150	3.916	4.607	3.944	4.64	ns
LVCMOS 1.5 V (for MSIOD I/O bank)	0	TBD	TBD	TBD	TBD	ns
	50	TBD	TBD	TBD	TBD	ns
	75	TBD	TBD	TBD	TBD	ns
	150	TBD	TBD	TBD	TBD	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 2-33 • LVCMOS 1.5 V Transmitter Characteristics

Output Drive Selection	Slew Control (0 lowest, 3 highest)	TDOUT		TENZL		TENZH		TENHZ		TENLZ		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 1.5 V (for DDRIO I/O bank)												
2	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
4	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
6	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns

***Table 2-33* • LVCMOS 1.5 V Transmitter Characteristics (continued)**

Output Drive Selection	Slew Control (0 lowest, 3 highest)	TDOUT		TENZL		TENZH		TENHZ		TENLZ		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
8	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
10	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
12	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
LVCMOS 1.5 V (for MSIO I/O bank)												
2	None	4.437	5.219	5.342	6.285	5.57	6.552	5.295	6.23	5.523	6.497	ns
4	None	3.989	4.692	7.006	8.242	6.488	7.633	6.959	8.187	6.441	7.578	ns
5	None	4.046	4.76	7.288	8.574	6.664	7.839	7.241	8.519	6.617	7.784	ns
7	None	4.226	4.971	7.869	9.257	6.99	8.224	7.822	9.202	6.943	8.169	ns
LVCMOS 1.5 V (For MSIOD I/O bank)												
3	None	2.788	3.279	6.125	7.206	5.662	6.661	6.179	7.27	5.716	6.725	ns
5	None	2.489	2.927	6.831	8.037	6.24	7.341	6.885	8.101	6.294	7.405	ns
7	None	2.508	2.95	7.212	8.484	6.527	7.679	7.266	8.548	6.581	7.743	ns

1.2 V LVCMOS

LVCMOS 1.2 is a general standard for 1.2 V applications and is supported in SmartFusion2 FPGAs in compliance to the JEDEC specification JESD8-12A.

LVCMOS 1.2 V Minimum and Maximum DC/AC Input and Output Levels Specification

Table 2-34 • LVCMOS 1.2 V DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply Voltage		1.14	1.2	1.26	V	
LVCMOS 1.2 V DC Input Voltage Specification							
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O bank)		0.65 * VDDI	–	1.26	V	
VIH (DC)	DC input logic High (for MSIO I/O bank)		0.65 * VDDI	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.35 * VDDI	V	
IIH (DC)	Input current High		–	–	10	mA	
IIL (DC)	Input current Low		–	–	10	mA	
LVCMOS 1.2 V DC Output Voltage Specification							
VOH	DC output logic High		VDDI * 0.75	–	–	V	
VOL	DC output logic Low		–	–	VDDI * 0.25	V	
LVCMOS 1.2 V AC Specifications							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: 2 pF load, maximum drive/slew	–	–	75	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2.5 pF load, maximum drive/slew	–	–	50	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 2.5 pF load, maximum drive/slew	–	–	100	Mbps	
Rref	Supported output driver calibrated impedance (for DDRIO I/O bank)			75, 60, 50, 40		Ohms	
LVCMOS 1.2 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point		–	0.6	–	V	
Rent	Resistance for enable path (tZH, tZL, tHZ, tLZ)		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (tZH, tZL, tHZ, tLZ)		–	5	–	pF	
Cload	Capacitive loading for data path (tDP)		–	5	–	pF	

Table 2-35 • LVCMOS 1.2 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)			
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min.	Max.	IOH (at VOH) mA	IOL (at VOL) mA	Notes
4	4	4	VDDI * 0.75	VDDI * 0.25	2	2	
7	8	8	VDDI * 0.75	VDDI * 0.25	4	4	
N/A	N/A	12	VDDI * 0.75	VDDI * 0.25	6	6	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.14 V

AC Switching Characteristics for Receiver (Input Buffers))

Table 2-36 • LVCMOS 1.2 V Receiver Characteristics

		TDIN		TSCH_DIN		
	On Die Termination (ODT)	**–1**	**Std.**	**–1**	**Std.**	**Units**
LVCMOS 1.2 V (for DDRIO I/O bank)	0	TBD	TBD	TBD	TBD	ns
	50	TBD	TBD	TBD	TBD	ns
	75	TBD	TBD	TBD	TBD	ns
	150	TBD	TBD	TBD	TBD	ns
LVCMOS 1.2 V (for MSIO I/O bank)	0	5.3	6.235	5.335	6.276	ns
	50	6.776	7.971	6.836	8.042	ns
	75	6.179	7.269	6.23	7.32	ns
	150	5.683	6.686	5.73	6.741	ns
LVCMOS 1.2 V (for MSIOD I/O bank)	0	TBD	TBD	TBD	TBD	ns
	50	4.639	5.458	4.676	5.502	ns
	75	5.599	6.588	5.66	6.66	ns
	150	5.037	5.926	5.081	5.978	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 2-37 • LVCMOS 1.2 V Transmitter Characteristics

Output Drive Selection	Slew Control (0 lowest, 3 highest)	TDOUT		TENZL		TENZH		TENHZ		TENLZ		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 1.2 V (for DDRIO I/O bank)												
4	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
8	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
12	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
LVCMOS 1.2 V (for MSIO I/O bank)												
4	None	5.87	6.905	8.659	10.186	7.563	8.897	8.53	10.035	7.434	8.746	ns
7	None	6.215	7.312	9.639	11.339	8.114	9.546	9.51	11.188	7.985	9.395	ns
LVCMOS 1.2 V (For MSIOD I/O bank)												
4	None	3.509	4.128	7.29	8.577	6.693	7.874	7.356	8.654	6.759	7.951	ns
8	None	3.419	4.022	8.135	9.571	7.347	8.644	8.201	9.648	7.413	8.721	ns

3.3 V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3 V standards specifies support for 33 MHz and 66 MHz PCI bus applications.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 2-38 • PCI/PCIX DC Voltage Specification – Applicable to MSIO Bank ONLY

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
PCI/PCIX Recommended DC Operating Conditions							
VDDI	Supply Voltage		3.15	3.3	3.45	V	
PCI/PCIX DC Input Voltage Specification							
VI	DC input voltage		0	–	3.45	V	
IIH(DC)	Input current High		–	–	10	µA	
IIL(DC)	Input current Low		–	–	10	µA	
PCI/PCIX DC Output Voltage Specification							
VOH	DC output logic High		Per PCI Specification			V	
VOL	DC output logic Low		Per PCI Specification			V	
PCI/PCIX AC Specifications							
Fmax	Maximum data rate (MSIO I/O bank)	AC Loading: per JEDEC specifications	–	–	630	Mbps	
PCI/PCIX AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path (falling edge)		–	0.615 * VDDI	–	V	
Vtrip	Measuring/trip point for data path (rising edge)		–	0.285 * VDDI	–	V	
Rtt_test	Resistance for data test path		–	25	–	Ohms	
Rent	Resistance for enable path (tZH, tZL, tHZ, tLZ)		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (tZH, tZL, tHZ, tLZ)		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 3.0 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 2-39 • AC Switching Characteristics for Receiver (Input Buffers)

	On Die Termination (ODT)	TDIN		TSCH_DIN		Units
		Speed Grade		Speed Grade		
		–	Std.	–1	Std.	
PCI/PCIX (for MSIO I/O bank)	None	2.266	2.667	2.25	2.648	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 2-40 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers

	TDOUT		TENZL		TENZH		TENHZ		TENLZ		Units
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
PCI/PCIX (for MSIO I/O bank)											
	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns

Memory Interface and Voltage Referenced I/O Standards

High-Speed Transceiver Logic (HSTL)

The High-Speed Transceiver Logic (HSTL) standard is a general purpose high-speed bus standard sponsored by IBM (EIA/JESD8-6). SmartFusion2 devices support two classes of the 1.5 V HSTL. These differential versions of the standard require a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 2-41 • **HSTL DC Voltage Specification**

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply Voltage		1.425	1.5	1.575	V	
VTT	Termination Voltage		0.698	0.750	0.803	V	
VREF	Input Reference Voltage		0.698	0.750	0.803	V	
HSTL DC Input Voltage Specification							
VIH (DC)	DC input logic High		VREF + 0.1	–	1.575	V	
VIL (DC)	DC input logic Low		–0.3	–	VREF – 0.1	V	
IIH (DC)	Input current High		–	–	10	V	
IIL (DC)	Input current Low		–	–	10	V	
HSTL DC Output Voltage Specification							
HSTL Class I							
VOH	DC output logic High		VDDI – 0.4	–	–	V	
VOL	DC output logic Low		–	–	0.4	V	
IOH at VOH	Output minimum source DC current (MSIOD I/O bank)		–7.8	–	–	mA	1
IOL at VOL	Output minimum sink current (MSIOD I/O bank)		7.8	–	–	mA	1
IOH at VOH	Output minimum source DC current (MSIO and DDRIO I/O banks)		–8.0	–	–	mA	
IOL at VOL	Output minimum sink current (MSIO and DDRIO I/O banks)		8.0	–	–	mA	
HSTL Class II (Applicable to MSIO and DDRIO IO Bank only)							
VOH	DC output logic High		VDDI – 0.4	–	–	V	
VOL	DC output logic Low		–	–	0.4	V	
IOH at VOH	Output minimum source DC current		–16.0	–	–	mA	
IOL at VOL	Output minimum sink current		16.0	–	–	mA	
HSTL AC/DC Differential Voltage Specifications							
VID (DC)	DC input differential voltage		0.2	–	–	V	
VDIFF (AC)	AC input differential voltage		0.4	–	–	V	
Vx (AC)	AC differential cross point voltage		0.68	–	0.9	V	
HSTL AC Specifications							
Fmax	Maximum data rate (DDRIO I/O bank)	AC loading: per JEDEC specifications	–	–	800	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 3 pF / 50 Ohm load	–	–	140	Mbps	

Notes:

1. *MSIOD I/O bank HSTL Class I does not meet standard JEDEC test point. Use provided lower current values as specified.*

***Table 2-41* • HSTL DC Voltage Specification (continued)**

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 3 pF / 50 Ohm load	–	–	180	Mbps	
Rref	Supported output driver calibrated impedance (for DDRIO I/O bank)	Reference resistance = 191 Ohms	–	25.5, 47.8	–	Ohms	
RTT	Effective impedance value (with respect to reference resistor of 191 Ohms) (ODT for DDRIO I/O bank only)	Reference resistance = 191 Ohms	–	47.8	–	Ohms	
RTT	Effective impedance value (ODT for MSIO and MSIOD I/O banks only)	Reference resistance = 191 Ohms	–	50, 75, 150	–	Ohms	
HSTL AC Test Parameters Specification							
Vtrip	Measuring/trip point for data path		–	–	–	V	
Rent	Resistance for enable path (tZH, tZL, tHZ, tLZ)		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (tZH, tZL, tHZ, tLZ)		–	5	–	pF	
Rtt_test	Reference resistance for data test path for SSTL15 Class I (tDP)			50		Ohms	
Rtt_test	Reference resistance for data test path for SSTL15 Class II (tDP)		–	25	–	Ohms	
Cload	Capacitive Loading for Data Path (tDP)		–	5	–	pF	

Notes:

1. *MSIOD I/O bank HSTL Class I does not meet standard JEDEC test point. Use provided lower current values as specified.*

AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 2-42 • HSTL Receiver Characteristics

	On Die Termination (ODT)	TDIN		TSCH_DIN		Units
		–1	Std.	–1	Std.	
HSTL (for DDRIO I/O bank)						
Pseudo-Differential	None	TBD	TBD	N/A	N/A	ns
	47.8	TBD	TBD	N/A	N/A	ns
True-Differential	None	TBD	TBD	N/A	N/A	ns
	47.8	TBD	TBD	N/A	N/A	ns
HSTL (for MSIO I/O bank)						
Pseudo-Differential	None	13.8	16.236	18.906	22.242	ns
	50	13.65	16.059	19.056	22.419	ns
	75	13.637	16.044	19.02	22.377	ns
	150	13.597	15.996	18.964	22.31	ns
True-Differential	None	TBD	TBD	TBD	TBD	ns
	50	TBD	TBD	TBD	TBD	ns
	75	TBD	TBD	TBD	TBD	ns
	150	TBD	TBD	TBD	TBD	ns
HSTL (for MSIOD I/O bank)						
Pseudo-Differential	None	TBD	TBD	TBD	TBD	ns
	50	TBD	TBD	TBD	TBD	ns
	75	TBD	TBD	TBD	TBD	ns
	150	TBD	TBD	TBD	TBD	ns
True-Differential	None	TBD	TBD	TBD	TBD	ns
	50	TBD	TBD	TBD	TBD	ns
	75	TBD	TBD	TBD	TBD	ns
	150	TBD	TBD	TBD	TBD	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 2-43 • HSTL Transmitter Characteristics

	TDOUT		TENZL		TENZH		TENHZ		TENLZ		
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	Units
HSTL Class I											
For DDRIO I/O Bank											
Single-ended	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Differential	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
For MSIO I/O Bank											
Single-ended	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Differential	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
For MSIOD I/O Bank											
Single-ended	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Differential	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
HSTL Class II											
For DDRIO I/O Bank											
Single-ended	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Differential	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns

Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in SmartFusion2 devices. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. SmartFusion2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3 and JEDEC standard JESD209A for LPDDR.

Stub-Series Terminated Logic 2.5 V (SSTL2)

SSTL2 Class I and Class II are supported in SmartFusion2 devices, and also comply with reduced and full drive of double data rate (DDR) standards. SmartFusion2 FPGA I/O supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

***Table 2-44* • DDR1/SSTL2 DC Voltage Specification**

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply Voltage		2.375	2.5	2.625	V	
VTT	Termination Voltage		1.164	1.250	1.339	V	
VREF	Input Reference Voltage		1.164	1.250	1.339	V	
DDR/SSTL2 DC Input Voltage Specification							
VIH (DC)	DC input logic High		VREF + 0.125	–	2.625	V	
VIL (DC)	DC input logic Low		–0.3	–	VREF – 0.15	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Lo		–	–	10	µA	
DDR/SSTL2 DC Output Voltage Specification							
SSTL2 Class I (DDR Reduced Drive)							
VOH	DC output logic High		VTT + 0.608	–	–	V	
VOL	DC output logic Low		–	–	VTT – 0.608	V	
IOH at VOH	Output minimum source DC current		8.1	–	–	mA	
IOL at VOL	Output minimum sink current		–8.1	–	–	mA	
SSTL2 Class II (DDR Full Drive) – Applicable to MSIO and DDRIO I/O Banks ONLY							
VOH	DC output logic High		VTT + 0.81	–	–	V	
VOL	DC output logic Low		–	–	VTT – 0.81	V	
IOH at VOH	Output minimum source DC current		16.2	–	–	mA	
IOL at VOL	Output minimum sink current		–16.2	–	–	mA	
SSTL2 AC/DC Differential Voltage Specification							
VID (DC)	DC input differential voltage		0.3	–	–	V	
VDIFF (AC)	AC input differential voltage		0.7	–	–	V	
Vx (AC)	AC differential cross point voltage		0.5 * VDDI – 0.2	–	0.5 * VDDI + 0.2	V	

***Table 2-44* • DDR1/SSTL2 DC Voltage Specification (continued)**

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
SSTL2 AC Specifications							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: per JEDEC specifications	–	–	400	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 10 pF / 50 Ohm load	–	–	575	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 30 pF / 50 Ohm load	–	–	700	Mbps	
Rref	Supported output driver calibrated impedance (for DDRIO I/O bank)	Reference resistor = 150 Ohms	–	20, 42	–	Ohms	
AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	1.25	–	V	
Rent	Resistance for enable path (tZH, tZL, tHZ, tLZ)		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (tZH, tZL, tHZ, tLZ)		–	5	–	pF	
Rs	Series resistance for data test path (tDP)		–	25	–	Ohms	
Rtt_test	Reference resistance for data test path for SSTL2 Class I (tDP)		–	50	–	Ohms	
Rtt_test	Reference resistance for data test path for SSTL2 Class II (tDP)		–	25	–	Ohms	
Cload	Capacitive loading for data path (tDP)		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 2-45 • DDR1/SSTL2 Receiver Characteristics

	On Die Termination (ODT)	TDIN		TSCH_DIN		Units
		–1	Std.	–1	Std.	
SSTL2 (for DDRIO I/O bank)						
Pseudo-Differential	None	TBD	TBD	–	–	ns
True-Differential	None	TBD	TBD	–	–	ns
SSTL2 (for MSIO I/O bank)						
Pseudo-Differential	None	2.805	3.3	2.987	3.515	ns
True-Differential	None	TBD	TBD	TBD	TBD	ns
SSTL2 (for MSIOD I/O bank)						
Pseudo-Differential	None	TBD	TBD	TBD	TBD	ns
True-Differential	None	TBD	TBD	TBD	TBD	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 2-46 • DDR1/SSTL2 Transmitter Characteristics

	TDOUT		TENZL		TENZH		TENHZ		TENLZ		
	–1	STD	–1	STD	–1	STD	–1	STD	–1	STD	Units
SSTL2 Class I											
For DDRIO I/O Bank											
Single-ended	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Differential	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
For MSIO I/O Bank											
Single-ended	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Differential	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
For MSIOD I/O Bank											
Single-ended	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Differential	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
SSTL2 Class II											
For DDRIO I/O Bank											
Single-ended	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Differential	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
For MSIO I/O Bank											
Single-ended	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Differential	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
For MSIOD I/O Bank											
Single-ended	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Differential	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns

Stub-Series Terminated Logic 1.8 V (SSTL18)

SSTL18 Class I and Class II are supported in SmartFusion2 devices, and also comply with the reduced and full drive double date rate (DDR2) standard. SmartFusion2 FPGA I/O supports both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 2-47 • SSTL18 DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply Voltage		1.71	1.8	1.89	V	
VTT	Termination Voltage		0.838	0.900	0.964	V	
VREF	Input Reference Voltage		0.838	0.900	0.964	V	
SSTL18 DC Input Voltage Specification							
VIH (DC)	DC input logic High		VREF + 0.125	–	1.89	V	
VIL (DC)	DC input logic Low		–0.3	–	VREF – 0.125	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
SSTL18 DC Output Voltage Specification							
SSTL18 Class I (DDR2 Reduced Drive)							
VOH	DC output logic High		VTT + 0.603	–	–	V	
VOL	DC output logic Low		–	–	VTT– 0.603	V	
IOH at VOH	Output minimum source DC current (MSIO I/O bank only		4.7	–	–	mA	1
IOL at VOL	Output minimum sink current (MSIO I/O bank only)		–4.7	–	–	mA	1
IOH at VOH	Output minimum source DC current (MSIOD I/O bank only		6.3	–	–	mA	1
IOL at VOL	Output minimum sink current (MSIOD I/O bank only)		–6.3	–	–	mA	1
IOH at VOH	Output minimum source DC current (DDRIO I/O bank only		6.5	–	–	mA	1
IOL at VOL	Output minimum sink current (DDRIO I/O bank only)		–6.5	–	–	mA	1

Notes:

1. *MSIO I/O bank SSTL18/DDR2 Reduced Drive does not have a standard test point. This is defined to fit within the DDR2 Reduced Drive IV Curve minimums.*
2. *MSIO I/O bank SSTL18/DDR2 Class II does not meet the standard JEDEC test points. Use provided lower current values as specified.*

***Table 2-47* • SSTL18 DC Voltage Specification (continued)**

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
STL18 Class II (DDR2 Full Drive) – Applicable to MSIO and DDRIO I/O Banks ONLY							
VOH	DC output logic High		VTT + 0.603	–	–	V	
VOL	DC output logic Low		–	–	VTT– 0.603	V	
IOH at VOH	Output minimum source DC current (MSIO I/O bank only)		9.3	–	–	mA	
IOL at VOL	Output minimum sink current (MSIO I/O bank only)		–9.3	–	–	mA	
IOH at VOH	Output minimum source DC current (DDRIO I/O bank only)		13.4	–	–	mA	
IOL at VOL	Output minimum sink current (DDRIO I/O bank only)		–13.4	–	–	mA	
SSTL18 AC/DC Differential Voltage Specification							
VID (DC	DC input differential voltage		0.3	–	–	V	
VDIFF (AC)	AC input differential voltage		0.7			V	
Vx (AC)	AC differential cross point voltage		0.5 * VDDI – 0.175	–	0.5 * VDDI + 0.175	V	
SSTL18 AC Specification							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: per JEDEC specification	–	–	800	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 3 pF / 25 Ohm load	–	–	432	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 3 pF / 25 Ohm load	–	–	430	Mbps	
Rref	Supported output driver calibrated impedance (for DDRIO I/O bank)	Reference resistor = 150 Ohms	–	20, 42		Ohms	
RTT	Effective impedance value (with respect to reference resistor 150 Ohms) (ODT for DDRIO I/O bank only)	Reference resistor = 150 Ohms	–	50, 75, 150		Ohms	

Notes:

1. *MSIO I/O bank SSTL18/DDR2 Reduced Drive does not have a standard test point. This is defined to fit within the DDR2 Reduced Drive IV Curve minimums.*
2. *MSIO I/O bank SSTL18/DDR2 Class II does not meet the standard JEDEC test points. Use provided lower current values as specified.*

Table 2-47 • SSTL18 DC Voltage Specification (continued)

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	0.9	–	V	
Rent	Resistance for enable path (tZH, tZL, tHZ, tLZ)		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (tZH, tZL, tHZ, tLZ)		–	5	–	pF	
Rs	Series resistance for data test path (tDP)		–	25	–	Ohms	
Rtt_test	Reference resistance for data test path for SSTL18 Class I (tDP)		–	50	–	Ohms	
Rtt_test	Reference resistance for data test path for SSTL18 Class II (tDP)		–	25	–	Ohms	
Cload	Capacitive loading for data path (tDP)		–	5	–	pF	

Notes:

1. *MSIO I/O bank SSTL18/DDR2 Reduced Drive does not have a standard test point. This is defined to fit within the DDR2 Reduced Drive IV Curve minimums.*
2. *MSIO I/O bank SSTL18/DDR2 Class II does not meet the standard JEDEC test points. Use provided lower current values as specified.*

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.71 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 2-48 • DDR2/SSTL18 Receiver Characteristics

	ODT (On Die Termination)	TDIN		TSCH_DIN		Units
		–1	STD	–1	STD	
SSTL18 (for DDRIO I/O bank)						
Pseudo-Differential	None	TBD	TBD	N/A	N/A	ns
	50	TBD	TBD	N/A	N/A	ns
	75	TBD	TBD	N/A	N/A	ns
	150	TBD	TBD	N/A	N/A	ns
True-Differential	None	TBD	TBD	N/A	N/A	ns
	50	TBD	TBD	N/A	N/A	ns
	75	TBD	TBD	N/A	N/A	ns
	150	TBD	TBD	N/A	N/A	ns
SSTL18 (for MSIO I/O bank)						
Pseudo-Differential	None	TBD	TBD	TBD	TBD	ns
	50	TBD	TBD	TBD	TBD	ns
	75	TBD	TBD	TBD	TBD	ns
	150	TBD	TBD	TBD	TBD	ns

***Table 2-48* • DDR2/SSTL18 Receiver Characteristics**

	ODT (On Die Termination)	TDIN		TSCH_DIN		Units
		–1	STD	–1	STD	
True-Differential	None	TBD	TBD	TBD	TBD	ns
	50	TBD	TBD	TBD	TBD	ns
	75	TBD	TBD	TBD	TBD	ns
	150	TBD	TBD	TBD	TBD	ns
SSTL18 (for MSIOD I/O bank)						
Pseudo-Differential	None	TBD	TBD	TBD	TBD	ns
	50	TBD	TBD	TBD	TBD	ns
	75	TBD	TBD	TBD	TBD	ns
	150	TBD	TBD	TBD	TBD	ns
True-Differential	None	TBD	TBD	TBD	TBD	ns
	50	TBD	TBD	TBD	TBD	ns
	75	TBD	TBD	TBD	TBD	ns
	150	TBD	TBD	TBD	TBD	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

***Table 2-49* • DDR2/SSTL18 Transmitter Characteristics**

	TDOUT		TENZL		TENZH		TENHZ		TENLZ		Units
	–1	STD	–1	STD	–1	STD	–1	STD	–1	STD	
SSTL2 Class I											
For DDRIO I/O Bank											
Single-ended	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Differential	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
For MSIO I/O Bank											
Single-ended	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Differential	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
For MSIOD I/O Bank											
Single-ended	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Differential	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
SSTL2 Class II											
For DDRIO I/O Bank											
Single-ended	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Differential	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
For MSIO I/O Bank											
Single-ended	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Differential	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
For MSIOD I/O Bank											
Single-ended	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Differential	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns

Stub-Series Terminated Logic 1.5 V (SSTL15)

SSTL15 Class I and Class II are supported in SmartFusion2 devices, and also comply with the reduced and full drive double data rate (DDR3) standard. SmartFusion2 FPGA I/O supports both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

***Table 2-50* • SSTL15 DC Voltage Specification (for DDRIO I/O Bank Only)**

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply Voltage		1.425	1.5	1.575	V	
VTT	Termination Voltage		0.698	0.750	0.803	V	
VREF	Input Reference Voltage		0.698	0.750	0.803	V	
SSTL15 DC Input Voltage Specification							
VIH(DC)	DC input logic High		VREF + 0.1	–	1.575	V	
VIL(DC)	DC input logic Low		–0.3	–	VREF – 0.1	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
SSTL15 DC Output Voltage Specification							
DDR3/SSTL15 Class I (DDR3 Reduced Drive)							
VOH	DC output logic High		0.8 * VDDI	–	–	V	
VOL	DC output logic Low		–	–	0.2 * VDDI	V	
IOH at VOH	Output minimum source DC current		6.5	–	–	mA	
IOL at VOL	Output minimum sink current		–6.5	–	–	mA	
SSTL15 Class II (DDR3 Full Drive)							
VOH	DC output logic High		0.8 * VDDI	–	–	V	
VOL	DC output logic Low		–	-	0.2 * VDDI	V	
IOH at VOH	Output minimum source DC current		7.6	–	–	mA	
IOL at VOL	Output minimum sink current		–7.6	–	–	mA	
SSTL15 Differential Voltage Specification							
VID (DC)	DC input differential voltage		0.2	–	–	V	
VDIFF (AC)	AC input differential voltage		0.7	–	–	V	
Vx (AC)	AC differential cross point voltage		0.5 * VDDI – 0.150	–	0.5 * VDDI + 0.150	V	

***Table 2-50* • SSTL15 DC Voltage Specification (for DDRIO I/O Bank Only) (continued)**

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
SSTL15 AC Specification							
Fmax	Maximum Data Rate (for DDRIO I/O bank)	AC loading: per JEDEC specifications			800	Mbps	
Rref	Supported output driver calibrated impedance	Reference resistor = 240 Ohms		34, 40		Ohms	
RTT	Effective impedance value (with respect to Reference Resistor 240 ohms) (ODT for DDRIO I/O bank only)	Reference resistor = 240 Ohms		20, 30, 40, 60, 120		Ohms	
AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	0.75	–	V	
Rent	Resistance for enable path (tZH, tZL, tHZ, tLZ)		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (tZH, tZL, tHZ, tLZ)		–	5	–	pF	
Rs	Series resistance for data test path (tDP)		–	25	–	Ohms	
Rtt_test	Reference resistance for data test path for SSTL15 Class I (tDP)		–	50	–	Ohms	
Rtt_test	Reference resistance for data test path for SSTL15 Class II (tDP)		–	25	–	Ohms	
Cload	Capacitive loading for data path (tDP)		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.425 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 2-51 • SSTL15 Receiver Characteristics

	On Die Termination (ODT)	TDIN		
		–1	Std.	Units
DDR3/SSTL15 (For DDRIO I/O bank)				
Pseudo-Differential	None	TBD	TBD	ns
	20	TBD	TBD	ns
	30	TBD	TBD	ns
	40	TBD	TBD	ns
	60	TBD	TBD	ns
	120	TBD	TBD	ns
True-Differential	None	TBD	TBD	ns
	20	TBD	TBD	ns
	30	TBD	TBD	ns
	40	TBD	TBD	ns
	60	TBD	TBD	ns
	120	TBD	TBD	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 2-52 • DDR3/SSTL15 Transmitter Characteristics

	TDOUT		TENZL		TENZH		TENHZ		TENLZ		
	–1	STD	–1	STD	–1	STD	–1	STD	–1	STD	Units
DDR3 Reduced Drive/SSTL15 Class I											
For DDRIO I/O Bank											
Single Ended	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Differential	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
DDR3 Full DriveSSTL15 Class II											
For DDRIO IO Bank											
Single Ended	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Differential	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns

Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in SmartFusion2 FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

***Table 2-53* • LPDDR DC Voltage Specification**

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply Voltage		1.71	1.8	1.89	V	
VTT	Termination Voltage		0.838	0.900	0.964	V	
VREF	Input Reference Voltage		0.838	0.900	0.964	V	
LPDDR DC Input Voltage Specification							
VIH (DC)	DC input Logic High		0.3 * VDDI	–	1.89	V	
VIL (DC)	DC input Logic Low		–0.3	–	0.7 * VDDI	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
LPDDR DC Output Voltage Specification							
VOH	DC output Logic High		0.9 * VDDI	–	–	V	
VOL	DC output Logic Low		–	–	0.1 * VDDI	V	
IOH at VOH	Output minimum source DC current		0.1	–	–	mA	
IOL at VOL	Output minimum sink current		–0.1	–	–	mA	
LPDDR Differential Voltage Specification							
VID (DC)	DC input differential voltage		0.4 * VDDI	–	–	V	
VDIFF (AC)	AC input differential voltage		0.6 * VDDI			V	
Vx (AC)	AC differential cross point voltage		0.4 * VDDI	–	0.6 * VDDI	V	
LPDDR AC Specifications							
Fmax	Maximum Data Rate	AC loading: per JEDEC specifications				Mbps	
Rref	Supported output driver calibrated impedance	Reference resistor = 150 Ohms		20, 42		Ohms	
Rtt	Effective impedance value – ODT	Reference resistor = 150 Ohms		50, 70, 150		Ohms	
AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	0.9	–	V	
Rent	Resistance for enable path (tZH, tZL, tHZ, tLZ)		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (tZH, tZL, tHZ, tLZ)		–	5	–	pF	
Rs	Series resistance for data test path (tDP)		–	25	–	Ohms	
Rtt_test	Reference resistance for data test path for LPDDR (tDP)		–	50	–	Ohms	
Cload	Capacitive loading for data path (tDP)		–	5	–	Ohms	

AC Switching Characteristics

Table 2-54 • LPDDR Receiver Characteristics

	On Die Termination (ODT)	TDIN		Units
		–1	Std.	
LPDDR (for DDRIO I/O Bank)				
Pseudo-Differential	None	TBD	TBD	ns
True-Differential	None	TBD	TBD	ns
	50	TBD	TBD	ns
	75	TBD	TBD	ns
	150	TBD	TBD	ns

Table 2-55 • LPDDR Transmitter Characteristics

	TDOUT		TENZL		TENZH		TENHZ		TENLZ		
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	Units
LPDDR Reduced Drive											
For DDRIO I/O Bank											
Single-ended	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Differential	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
LPDDR Full Drive											
For DDRIO I/O Bank											
Single-ended	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Differential	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns

Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by SoC Products Group Libero software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

Minimum and Maximum Input and Output Levels

***Table 2-56* • LVDS DC Voltage Specification**

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply Voltage		2.375	2.5	3.45	V	
LVDS DC Input Voltage Specification							
VI	DC Input voltage		0	–	2.925	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
LVDS DC Output Voltage Specification							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
LVDS Differential Voltage Specification							
VOD	Differential output voltage swing		250	350	450	mV	
VOCM	Output common mode voltage		1.125	1.25	1.375	V	
VICM	Input common mode voltage		0.05	1.25	1.375	V	
VID	Input differential voltage		100	350	600	mV	
LVDS AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	535	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – NO PRE-EMPHASIS	AC loading: 2 pF / 100 Ohm differential load	700	730	750	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – MIN. PRE-EMPHASIS	AC loading: 2 pF / 100 Ohm differential load	970	1200	1270	Mbps	
Fmax	Maximum Data Rate (for MSIOD IO Bank) – MAX. PRE-EMPHASIS	AC loading: 2 pF / 100 Ohm differential load	1000	1500	1700	Mbps	
Rt	Termination resistance		–	100	–	Ohms	
AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (tZH, tZL, tHZ, tLZ)		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (tZH, tZL, tHZ, tLZ)		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 2-57 • LVDS Receiver Characteristics

	On Die Termination (ODT)	TDIN		TSCH_DIN		Units
		–1	Std.	–1	Std.	
LVDS (for MSIO I/O bank)	None	TBD	TBD	TBD	TBD	ns
	100	TBD	TBD	TBD	TBD	ns
LVDS (for MSIOD I/O bank)	None	TBD	TBD	TBD	TBD	ns
	100	TBD	TBD	TBD	TBD	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 2-58 • LVDS Transmitter Characteristics

	TDOUT		TENZL		TENZH		TENHZ		TENLZ		Units
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVDS (For MSIO I/O bank)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
LVDS (For MSIOD I/O bank)											
No pre-emphasis	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Min. pre-emphasis	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Max. pre-emphasis	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns

B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 2-59 • B-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply Voltage		2.375	2.5	2.625	V	
Bus LVDS DC Input Voltage Specification							
VI	DC input voltage		0	–	2.925	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
Bus LVDS DC Output Voltage Specification (For MSIO I/O Bank ONLY)							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
Bus LVDS Differential Voltage Specification							
VOD	Differential output voltage swing (for MSIO I/O bank ONLY)		240	–	460	mV	
VOCM	Output common mode voltage (for MSIO I/O bank ONLY)		1.1	–	1.5	V	
VICM	Input common mode voltage		0.05	–	2.4 – VID/2	V	
VID	Input differential voltage		100	–	2 * VDDI	mV	
Bus LVDS AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	500	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank, receiver ONLY)		–	–	–	Mbps	
Rt	Termination resistance		–	27	–	Ohms	
Bus LVDS AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (tZH, tZL, tHZ, tLZ)		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (tZH, tZL, tHZ, tLZ)		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 2-60 • AC Switching Characteristics for Receiver (Input Buffers)

	On Die Termination (ODT)	TDIN		TSCH_DIN		Units
		Speed Grade		Speed Grade		
		–1	Std.	–1	Std.	
Bus LVDS (For MSIO I/O Bank)	None	TBD	TBD	TBD	TBD	ns
	100	TBD	TBD	TBD	TBD	ns
Bus LVDS (For MSIOD I/O Bank)	None	TBD	TBD	TBD	TBD	ns
	100	TBD	TBD	TBD	TBD	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 2-61 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers

	TDOUT		TENZL		TENZH		TENHZ		TENLZ		
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	Units
Bus-LVDS (For MSIO I/O Bank)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns

M-LVDS

MLVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

Minimum and Maximum Input and Output Levels

Table 2-62 • M-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
M-LVDS Recommended DC Operating Conditions							
VDDI	Supply Voltage		2.375	2.5	2.625	V	
M-LVDS DC Input Voltage Specification							
VI	DC input voltage		0	–	2.925	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
M-LVDS DC Output Voltage Specification (For MSIO IO Bank ONLY)							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
M-LVDS Differential Voltage Specification							
VOD	Differential output voltage Swing (for MSIO I/O bank ONLY)		480	–	650	mV	
VOCM	Output common mode voltage (for MSIO I/O bank ONLY)		0.3	–	2.1	V	
VICM	Input common mode voltage		0.3	–	1.2	V	
VID	Input differential voltage		50	–	2400	mV	
M-LVDS AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	500	Mbps	
Rt	Termination resistance		–	50	–	Ohms	
M-LVDS AC Test Parameters Specifications							
VTrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (tZH, tZL, tHZ, tLZ)		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (tZH, tZL, tHZ, tLZ)		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 2-63 • AC Switching Characteristics for Receiver (Input Buffers)

	On Die Termination (ODT)	TDIN		TSCH_DIN		Units
		Speed Grade		Speed Grade		
		–1	Std.	–1	Std.	
MLVDS (For MSIO I/O Bank)	None	TBD	TBD	TBD	TBD	ns
	100	TBD	TBD	TBD	TBD	ns
MLVDS (For MSIOD I/O Bank)	None	TBD	TBD	TBD	TBD	ns
	100	TBD	TBD	TBD	TBD	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 2-64 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	TDOUT		TENZL		TENZH		TENHZ		TENLZ		
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	Units
M-LVDS (For MSIO I/O Bank)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns

Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

Mini-LVDS Minimum and Maximum Input and Output Levels

Table 2-65 • Mini-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply Voltage		2.375	2.5	2.625	V	
Mini-LVDS DC Input Voltage Specification							
VI	DC Input voltage		0	–	2.925	V	
Mini-LVDS DC Output Voltage Specification							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
Mini-LVDS Differential Voltage Specification							
VOD	Differential output voltage swing		300	–	600	mV	
VOCM	Output common mode voltage		1	–	1.4	V	
VICM	Input common mode voltage		0.3	–	1.2	V	
VID	Input differential voltage		200	–	600	mV	
Mini-LVDS AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	520	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank, No Pre-Emphasis)	AC loading: 2 pF / 100 Ohm differential load	700	725	740	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – Min. Pre-Emphasis	AC loading: 2 pF / 100 Ohm differential load	700	735	750	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – Med. Pre-Emphasis	AC loading: 2 pF / 100 Ohm differential load	970	1,200	1,280	Mbps	
Fmax	Maximum Data Rate (for MSIOD I/O bank) – Max. Pre-Emphasis	AC loading: 2 pF / 100 Ohm differential load	1,000	1,500	1,700	Mbps	
Rt	Termination resistance		50		150	Ohms	
Mini-LVDS AC Test Parameters Specifications							
VTrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (tZH, tZL, tHZ, tLZ)		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (tZH, tZL, tHZ, tLZ)		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 2-66 • AC Switching Characteristics for Receiver (Input Buffers)

	On Die Termination (ODT)	TDIN		TSCH_DIN		Units
		Speed Grade		Speed Grade		
		–1	Std.	–1	Std.	
Mini-LVDS (For MSIO I/O Bank)	None	TBD	TBD	TBD	TBD	ns
	100	TBD	TBD	TBD	TBD	ns
Mini-LVDS (For MSIOD I/O Bank)	None	TBD	TBD	TBD	TBD	ns
	100	TBD	TBD	TBD	TBD	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 2-67 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	TDOUT		TENZL		TENZH		TENHZ		TENLZ		Units
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
Mini-LVDS (for MSIO I/O bank)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Mini-LVDS (for MSIOD I/O bank)											
No Pre-Emphasis	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Min. Pre-Emphasis	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Max. Pre-Emphasis	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns

RSDS

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

Minimum and Maximum Input and Output Levels

Table 2-68 • RSDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply Voltage		2.375	2.5	2.625	V	
RSDS DC Input Voltage Specification							
VI	DC input voltage		0	–	2.925	V	
RSDS DC Output Voltage Specification							
VOH	DC output Logic High		1.25	1.425	1.6	V	
VOL	DC output Logic Low		0.9	1.075	1.25	V	
RSDS Differential Voltage Specification							
VOD	Differential output voltage swing		100	–	600	mV	
VOCM	Output common mode voltage		0.5	–	1.5	V	
VICM	Input common mode voltage		0.3	–	1.5	V	
VID	Input differential voltage		100	–	2 * VDDI	mV	
RSDS AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	520	Mbps	
Fmax	Maximum data Rate (for MSIOD I/O banks, No Pre-Emphasis)	AC loading: 2 pF / 100 Ohm differential load	700	725	740	Mbps	
Fmax	Maximum Data Rate (for MSIOD I/O Banks) – Min. Pre-Emphasis	AC loading: 2 pF / 100 Ohm differential load	700	735	750	Mbps	
Fmax	Maximum data rate (for MSIOD I/O banks) – Med. Pre-Emphasis	AC loading: 2 pF / 100 Ohm differential load	970	1200	1,280	Mbps	
Fmax	Maximum data rate (for MSIOD I/O banks) – Max. Pre-Emphasis)	AC loading: 2 pF / 100 Ohm differential load	1,000	1,500	1,700	Mbps	
Rt	Termination Resistance			100		Ohms	
AC Test Parameters Specifications							
VTrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (tZH, tZL, tHZ, tLZ)		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (tZH, tZL, tHZ, tLZ)		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 2-69 • AC Switching Characteristics for Receiver (Input Buffers)

	On Die Termination (ODT)	TDIN		TSCH_DIN		Units
		Speed Grade		Speed Grade		
		–1	Std.	–1	Std.	
RSDS (for MSIO I/O bank)	None	TBD	TBD	TBD	TBD	ns
	100	TBD	TBD	TBD	TBD	ns
RSDS (for MSIOD I/O bank)	None	TBD	TBD	TBD	TBD	ns
	100	TBD	TBD	TBD	TBD	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 2-70 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	TDOUT		TENZL		TENZH		TENHZ		TENLZ		Units
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
RSDS (for MSIO I/O bank)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
RSDS (for MSIOD I/O bank)											
No Pre-Emphasis	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Min. Pre-Emphasis	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
Max. Pre-Emphasis	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. SmartFusion2 devices support only LVPECL receivers and do not support LVPECL transmitters.

Minimum and Maximum Input and Output Levels

Table 2-71 • LVPECL DC Voltage Specification – Applicable to MSIO I/O Banks Only

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply Voltage		3.15	3.3	3.45	V	
LVPECL DC Input Voltage Specification							
VIH (DC)	DC input logic High		–	–	2.3	V	
VIL (DC)	DC input logic Low		1.6	–	–	V	
LVPECL Differential Voltage Specification							
VICM	Input common mode voltage		0.3		2.8	V	
VIDIFF	Input differential voltage		100	300	1,000	mV	
Other Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)		–	–	900	Mbps	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 2-72 • LVPECL Receiver Characteristics

	On Die Termination (ODT)	TDIN		TSCH_DIN		Units
		–1	Std.	–1	Std.	
LVPECL (for MSIO I/O bank)	None	TBD	TBD	TBD	TBD	ns
	100	TBD	TBD	TBD	TBD	ns

I/O Register Specifications

Input Register

Table 2-73 • Input Data Enable Register Propagation Delays
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Measuring Nodes (from, to)*	–1	Std.	Units
tICLKQ	Clock-to-Q of the Input Data Register		TBD	TBD	ns
tISUD	Data Setup Time for the Input Data Register		TBD	TBD	ns
tIHD	Data Hold Time for the Input Data Register		TBD	TBD	ns
tISUE	Enable Setup Time for the Input Data Register		TBD	TBD	ns
tIHE	Enable Hold Time for the Input Data Register		TBD	TBD	ns
tICLR2Q	Asynchronous Clear-to-Q of the Input Data Register		TBD	TBD	ns
tIPRE2Q	Asynchronous Preset-to-Q of the Input Data Register		TBD	TBD	ns
tIREMCLR	Asynchronous Clear Removal Time for the Input Data Register		TBD	TBD	ns
tIRECCLR	Asynchronous Clear Recovery Time for the Input Data Register		TBD	TBD	ns
tIREMPRE	Asynchronous Preset Removal Time for the Input Data Register		TBD	TBD	ns
tIRECPRE	Asynchronous Preset Recovery Time for the Input Data Register		TBD	TBD	ns
tIWCLR	Asynchronous Clear Minimum Pulse Width for the Input Data Register		TBD	TBD	ns
tIWPRE	Asynchronous Preset Minimum Pulse Width for the Input Data Register		TBD	TBD	ns
tICKMPWH	Clock Minimum Pulse Width High for the Input Data Register		TBD	TBD	ns
tICKMPWL	Clock Minimum Pulse Width Low for the Input Data Register		TBD	TBD	ns

*For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-11 on page 2-14 for derating values.

Output/Enable Register

Table 2-74 • Output Data/Enable Register Propagation Delays
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Measuring Nodes (from, to)*	–1	Std.	Units
tOCLKQ	Clock-to-Q of the Output/Enable Register		TBD	TBD	ns
tOSUD	Data Setup Time for the Output/Enable Register		TBD	TBD	ns
tOHD	Data Hold Time for the Output/Enable Register		TBD	TBD	ns
tOSUE	Enable Setup Time for the Output/Enable Register		TBD	TBD	ns
tOHE	Enable Hold Time for the Output/Enable Register		TBD	TBD	ns
tOSUSL	Synchronous Load Setup Time for the Output/Enable Register		TBD	TBD	ns
tOHSL	Synchronous Load Hold Time for the Output/Enable Register		TBD	TBD	ns
tOALn2Q	Asynchronous Clear-to-Q of the Output/Enable Register (ADn = 1)		TBD	TBD	ns
	Asynchronous Preset-to-Q of the Output/Enable Register (ADn = 0)		TBD	TBD	ns
tOREMALn	Asynchronous Load Removal Time for the Output/Enable Register		TBD	TBD	ns
tORECALn	Asynchronous Load Recovery Time for the Output/Enable Register		TBD	TBD	ns
tOWALn	Asynchronous Load Minimum Pulse Width for the Output/Enable Register		TBD	TBD	ns
tOCKMPWH	Clock Minimum Pulse Width High for the Output/Enable Register		TBD	TBD	ns
tOCKMPWL	Clock Minimum Pulse Width Low for the Output/Enable Register		TBD	TBD	ns

*Note: *For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-11 on page 2-14 for derating values.*

DDR Module Specification

Input DDR Module

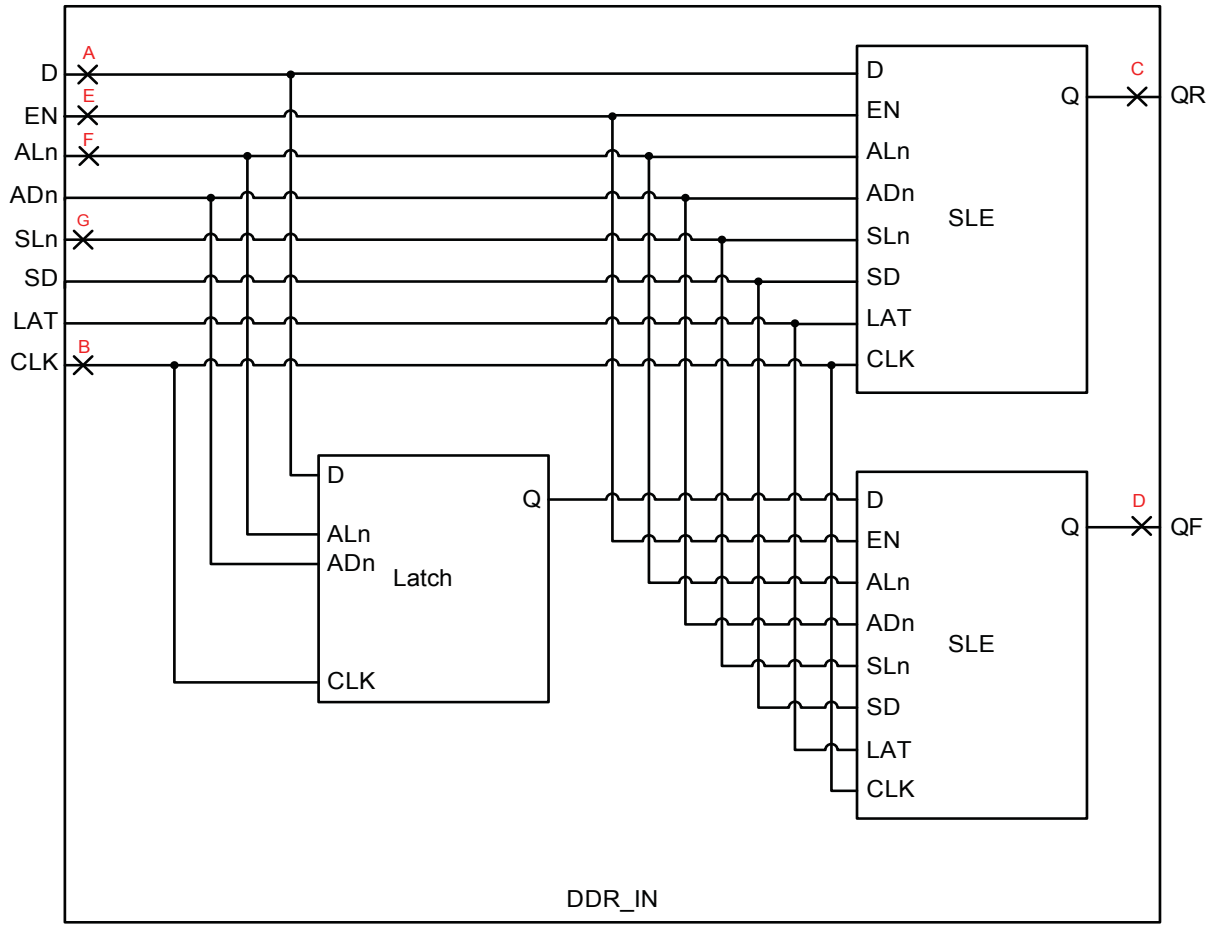


Figure 2-2 • **Input DDR Module**

Input DDR Timing Diagram

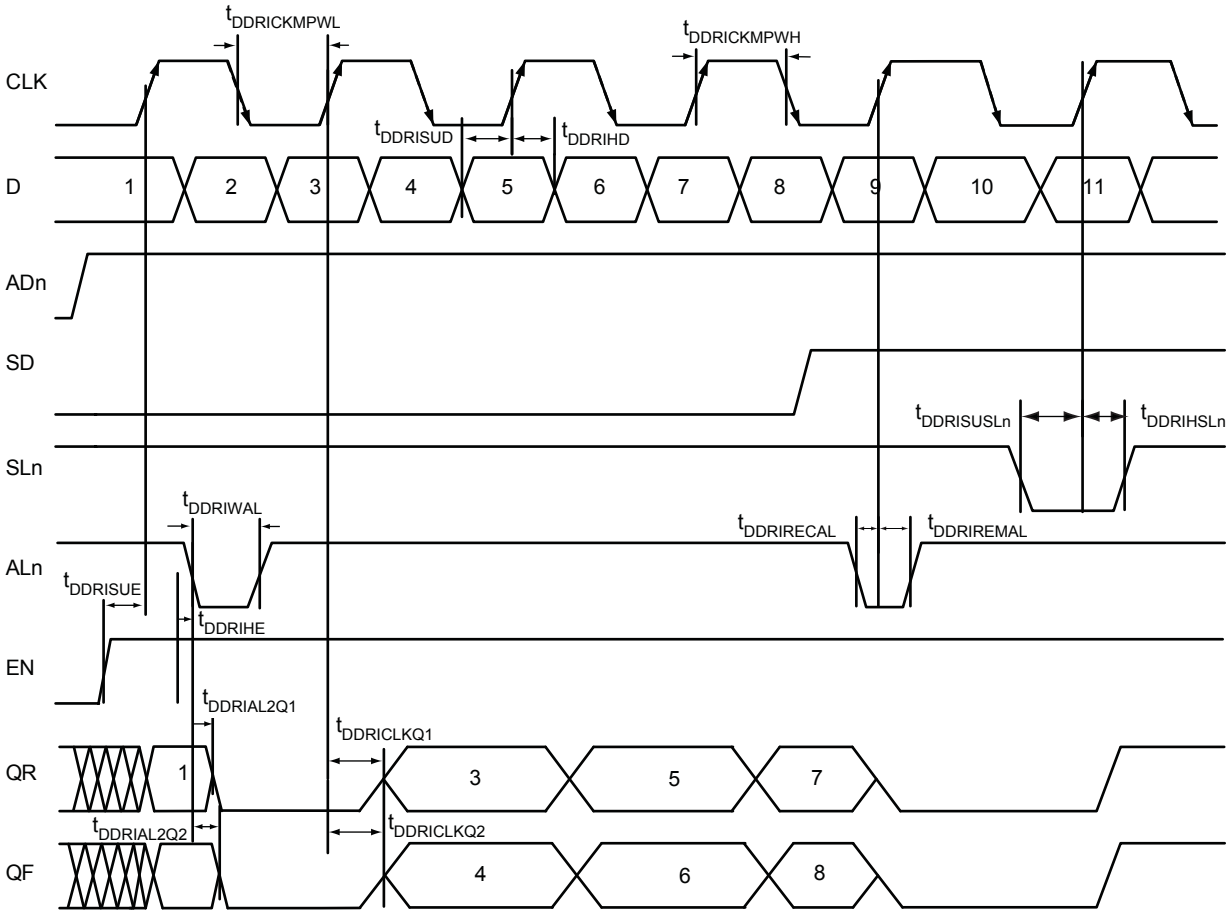


Figure 2-3 • **Input DDR Timing Diagram**

Timing Characteristics

***Table 2-75* • Input DDR Propagation Delays**

Parameter	Description	Measuring Nodes (from, to)	–1	Std.	Units
tDDRICLKQ1	Clock-to-Out Out_QR for Input DDR	B, C	0.178	0.209	ns
tDDRICLKQ2	Clock-to-Out Out_QF for Input DDR	B, D	0.175	0.205	ns
tDDRISUD	Data Setup for Input DDR	A, B	0.464	0.546	ns
tDDRIHD	Data Hold for Input DDR	A, B	0	0	ns
tDDRISUE	Enable Setup for Input DDR	E, B	TBD	TBD	ns
tDDRIHE	Enable Hold for Input DDR	E, B	0	0	ns
tDDRISUSLn	Synchronous Load Setup for Input DDR	G, B	0.577	0.679	ns
tDDRIHSLn	Synchronous Load Hold for Input DDR	G, B	0	0	ns
tDDRIAL2Q1	Asynchronous Load-to-Out QR for Input DDR	F, C	0.618	0.727	ns
tDDRIAL2Q2	Asynchronous Load-to-Out QF for Input DDR	F, D	0.569	0.67	ns
tDDRIREMAL	Asynchronous Load Removal time for Input DDR	F, B	0	0	ns
tDDRIRECAL	Asynchronous Load Recovery time for Input DDR	F, B	0.041	0.048	ns
tDDRIWAL	Asynchronous Load Minimum Pulse Width for Input DDR	F, F	0.32	0.376	ns
tDDRICKMPWH	Clock Minimum Pulse Width High for Input DDR	B, B	0.08	0.094	ns
tDDRICKMPWL	Clock Minimum Pulse Width Low for Input DDR	B, B	0.068	0.08	ns

Output DDR Module

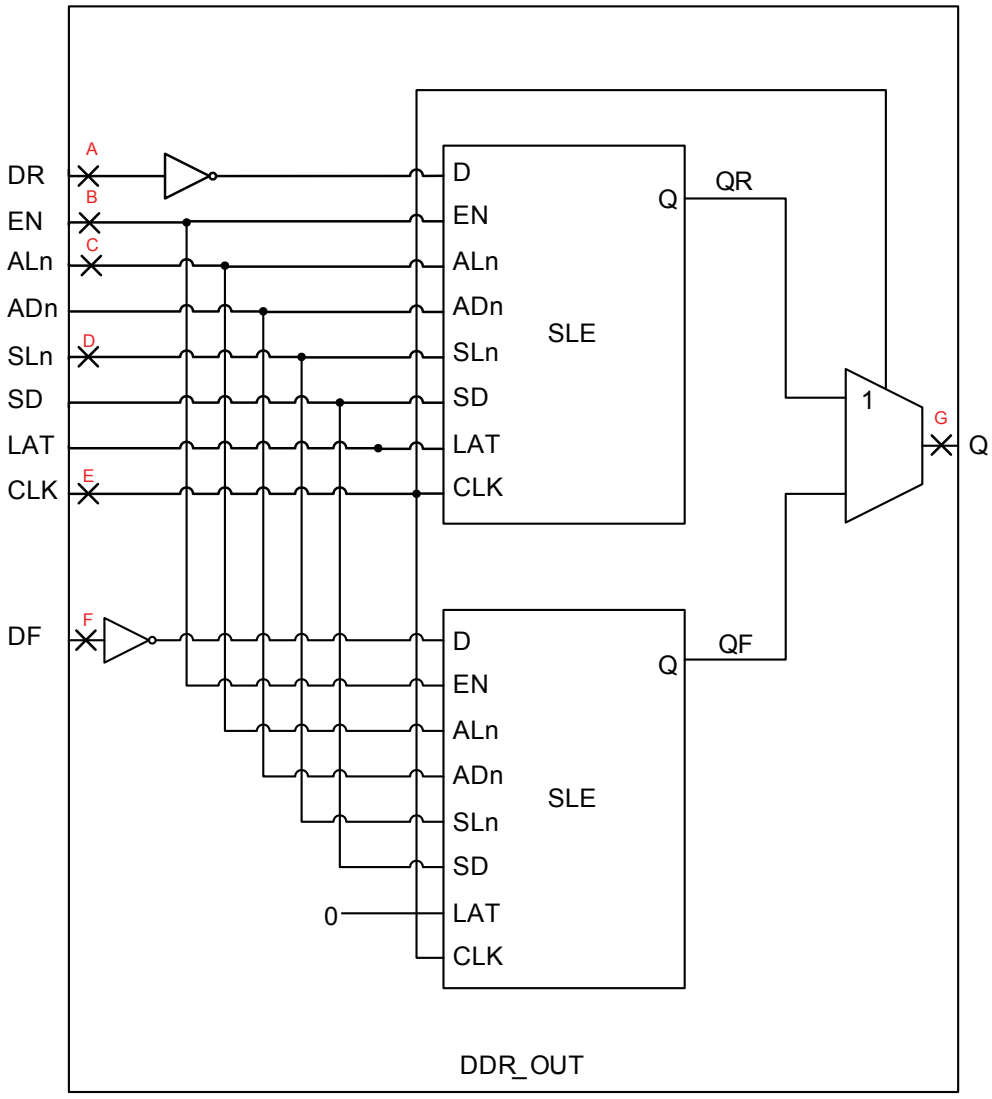


Figure 2-4 • **Output DDR Module**

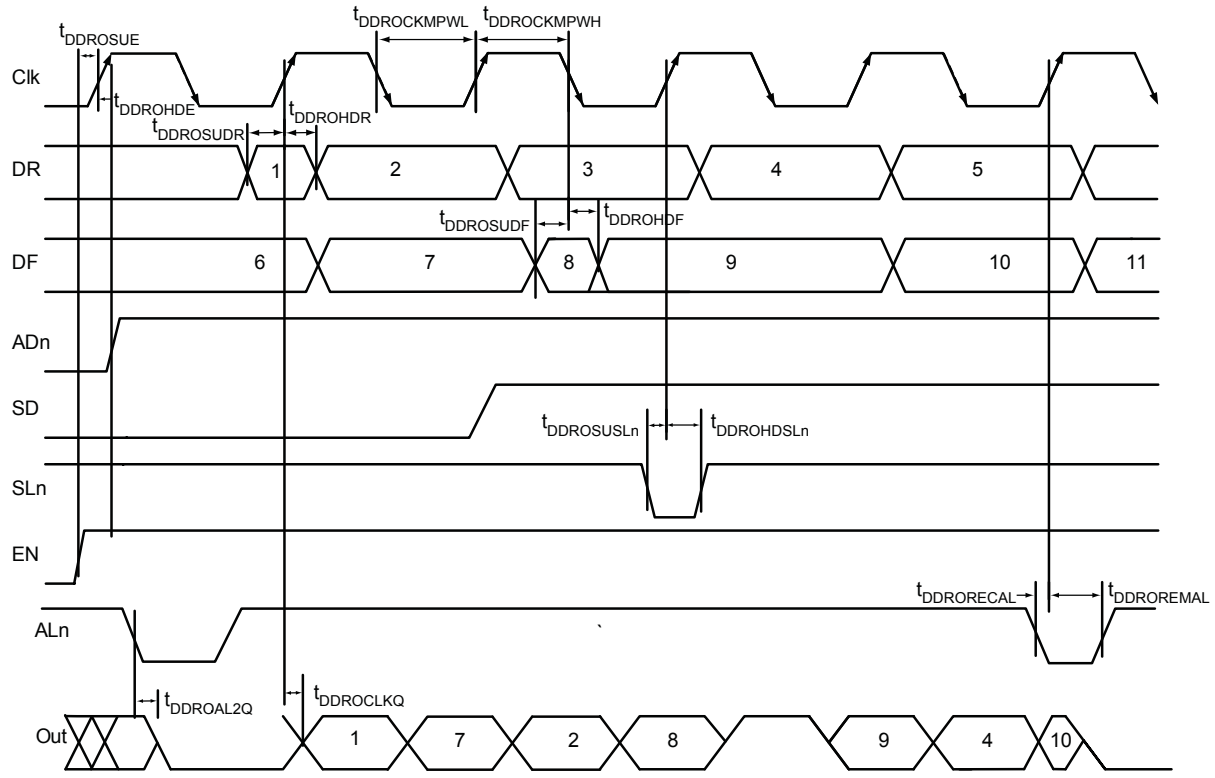


Figure 2-5 • **Output DDR Timing Diagram**

Timing Characteristics

Table 2-76 • Output DDR Propagation Delays

Parameter	Description	Measuring Nodes (from, to)	–1	Std.	Units
tDDROCLKQ	Clock-to-Out of DDR for Output DDR	E, G	0.288	0.339	ns
tDDROSUDF	Data_F Data Setup for Output DDR	F, E	0.154	0.181	ns
tDDROSUDR	Data_R Data Setup for Output DDR	A, E	TBD	TBD	ns
tDDROHDF	Data_F Data Hold for Output DDR	F, E	0	0	ns
tDDROHDR	Data_R Data Hold for Output DDR	A, E	0	0	ns
tDDROSUE	Enable Setup for Input DDR	B, E	0.148	0.174	ns
tDDROHE	Enable Hold for Input DDR	B, E	0	0	ns
tDDROSUSLn	Synchronous Load Setup for Input DDR	D, E	0.79	0.93	ns
tDDROHSLn	Synchronous Load Hold for Input DDR	D, E	0	0	ns
tDDROAL2Q	Asynchronous Load-to-Out for Output DDR	C, G	0.575	0.677	ns
tDDROREMAL	Asynchronous Load Removal time for Output DDR	C, E	0	0	ns
tDDRORECAL	Asynchronous Load Recovery time for Output DDR	C, E	0.775	0.911	ns
tDDROWAL	Asynchronous Load Minimum Pulse Width for Output DDR	C, C	0.191	0.224	ns
tDDROCKMPWH	Clock Minimum Pulse Width High for the Output DDR	E, E	0.101	0.119	ns
tDDROCKMPWL	Clock Minimum Pulse Width Low for the Output DDR	E, E	0.156	0.184	ns

Logic Module Specifications

4-input LUT (LUT-4)

The SmartFusion2 offers a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library.

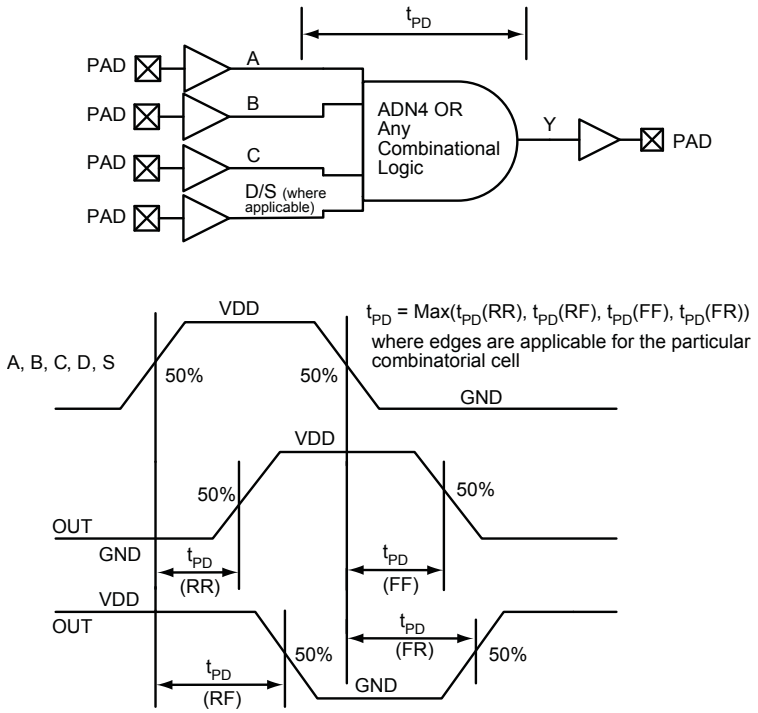


Figure 2-6 • **LUT-4**

Timing Characteristics

Table 2-77 • **Combinatorial Cell Propagation Delays**

Combinatorial Cell	Equation	Parameter	–1	Std.	Units	Notes
INV	Y = !A	tPD	0.108	0.127	ns	
AND2	Y = A · B	tPD	0.172	0.203	ns	
NAND2	Y = !(A · B)	tPD	0.16	0.188	ns	
OR2	Y = A + B	tPD	0.172	0.203	ns	
NOR2	Y = !(A + B)	tPD	0.16	0.188	ns	
XOR2	Y = A ⊕ B	tPD	0.172	0.203	ns	
XOR3	Y = A ⊕ B ⊕ C	tPD	0.24	0.283	ns	
AND3	Y = A · B · C	tPD	0.22	0.259	ns	
AND4	Y = A · B · C · D	tPD	0.493	0.58	ns	

Sequential Module

SmartFusion2 offers a separate flip flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

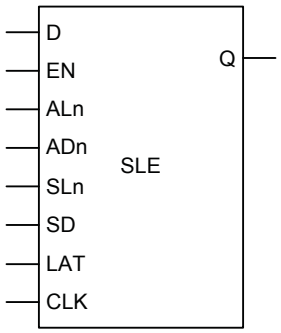


Figure 2-7 • **Sequential Module**

Figure 2-8 shows a configuration with SD = 1 (synchronous preset) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

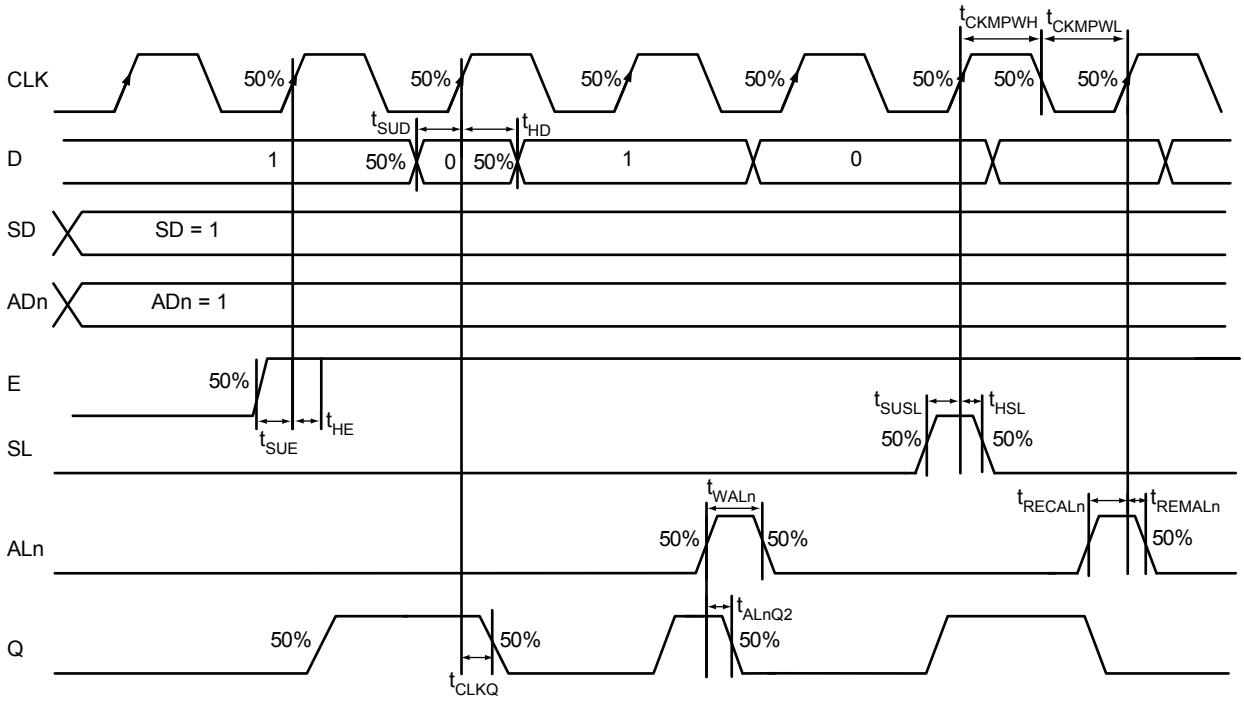


Figure 2-8 • **Timing Diagram**

Timing Characteristics

***Table 2-78* • Register Delays**

Parameter	Description	–1	Std.	Units	Notes
tCLKQ	Clock-to-Q of the Core Register	0.114	0.134	ns	
tSUD	Data Setup Time for the Core Register	0.267	0.314	ns	
tHD	Data Hold Time for the Core Register	0	0	ns	
tSUE	Enable Setup Time for the Core Register	0.353	0.415	ns	
tHE	Enable Hold Time for the Core Register	0	0	ns	
tSUSL	Synchronous Load Setup Time for the Core Register	0.353	0.415	ns	
tHSL	Synchronous Load Hold Time for the Core Register	0	0	ns	
tALn2Q	Asynchronous Clear-to-Q of the Core Register (ADn = 1)	0.498	0.586	ns	
	Asynchronous Preset-to-Q of the Core Register (ADn = 0)	0.475	0.559	ns	
tREMALn	Asynchronous Load Removal Time for the Core Register	0	0	ns	
tRECALn	Asynchronous Load Recovery Time for the Core Register	0.371	0.437	ns	
tWALn	Asynchronous Load Minimum Pulse Width for the Core Register	0.32	0.376	ns	
tCKMPWH	Clock Minimum Pulse Width High for the Core Register	0.079	0.093	ns	
tCKMPWL	Clock Minimum Pulse Width Low for the Core Register	0.168	0.197	ns	

Global Resource Characteristics

SmartFusion2 devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. Refer to the *SmartFusion2 FPGA Fabric Architecture User's Guide* for the positions of various global routing resources.

***Table 2-79* • M2S050T Global Resource**

Parameter	Description	Speed Grade				Units	Notes
		–1		Std.			
		Min.	Max.	Min.	Max.		
tRCKL	Input Low Delay for Global Clock	TBD	TBD	TBD	TBD	ns	
tRCKH	Input High Delay for Global Clock	TBD	TBD	TBD	TBD	ns	
tRCKMPWH	Minimum Pulse Width High for Global Clock	TBD	TBD	TBD	TBD	ns	
tRCKMPWL	Minimum Pulse Width Low for Global Clock	TBD	TBD	TBD	TBD	ns	
tRCKSW	Maximum Skew for Global Clock	TBD	TBD	TBD	TBD	ns	

FPGA Fabric SRAM

Refer to the *SmartFusion2 FPGA Fabric Architecture User's Guide* for more information.

FPGA Fabric Large SRAM (LSRAM)

***Table 2-80* • RAM1K18**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
tcy	Clock Period	1.656	–	1.948	–	ns
tclkmpwh	Clock Minimum Pulse Width High	0.828	–	0.974	–	ns
tclkmpwl	Clock Minimum pulse Width Low	0.327	–	0.384	–	ns
tplcy	Pipelined Clock Period	1.652	–	1.944	–	ns
tplclkmpwh	Pipelined Clock Minimum Pulse Width High	0.826	–	0.972	–	ns
tplclkmpwl	Pipelined Clock Minimum pulse Width Low	0.324	–	0.381	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.337	–	0.396	ns
	Read Access Time without Pipeline Register	–	TBD	–	TBD	ns
	Access Time with Feed-Through Write Timing	–	TBD	–	TBD	ns
taddrsu	Address Setup Time	0.207	–	0.244	–	ns
taddrhd	Address Hold Time	0.041	–	0.048	–	ns
tdsu	Data Setup Time	0.33	–	0.389	–	ns
tdhd	Data Hold Time	0.074	–	0.087	–	ns
tblksu	Block Select Setup Time (With Pipe-Line Register Enabled)	0.188	–	0.221	–	ns
tblkhd	Block Select Hold Time (With Pipe-Lined Register Enabled)	0.079	–	0.093	–	ns
tblk2q	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	TBD	–	TBD	ns
	Block Select to Out Enable Time (when Pipe-Lined Registered is Disabled)	–	TBD	–	TBD	ns
tblkmpw	Block Select Minimum Pulse Width	TBD	–	TBD	–	ns
trdesu	Read Enable Setup Time (A_WEN, B_WEN =0)	0.465	–	0.547	–	ns
trdehd	Read Enable Hold Time (A_WEN, B_WEN =0)	0.053	–	0.063	–	ns
trdplesu	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.703	–	0.827	–	ns
trdplehd	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	–0.053	–	–0.062	–	ns
tr2q	Asynchronous Reset to Output Propagation Delay	-	0.792	–	0.931	ns
trstrem	Asynchronous Reset Removal Time	TBD	–	TBD	–	ns
trstrec	Asynchronous Reset Recovery Time	0.005	–	0.006	–	ns
trstmpw	Asynchronous Reset Minimum Pulse Width	0.323	–	0.38	–	ns
tplrstrem	Pipelined Register Asynchronous Reset Removal Time	TBD	–	TBD	–	ns
tplrstrec	Pipelined Register Asynchronous Reset Recovery Time	0.344	–	0.405	–	ns
tplrstmpw	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.307	–	0.361	–	ns
tsrstsu	Synchronous Reset Setup Time	0.231	–	0.271	–	ns

***Table 2-80* • RAM1K18**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
tsrsthd	Synchronous Reset Hold Time	TBD	–	TBD	–	ns
twesu	Write Enable Setup Time (A_WEN, B_WEN = 1)	0.403	–	0.474	–	ns
twehd	Write Enable Hold Time (A_WEN, B_WEN = 1)	0.061	–	0.072	–	ns

FPGA Fabric Micro SRAM (uSRAM)

***Table 2-81* • uSRAM (RAM64x18) in 64x18 Mode**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
tcy	Read Clock Period	0.65	–	0.766	–	ns
tclkmpwh	Read Clock Minimum Pulse Width High	0.296	–	0.348	–	ns
tclkmpwl	Read Clock Minimum pulse Width Low	0.325	–	0.383	–	ns
tplcy	Read Pipe-line clock period	0.622	–	0.732	–	ns
tplclkmpwh	Read Pipe-line clock Minimum Pulse Width High	0.281	–	0.331	–	ns
tplclkmpwl	Read Pipe-line clock Minimum Pulse Width Low	0.311	–	0.366	–	ns
tclpl1	Minimum pipe-line clock low phase in order to prevent glitches with Pipeline Register in Latch Mode	TBD	–	TBD	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.368	–	0.433	ns
	Read Access Time with Pipeline Register in Latch Mode	–	TBD	–	TBD	ns
	Read Access Time without Pipeline Register	–	1.777	–	2.09	ns
taddrsu	Read Address Setup Time in Synchronous Mode	0.172	–	0.202	–	ns
	Read Address Setup Time in Asynchronous Mode	1.059	–	1.246	–	ns
taddrhd	Read Address Hold Time in Synchronous Mode	0.028	–	0.033	–	ns
	Read Address Hold Time in Asynchronous Mode	0.008	–	0.01	–	ns
trdensu	Read Enable Setup Time	0.245	–	0.289	–	ns
trdenhd	Read Enable Hold Time	0.074	–	0.087	–	ns
tblksu	Read Block Select Setup Time (With Pipe-Line Register Enabled)	0.301	–	0.355	–	ns
tblkhd	Read Block Select Hold Time (With Pipe-Lined Register Enabled)	TBD	–	TBD	–	ns
tblk2q	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.093	–	2.462	ns
	Read Block Select to Out Enable Time (when Pipe-Lined Registered is Disabled)	–	1.503	–	1.768	ns
tblkmpw	Read Block Select Minimum Pulse Width	TBD	–	TBD	–	ns
trstrem	Read Asynchronous Reset Removal Time (Pipelined Clock)	–0.002	–	–0.002	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.03	–	0.036	–	ns

***Table 2-81* • uSRAM (RAM64x18) in 64x18 Mode (continued)**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
trstrec	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.546	–	0.642	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.085	–	0.099	–	ns
tr2q	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.938	-	1.103	ns
	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Disabled)	–	1.588	-	1.868	ns
tsrstsu	Read Synchronous Reset Setup Time	0.189	–	0.222	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.074	–	0.087	–	ns
tccy	Write Clock Period	1.012	–	1.192	–	ns
tcclkmpwh	Write Clock Minimum Pulse Width High	0.506	–	0.596	–	ns
tcclkmpwl	Write Clock Minimum Pulse Width Low	0.297	–	0.349	–	ns
tblkcsu	Write Block Setup Time	0.332	–	0.39	–	ns
tblkchd	Write Block Hold Time	TBD	–	TBD	–	ns
tdincsu	Write Input Data setup Time	TBD	–	TBD	–	ns
tdinchd	Write Input Data hold Time	0.002	–	0.003	–	ns
taddrcsu	Write Address Setup Time	TBD	–	TBD	–	ns
taddrchd	Write Address Hold Time	TBD	–	TBD	–	ns
twecsu	Write Enable Setup Time	0.32	–	0.377	–	ns
twechd	Write Enable Hold Time	TBD	–	TBD	–	ns

On-Chip Oscillators

Table 2-82 through Table 2-84 on page 2-81 describe the electrical characteristics of the available on-chip oscillators in SmartFusion2 devices.

***Table 2-82* • Electrical Characteristics of the Crystal Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units	Notes
FXTAL	Operating frequency		–	32	–	kHz	
ACCXTAL	Accuracy	Temperature: 0°C to 85°C	TBD	TBD	TBD	%	
CYCXTAL	Output duty cycle		TBD	TBD	TBD	%	
JITXTAL	Output jitter	Period jitter	TBD	TBD	TBD	ps RMS	
		Cycle-to-Cyle jitter	TBD	TBD	TBD	ps	
IDYNXTAL	Operating current		TBD	TBD	TBD	mA	
ISTBXTAL	Standby current of crystal oscillator		TBD	TBD	TBD	µA	
PSRRXTAL	Power supply noise tolerance		TBD	TBD	TBD	Vp-p	
ENXTAL	Enable Time		TBD	TBD	TBD	µs	
VIHXTAL	Input logic level High		TBD	TBD	TBD	V	
VILXTAL	Input logic level Low		TBD	TBD	TBD	V	
SUXTAL	Startup time	Test load used:	TBD	TBD	TBD	µs	

***Table 2-83* • Electrical Characteristics of the 25/50 MHz RC Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units	Notes
F25_50RC	Operating frequency		–	25/50	–	MHz	
ACC25_50RC	Accuracy	Temperature: 0°C to 85°C	TBD	TBD	TBD	%	
CYC25_50RC	Output duty cycle		TBD	TBD	TBD	%	
JIT25_50RC	Output jitter	Period Jitter	TBD	TBD	TBD	ps RMS	
		Cycle-to-Cyle Jitter	TBD	TBD	TBD	ps	
IDYN25_50RC	Operating current		TBD	TBD	TBD	mA	
ISTB25_50RC	Standby current of crystal oscillator		TBD	TBD	TBD	µA	
PSRR25_50RC	Power supply noise tolerance		TBD	TBD	TBD	Vp-p	
VIH25_50RC	Input logic level High		TBD	TBD	TBD	V	
VIL25_50RC	Input logic level Low		TBD	TBD	TBD	V	
SU25_50RC	Startup time	Test load used:	TBD	TBD	TBD	µs	

***Table 2-84* • Electrical Characteristics of the 1 MHz RC Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units	Notes
F1RC	Operating frequency		–	1	–	MHz	
ACC1RC	Accuracy	Temperature: 0°C to 85°C	TBD	TBD	TBD	%	
CYC1RC	Output duty cycle		TBD	TBD	TBD	%	
JIT1RC	Output jitter	Period Jitter	TBD	TBD	TBD	ps RMS	
		Cycle-to-Cyle Jitter	TBD	TBD	TBD	ps	
IDYN1RC	Operating current		TBD	TBD	TBD	mA	
ISTB1RC	Standby current of crystal oscillator		TBD	TBD	TBD	µA	
PSRR1RC	Power supply noise tolerance		TBD	TBD	TBD	Vp-p	
EN1RC	Enable Time		TBD	TBD	TBD	µs	
VIH1RC	Input logic level High		TBD	TBD	TBD	V	
VIL1RC	Input logic level Low		TBD	TBD	TBD	V	
SU1RC	Startup time	Test load used:	TBD	TBD	TBD	µs	

Clock Conditioning Circuits (CCC)

***Table 2-85* • SmartFusion2 CCC/PLL Specification**

Parameter			Minimum	Typical	Maximum	Units	Notes
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}			1		200	MHz	
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}			20		400	MHz	
Delay Increments in Programmable Delay Blocks				100		ps	
Number of Programmable Values in Each Programmable Delay Block					64		
Acquisition Time					500	µs	
Tracking Jitter				TBD		ns	
Output Duty Cycle			48		52	%	
Feedback Delay					8	ns	
CCC Output Peak-to-Peak Period Jitter FCCC_OUT	Maximum peak-to-peak period Jitter						
	SSO = 0	0 < SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16		
	FG896	FG896	FG896	FG896	FG896		
20 MHz to 100 MHz	1	TBD	TBD	TBD	TBD	% f_{OUT_CCC}	
100 MHz to 200 MHz	1	TBD	TBD	TBD	TBD	% f_{OUT_CCC}	
200 MHz to 400 MHz	1	TBD	TBD	TBD	TBD	% f_{OUT_CCC}	
Spread Spectrum Characteristics							
Modulation Frequency Range			25	35	50	kHz	
Modulation Depth Range			0		1.5	%	
Modulation Depth Control				0.5		%	

Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to Figure 2-9 on page 2-84.

***Table 2-86* • SPI Characteristics**
Commercial Case Conditions: T_J = 85ºC, VDD = 1.425 V, –1 Speed Grade

Symbol	Description and Condition	M2S050T	Unit
sp1	SPI_x_CLK minimum period		
	SPI_x_CLK = PCLK/2	–	ns
	SPI_x_CLK = PCLK/4	TBD	ns
	SPI_x_CLK = PCLK/8	TBD	ns
	SPI_x_CLK = PCLK/16	TBD	µs
	SPI_x_CLK = PCLK/32	TBD	µs
	SPI_x_CLK = PCLK/64	TBD	µs
	SPI_x_CLK = PCLK/128	TBD	µs
	SPI_x_CLK = PCLK/256	TBD	µs
sp2	SPI_x_CLK minimum pulse width high		
	SPI_x_CLK = PCLK/2	–	ns
	SPI_x_CLK = PCLK/4	TBD	ns
	SPI_x_CLK = PCLK/8	TBD	ns
	SPI_x_CLK = PCLK/16	TBD	µs
	SPI_x_CLK = PCLK/32	TBD	µs
	SPI_x_CLK = PCLK/64	TBD	µs
	SPI_x_CLK = PCLK/128	TBD	µs
	SPI_x_CLK = PCLK/256	TBD	us
sp3	SPI_x_CLK minimum pulse width low		
	SPI_x_CLK = PCLK/2	–	ns
	SPI_x_CLK = PCLK/4	TBD	ns
	SPI_x_CLK = PCLK/8	TBD	ns
	SPI_x_CLK = PCLK/16	TBD	µs
	SPI_x_CLK = PCLK/32	TBD	µs
	SPI_x_CLK = PCLK/64	TBD	µs
	SPI_x_CLK = PCLK/128	TBD	µs
	SPI_x_CLK = PCLK/256	TBD	µs
sp4	SPI_x_CLK, SPI_x_DO, SPI_x_SS rise time (10%-90%)	TBD	ns
sp5	SPI_x_CLK, SPI_x_DO, SPI_x_SS fall time (10%-90%)	TBD	ns
sp6	Data from master (SPI_x_DO) setup time	TBD	pclk cycles
sp7	Data from master (SPI_x_DO) hold time	TBD	pclk cycles
sp8	SPI_x_DI setup time	TBD	pclk cycles
sp9	SPI_x_DI hold time	TBD	pclk cycles

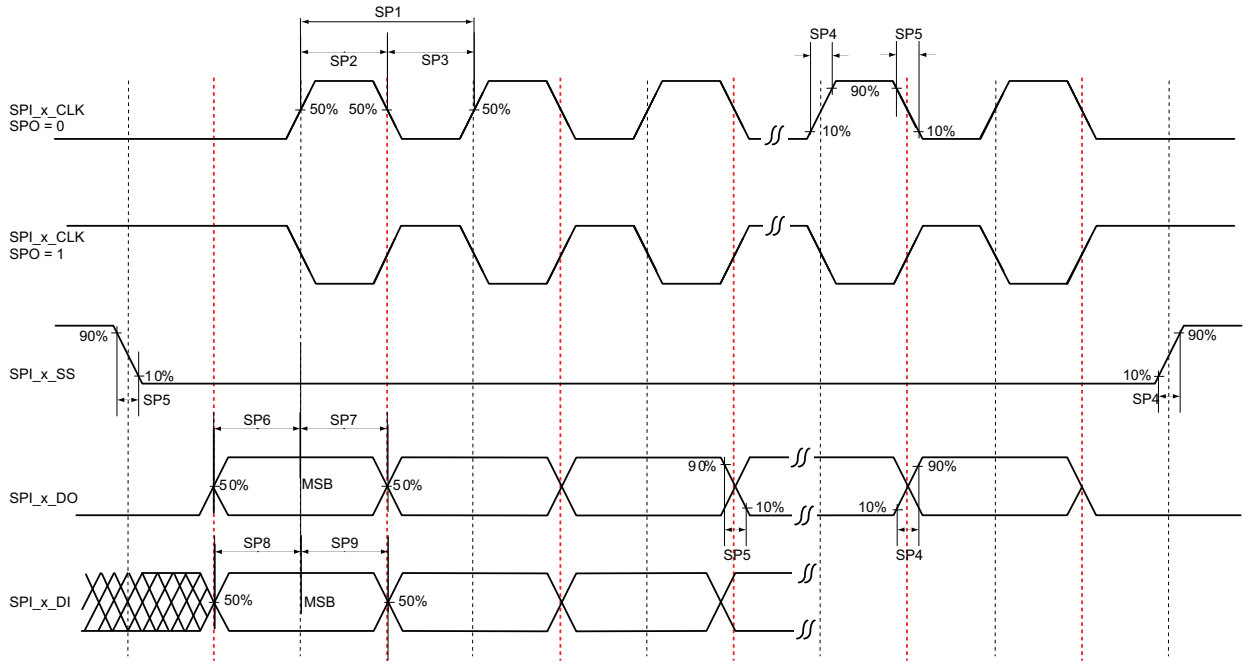


Figure 2-9 • **SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**

Inter-Integrated Circuit (I^2C) Characteristics

This section describes the DC and switching of the I^2C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, refer to Figure 2-10 on page 2-86.

Table 2-87 • **I^2C Characteristics**
Commercial Case Conditions: T_J = 85ºC, VDD = 1.14 V, –1 Speed Grade

Parameter	Definition	Condition	Value	Unit
VIL	Minimum input low voltage	–	See Table 2-18 on page 2-22	–
	Maximum input low voltage	–	See Table 2-18	–
VIH	Minimum input high voltage	–	See Table 2-18	–
	Maximum input high voltage	–	See Table 2-18	–
VOL	Maximum output voltage low	IOL = TBD	See Table 2-18	–
IIL	Input current high	–	See Table 2-18	–
IIH	Input current low	–	See Table 2-18	–
Vhyst	Hysteresis of Schmitt trigger inputs	–	See Table 2-17 on page 2-21	V
T_{FALL}	Fall time	VIHmin to VILMax, Cload = 400 pF	TBD	ns
		VIHmin to VILMax, Cload = 100 pF	TBD	ns
T_{RISE}	Rise time	VILMax to VIHmin, Cload = 400 pF	TBD	ns
		VILMax to VIHmin, Cload = 100 pF	TBD	ns
Cin	Pin capacitance	VIN = 0, f = 1.0 MHz	TBD	pF
$R_{pull-up}$	Output buffer maximum pull-down Resistance	–	TBD	Ω
$R_{pull-down}$	Output buffer maximum pull-up Resistance	–	TBD	Ω
D_{max}	Maximum data rate	Fast mode	TBD	Kbps
t_{LOW}	Low period of I2C_x_SCL	–	TBD	pclk cycles
t_{HIGH}	High period of I2C_x_SCL	–	TBD	pclk cycles
$t_{HD;STA}$	START hold time	–	TBD	pclk cycles
$t_{SU;STA}$	START setup time	–	TBD	pclk cycles
$t_{HD;DAT}$	DATA hold time	–	TBD	pclk cycles
$t_{SU;DAT}$	DATA setup time	–	TBD	pclk cycles
$t_{SU;STO}$	STOP setup time	–	TBD	pclk cycles
t_{FILT}	Maximum spike width filtered	–	TBD	ns

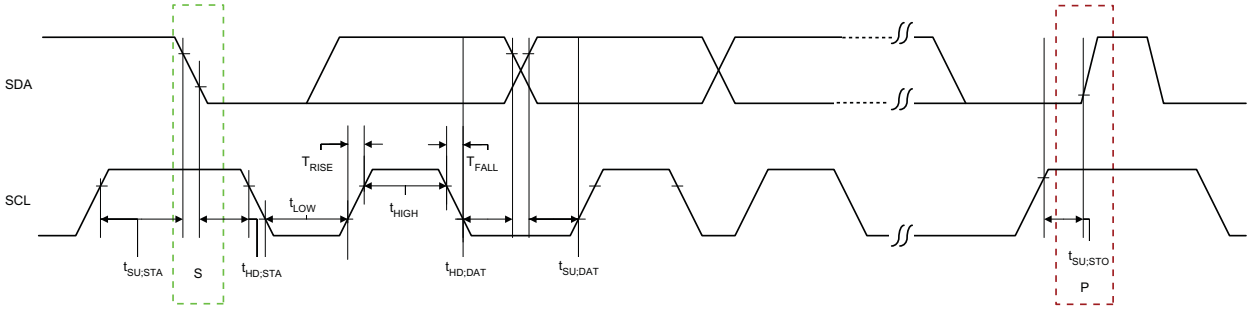


Figure 2-10 • **I2C Timing Parameter Definition**

3 – SmartFusion2 Development Tools

System designers can leverage the newly released, easy-to-use Libero® system-on-chip (SoC) software toolset for designing SmartFusion2 devices. Libero SoC highlights include the following:

- System Builder for creation of system level architecture
- Synthesis, debug and DSP support from Synopsys
- Simulation from Mentor Graphics
- Push-button design flow with power analysis and timing analysis
- SmartDebug for access to non-invasive probes within SmartFusion2 devices
- Integrated firmware flows for GNU, IAR, and Keil
- Operating system support includes uClinux from Emcraft Systems, FreeRTOS,™ SAFERTOS,® and uc/OS-III™ from Micrium.

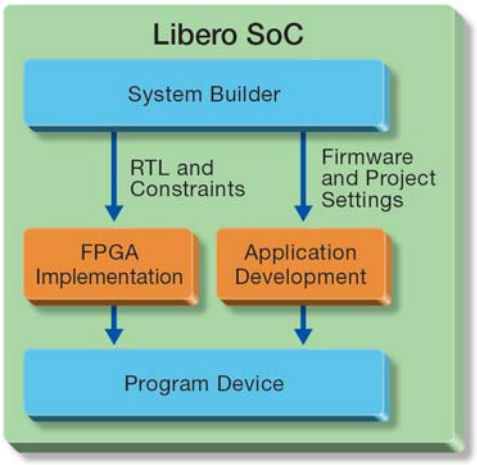


Figure 3-1 • **Tool Flow**

Libero SoC

Libero SoC and Libero Integrated Design Environment (IDE) are comprehensive software toolsets for designing with Microsemi FPGAs. Different versions of Libero support different families.

- Libero SoC v11.0 Beta software release supports only the recently announced SmartFusion2 SoC FPGAs. This version includes a new System Builder design approach, specifically targeted for SmartFusion2 devices. A production version of this software will be available in April 2013, when it will integrate support for the other production flash families currently supported by Libero v10.1.
- Libero SoC v10.1 software release for designing with Microsemi's SmartFusion, IGLOO,® ProASIC®3, and Fusion® families, managing the entire design flow from design entry, synthesis and simulation, through place-and-route, timing and power analysis, with enhanced integration of the embedded design flow.
- Libero IDE software release for designing with Microsemi antifuse and legacy flash FPGAs and managing the entire design flow from design entry, synthesis and simulation, through place-and-route, timing and power analysis (refer to *PCN 1108*).

Libero SoC introduces a new SoC design flow, specifically targeted to simplify the design of our newest flash FPGAs. Standalone tools such as Silicon Sculptor, FlashPro, Identify ME, and Synphony Model Compiler ME are not changing and will continue to include support for all silicon devices.

Current licenses are valid for both SoC and IDE releases; a new license is not required for Libero SoC.

From design, synthesis and simulation, through floorplanning, place-and-route, timing constraints and analysis, power analysis, and program file generation, Libero manages the entire design flow quickly and efficiently. SmartDesign provides an efficient methodology for creating complete simple and complex embedded processor-based system-on-chip (SoC) designs with ease.

The SoC design flow provides the designer the choice of using the powerful microprocessor subsystem (MSS) standalone or creating a more complex system by utilizing available programmable gates in the FPGA fabric. Libero enables the designer to configure the hardwired Cortex-M3 processor, analog (SmartFusion only), and peripherals within MSS, plus extend additional logic functionality into the FPGA fabric, thus taking full advantage of the specific SoC FPGA device resources.

Libero provides full power optimization and analysis tools for Microsemi's low-power flash FPGA families.

Libero Software Features

Libero software offers the latest and best-in-class FPGA development tools from leading EDA vendors such as Mentor Graphics and Synopsys. These tools, combined with tools developed by Microsemi, allow you to quickly and easily manage your Microsemi FPGA designs. An intuitive user interface and powerful design manager guide you through the process while organizing design files and seamlessly managing exchanges between the various tools.

- Powerful project and design flow management
- Full suite of integrated design entry tools and methodologies:
  - SmartDesign graphical SoC design creation with automatic abstraction to HDL
  - Core Catalog and configuration
  - Fabric utilization for SmartFusion2 designs
  - HDL and HDL templates
  - User-defined block creation flow for design re-use
  - Microsemi cell libraries
- Synplify Pro® ME synthesis fully optimizes Microsemi FPGA device performance and area utilization
- Synphony Model Compiler ME performs high-level synthesis optimizations within a Simulink® environment
- ModelSim® ME VHDL or Verilog behavioral, post-synthesis and post-layout simulation capability
- Designer physical design implementation, floorplanning, physical constraints, and layout
- Timing-driven and power-driven place-and-route
- SmartTime environment for timing constraint management and analysis
- SmartPower provides comprehensive power analysis for actual and "what if" power scenarios
- Interface to FlashPro programmers
- Post-route probe insertion and Identify® AE debugging software for Microsemi flash designs
- Supported on Microsoft® Windows® and RedHat Linux operating systems

System Builder

System builder (Figure 3-2 on page 3-3) is a new graphical design wizard designed specifically for SmartFusion2 based designs. System builder walks the user through the following steps:

- Asks the user basic questions on system architecture
- Adds any additional peripherals in the fabric
- Walks through configuration options for each selected feature
- Builds complete base system and API – correct by design

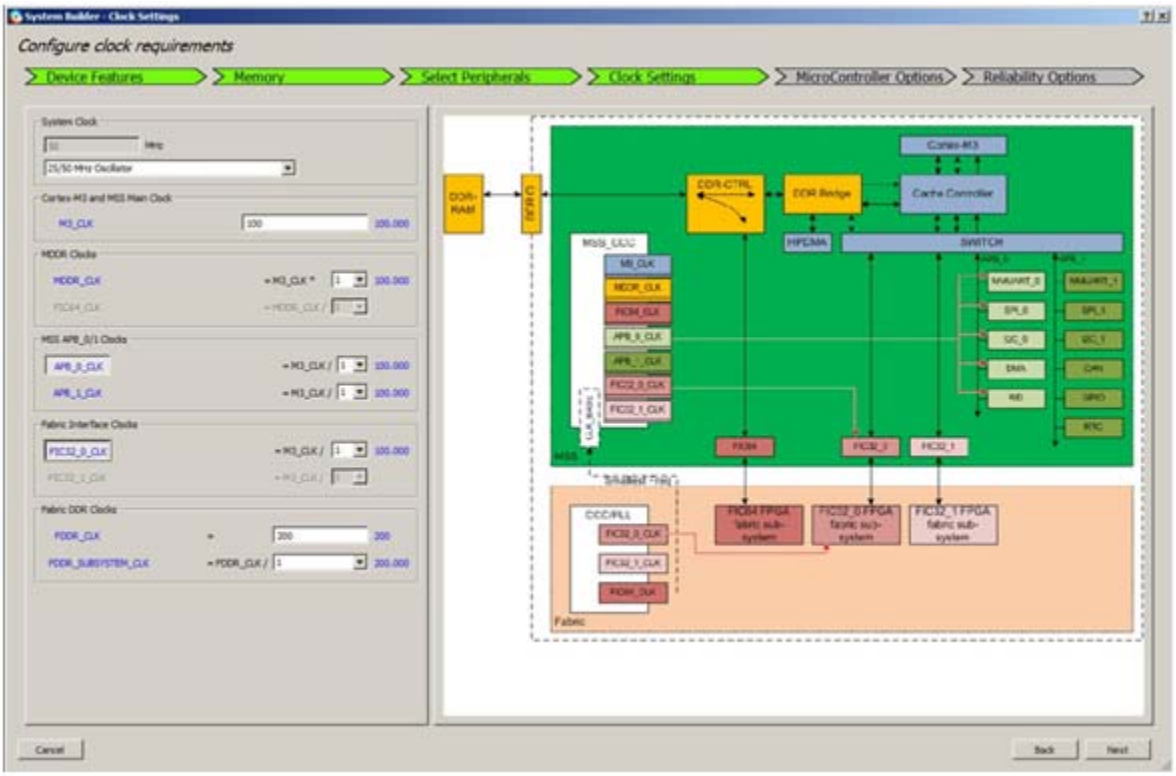


Figure 3-2 • **System Builder**

SmartDebug

SmartDebug is a new debug tool added in Libero SoC v11.0 software that supports probe capabilities in the SmartFusion2 architecture and also supports device debug features for memory. SmartFusion2 devices have built-in probe points that greatly enhance the ability to debug logic elements within the device. The enhanced debug features implemented in SmartFusion2 devices give access to any logic element and enable designers to check the state of inputs and outputs in real time. Live Probe and Active Probe are only available on the SmartFusion2 family of products.

- With Live Probe, two dedicated probes can be configured to observe a Probe Point which is any input or output of a logic element. The probe data can then be sent to an oscilloscope or even redirected back to the FPGA fabric to drive a software logic analyzer.
- Active Probe allows dynamic asynchronous read and write to a flip-flop or probe point. This enables a user to quickly observe the output of the logic internally or to quickly experiment on how the logic will be affected by writing to a probe point.
- Memory debug gives the ability to perform dynamic asynchronous reads and writes to a micro SRAM or large SRAM block so the user can quickly verify if the content of the memory is changing as expected.

SmartDebug features can be accessed from within the Libero design flow or FlashPro software.

SoftConsole

Microsemi's Embedded Software Development Environment

SoftConsole is Microsemi's free software development environment that enables the rapid production of C and C++ executables for Microsemi FPGAs using Cortex-M3, Cortex-M1, and Core8051s. Libero SoC automatically generates SoftConsole projects and firmware for SoC FPGA designs. SoftConsole includes a fully integrated debugger that offers easy access to memory contents, registers, and single-instruction execution.

Product Features

SoftConsole (Figure 3-3 on page 3-5) provides a flexible and easy-to-use graphical user interface for managing your embedded software development projects. You can quickly develop and debug software programs and implement them in Microsemi FPGAs. SoftConsole enables you to configure project settings, edit and debug software programs, and organize your files. With this tool you have simultaneous access to multiple tool windows and the ability to quickly switch editing and debug views.

- Available for free download
- Eclipse-based IDE
- GNU C/C++ compiler (Cortex-M3 and Cortex-M1)
- SDCC compiler (Core8051s)
- GDB debugger
- FlashPro4/3/3X compatible debug sprite
- Seamless access to and debug of flash memory (SmartFusion2 eNVM, Fusion NVM, external flash)
- Simultaneous access to multiple tool windows
- Fast switch between C/C++ and debug
- One or more perspectives in a workbench window
- Perspectives can be customized by the user
- Provides a direct interface to:
  - SmartFusion2 microcontroller subsystem (MSS) for SmartFusion2 designs
  - Firmware Catalog, which includes CMSIS-PAL for Cortex-M3, HALs for Cortex-M1 and 8051s, driver firmware packages, sample programs, and linker scripts
- Compatible with Libero SoC and IDE design flows

SoftConsole User Interface

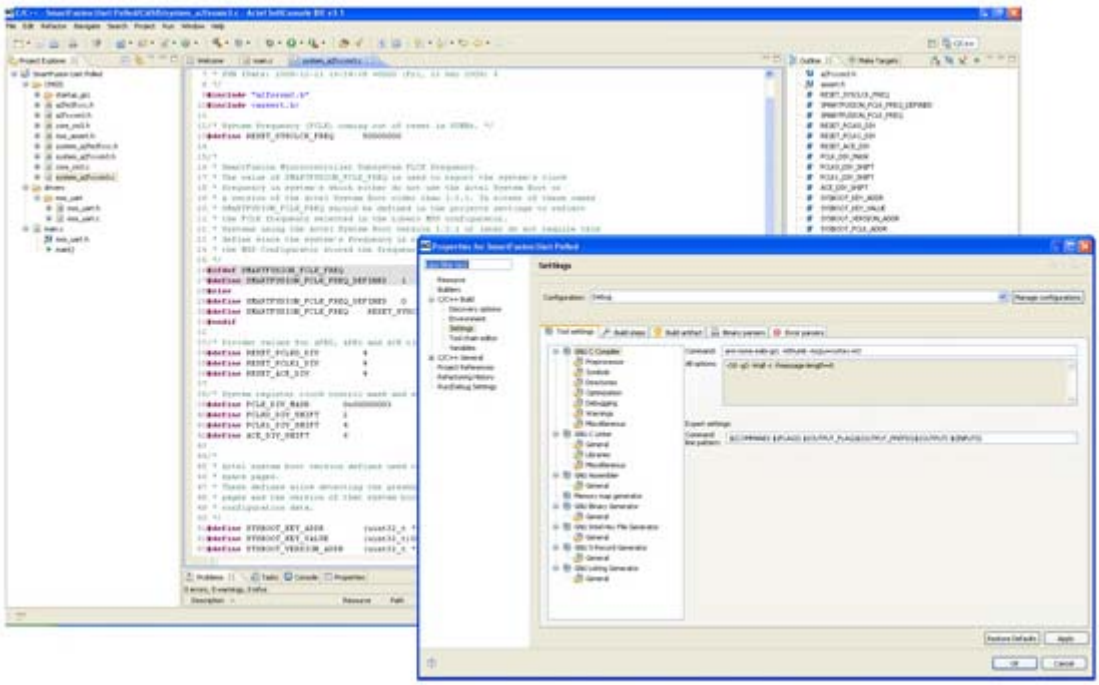


Figure 3-3 • **SoftConsole User Interface**

Firmware Catalog

The Firmware Catalog is a standalone executable program that supports Microsemi SoftConsole, Keil™, and IAR Systems® embedded processor development toolchains targeting the ARM Cortex-M3, Cortex-M1, and Core8051s processors. The Firmware Catalog streamlines locating and generating firmware that is compatible with Intellectual Property (IP) cores used in Microsemi FPGA designs. Firmware can also be delivered through SmartDesign within the Libero environment.

Software Drivers

Microsemi has a broad offering of proven and pre-implemented synthesizable IP building blocks that can be easily configured and used within Microsemi FPGA system-level designs. Software drivers for many Microsemi IP cores are available within the Firmware Catalog. The drivers are free of charge and delivered as C source, so they can be easily compiled and linked into a user's program or executable. These drivers hide the implementation details of peripheral operations behind a driver application program interface (API), so the developer need only be concerned with the peripheral's function.

Hardware Abstraction Layers

A hardware abstraction layer (HAL) that supports ARM Cortex-M3, Cortex-M1 and Core8051s processors is also available. HALs enable the software driver to be used without modification, isolating the driver's implementation from the hardware platform variations. A driver implementation interacts with the hardware peripheral it is controlling. This enables programmers to seamlessly reuse code, even when the hardware platform changes.

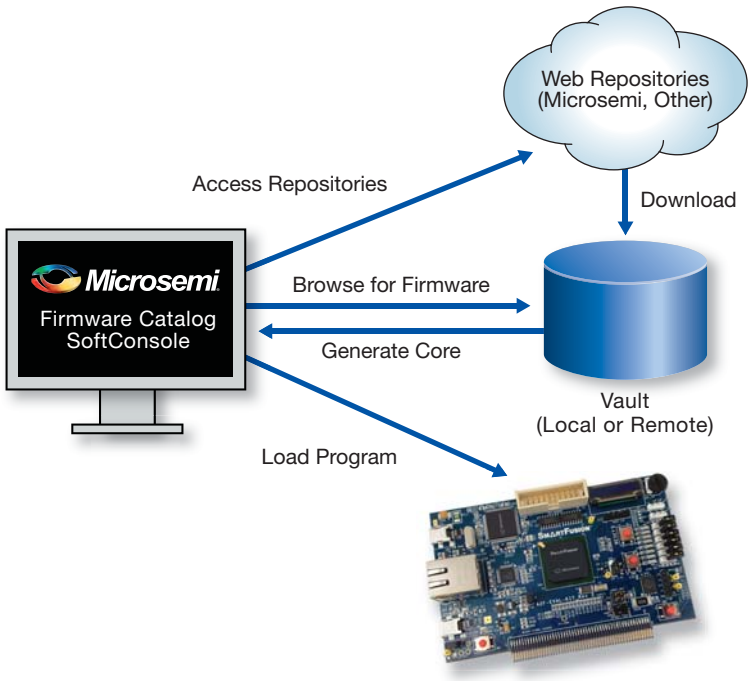


Figure 3-4 • **Hardware Abstraction Layer**

The Firmware Catalog notifies the user if new firmware cores or firmware updates are available from Microsemi's web repository. The updates can be downloaded into a local vault on a PC. A vault is a local directory (either local to a machine or on the local network) that contains cores downloaded from one or more repositories. The repository is a location on the web that contains firmware cores ready to be used directly in any toolchain software.

After selecting IPs to use in the Microsemi FPGA design, the associated firmware can be selected in the Firmware Catalog and the IP cores can be generated. The IP cores are then loaded into the code via SoftConsole, Keil, or IAR Systems software development environments.

For the SoC design flow, the designer does not need to determine which firmware must be selected and generated. Although the designer can browse the complete listing of firmware in the Firmware Catalog, the SmartDesign flow for SmartFusion2 and SmartFusion searches the design for instantiated IP and automatically presents the appropriate firmware.

Firmware Catalog User Interface

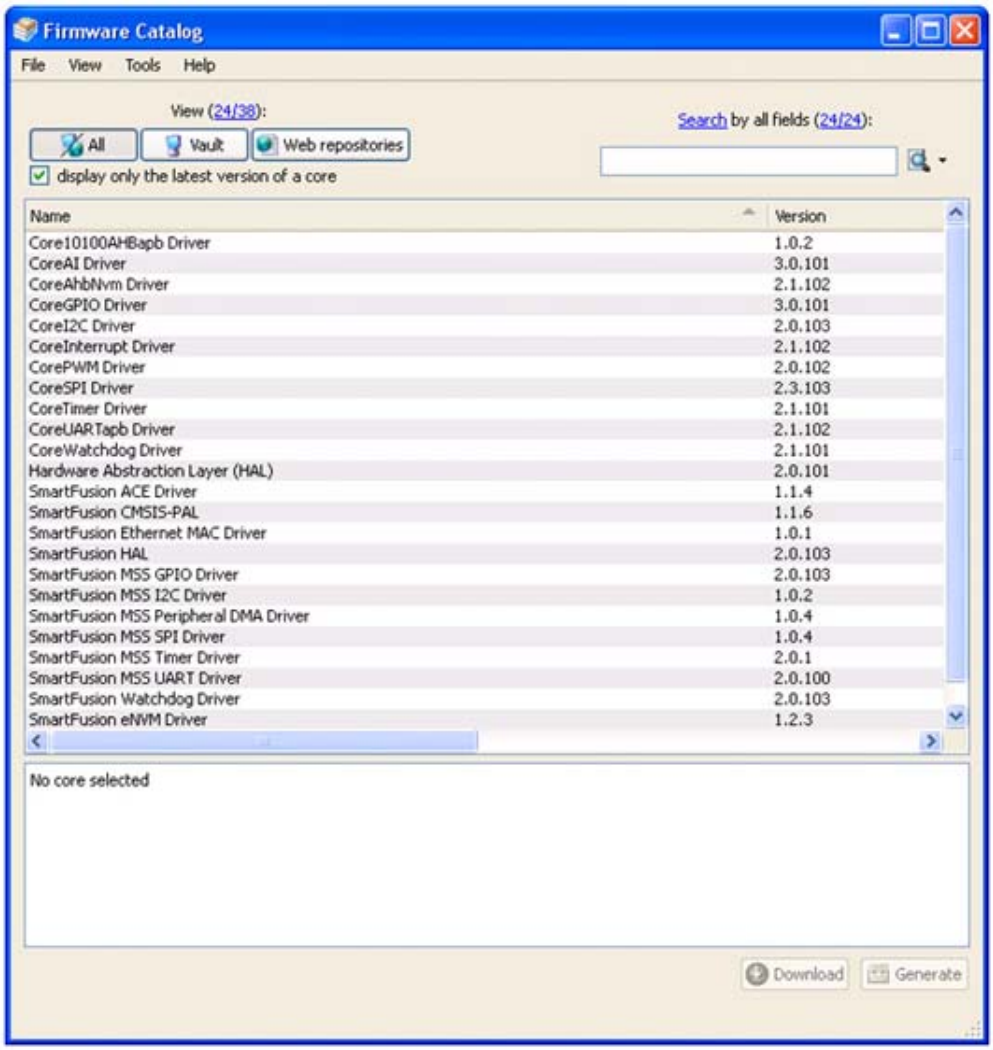


Figure 3-5 • **Firmware Catalog User Interface**

The Firmware Catalog is configured within SoftConsole so that it is integrated in the toolchain, which allows seamless location, configuration, and addition of firmware to the user's SoftConsole project.

SoC FPGA Ecosystem

Microsemi has a long history of supplying comprehensive FPGA development tools and recognizes the benefit of partnering with industry leaders to deliver the optimum usability and productivity to customers. Taking the same approach with processor development, Microsemi has partnered with key industry leaders in the microcontroller space to provide the robust SoC FPGA ecosystem.

Microsemi is partnering with Keil and IAR to provide Software IDE support to system designers. The result is a robust solution that can be easily adopted by developers who are already doing embedded design. The learning path is straightforward for FPGA designers.

Figure 3-6 shows a software stack with examples of drivers, RTOS and middleware from Microsemi and partners. By leveraging the software stack, designers can decide at which level to add their own customization to their design, thus speeding time to market and reducing overhead in the design.

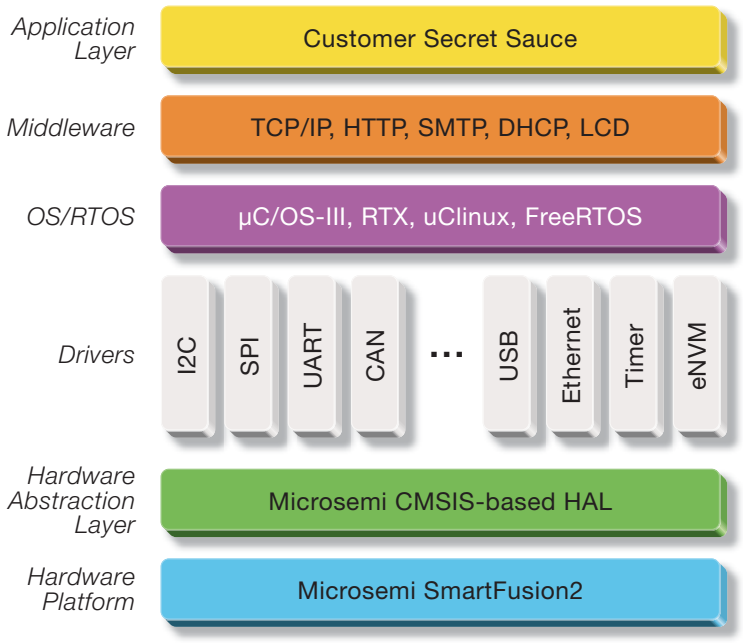


Figure 3-6 • **Software Stack**

ARM

Because an ARM processor was chosen for SmartFusion2 and SmartFusion devices, Microsemi's customers can benefit from the extensive ARM ecosystem. By building on Microsemi supplied hardware abstraction layer (HAL) and drivers, third party vendors can easily port RTOS and middleware for the SmartFusion devices.

- ARM Cortex-M Series Processors
- ARM Cortex-M3 Processor Resources
- ARM Cortex-M3 Technical Reference Manual
- *ARM Cortex-M3 Processor Software Development for ARM7TDMI Processor Programmers White Paper*

Compile and Debug

			
Software IDE	**SoftConsole**	**Keil MDK**	**IAR Embedded Workbench®**
Website	www.microsemi.com/soc	www.keil.com	www.iar.com
Free versions from SoC Products Group	Free with Libero SoC	32 K code limited	32 K code limited
Available from Vendor	N/A	Full version	Full version
Compiler	GNU GCC	RealView C/C++	IAR ARM Compiler
Debugger	GDB debug	Vision Debugger	C-SPY® Debugger
Instruction Set Simulator	No	Vision Simulator	Yes
Debug Hardware	FlashPro4	ULINK2® or ULINK-ME	J-LINK™ or J-LINK Lite

Microsemi's SoftConsole is a free Eclipse-based IDE that enables the rapid production of C and C++ executables for Microsemi FPGAs and cSoCs using Cortex-M3, Cortex-M1, and Core8051s. For SmartFusion support, SoftConsole includes the GNU C/C++ compiler and GDB debugger. Additional examples can be found on the SoftConsole page.

Using UART with SmartFusion cSoC: SoftConsole Standalone Flow Tutorial

Displaying POT Level with LEDs: Libero SoC and SoftConsole Flow Tutorial for a SmartFusion cSoC

IAR Embedded Workbench® for ARM/Cortex is an integrated development environment for building and debugging embedded ARM applications using assembler, C and C++. It includes a project manager, editor, build and debugger tools with support for RTOS-aware debugging on hardware or in a simulator.

- *Designing SmartFusion with IAR Systems*
- *IAR Embedded Workbench for ARM*

Keil's Microcontroller Development Kit comes in two editions: MDK-ARM and MDK Basic. Both editions feature µVision®, the ARM Compiler, MicroLib, and RTX, but the MDK Basic edition is limited to 256K so that small applications are more affordable.

- *Designing SmartFusion with Keil*
- *Using Keil µVision and Microsemi SmartFusion*
- Keil Microcontroller Development Kit for ARM Product Manuals
- Download Evaluation version of Keil MDK-ARM

Operating Systems

FreeRTOS™ is a portable, open source, royalty free, mini real-time kernel (a free-to-download and free-to-deploy RTOS that can be used in commercial applications without any requirement to expose your proprietary source code). FreeRTOS is scalable and designed specifically for small embedded systems. This FreeRTOS version ported by Microsemi is 6.0.1. For more information, visit the FreeRTOS website: www.freertos.org

- *SmartFusion Webserver Demo Using uIP and FreeRTOS*
- *SmartFusion: Running Webserver, TFTP on lwIP TCP/IP Stack Application Note*

Emcraft Systems provides porting of the open-source U-boot firmware and uClinux™ kernel to SmartFusion, a Linux-based cross-development framework, and other complementary components. Combined with the release of its *A2F-Linux Evaluation Kit*, this provides a low-cost platform for evaluation and development of Linux (uClinux) on the Cortex-M3 CPU core of Microsemi SmartFusion2 devices.

- Emcraft Linux on Microsemi's SmartFusion

Keil offers the RTX Real-Time Kernel as a royalty-free, deterministic RTOS designed for ARM and Cortex-M devices. It allows you to create programs that simultaneously perform multiple functions and helps to create applications which are better structured and more easily maintained.

- The RTX Real-Time Kernel is included with MDK-ARM. Download the Evaluation version of Keil MDK-AR.
- RTX source code is available as part of Keil/ARM Real-Time Library (RL-ARM), a group of tightly-coupled libraries designed to solve the real-time and communication challenges of embedded systems based on ARM-powered microcontroller devices. The RL-ARM library now supports SmartFusion devices and designers with additional key features listed in the "Middleware" section on page 3-11.

Micrium supports SmartFusion with the company's flagship µC/OS family, recognized for a variety of features and benefits, including unparalleled reliability, performance, dependability, impeccable source code and vast documentation. Micrium supports the following products for SmartFusion devices and continues to work with Microsemi on additional projects.

- µC/OS-III, Micrium's newest RTOS, is designed to save time on your next embedded project and puts greater control of the software in your hands.
- *SmartFusion Quickstart Guide for Micrium µC/OS-III Examples*

RoweBots provides an ultra tiny Linux-compatible RTOS called Unison for SmartFusion. Unison consists of a set of modular software components, which, like Linux, are either free or commercially licensed. Unison offers POSIX® and Linux compatibility with hard real-time performance, complete I/O modules and an easily understood environment for device driver programming. Seamless integration with FPGA and analog features are fast and easy.

- Unison V4-based products include a free Unison V4 Linux and POSIX-compatible kernel with serial I/O, file system, six demonstration programs, upgraded documentation and source code for Unison V4, and free (for non-commercial use) Unison V4 TCP/IP server. Commercial license upgrade is available for Unison V4 TCP/IP server with three demonstration programs, DHCP client and source code.
- Unison V5-based products include commercial Unison V5 Linux- and POSIX-compatible kernel with serial I/O, file system, extensive feature set, full documentation, source code and more than 20 demonstration programs, Unison V5 TCP/IPv4 with extended feature set, sockets interface, multiple network interfaces, PPP support, DHCP client, documentation, source code and six demonstration programs, and multiple other features.

Middleware

Microsemi has ported both uIP and lwIP for Ethernet support as well as including TFTP file service.

- *SmartFusion Webserver Demo Using uIP and FreeRTOS*
- *SmartFusion: Running Webserver, TFTP on lwIP TCP/IP Stack Application Note*

The Keil/ARM Real-Time Library (RL-ARM)* in addition to RTX source includes:

- RL-TCPnet (TCP/IP) – The Keil RL-TCPnet library, supporting full TCP/IP and UDP protocols, is a full networking suite specifically written for small ARM and Cortex-M processor-based microcontrollers. TCPnet is now ported to and supports SmartFusion Cortex-M3. It is highly optimized, has a small code footprint, and gives excellent performance, providing a wide range of application level protocols and examples such as FTP, SNMP, SOAP, and AJAX. An HTTP server example of TCPnet working in a SmartFusion design is available.
- The Flash File System (RL-Flash) allows your embedded applications to create, save, read, and modify files in standard storage devices such as ROM, RAM, or FlashROM, using a standard serial peripheral interface (SPI). Many ARM-based microcontrollers have a practical requirement for a standard file system. With RL-FlashFS you can implement new features in embedded applications such as data logging, storing program state during standby modes, or storing firmware upgrades.

*Note: * The CAN and USB functions within RL-ARM are not supported for SmartFusion.*

Micrium in addition to their µC/OS-III offers the following support for SmartFusion:

- µC/TCP-IP™ is a compact, reliable and high-performance stack built from the ground up by Micrium and has the quality, scalability and reliability that translates into a rapid configuration of network options, remarkable ease-of-use and rapid time-to-market.
- µC/Probe™ is one of the most useful tools in embedded systems design and puts you in the driver's seat, allowing you to take charge of virtually any variable, memory location, and I/O port in your embedded product, while your system is running.

SmartFusion2 Development Kit

The SmartFusion2 Development Kit allows access to the peripherals of the SmartFusion2 SoC FPGA. This board is designed to support full application development and prototyping. The kit will also serve as a motherboard for several application-specific daughtercards that will be rolled over the next year.

- Motor control interface card supports up to 6 motor daughtercards
- System Management daughtercard
- Aviation daughtercard

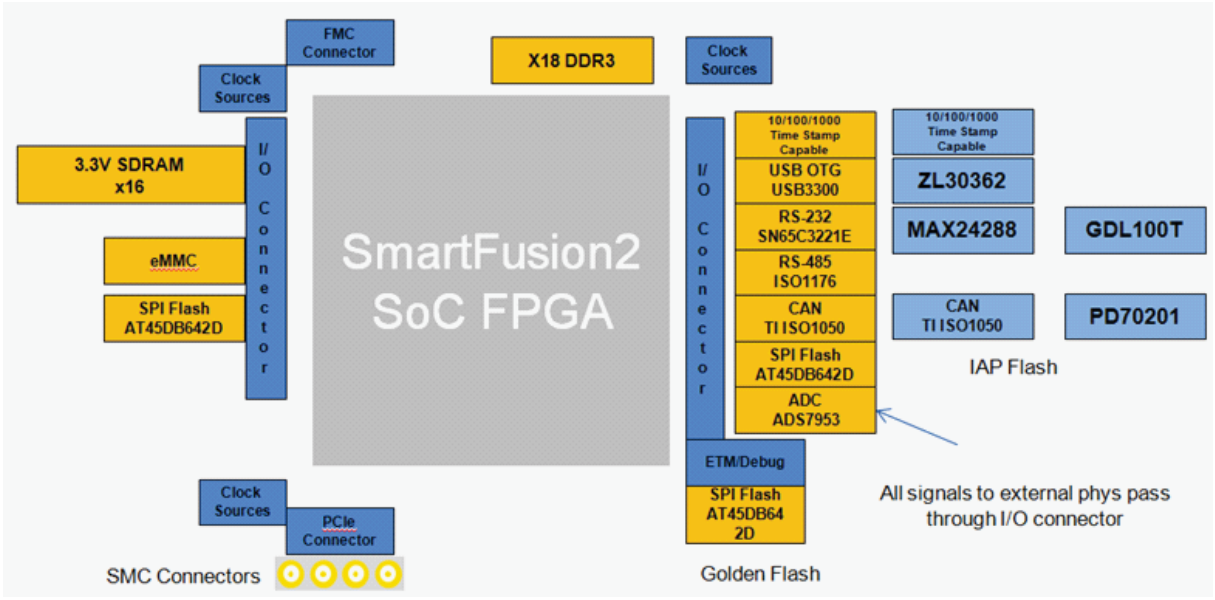


Figure 3-7 • **SmartFusion2 Development Kit**

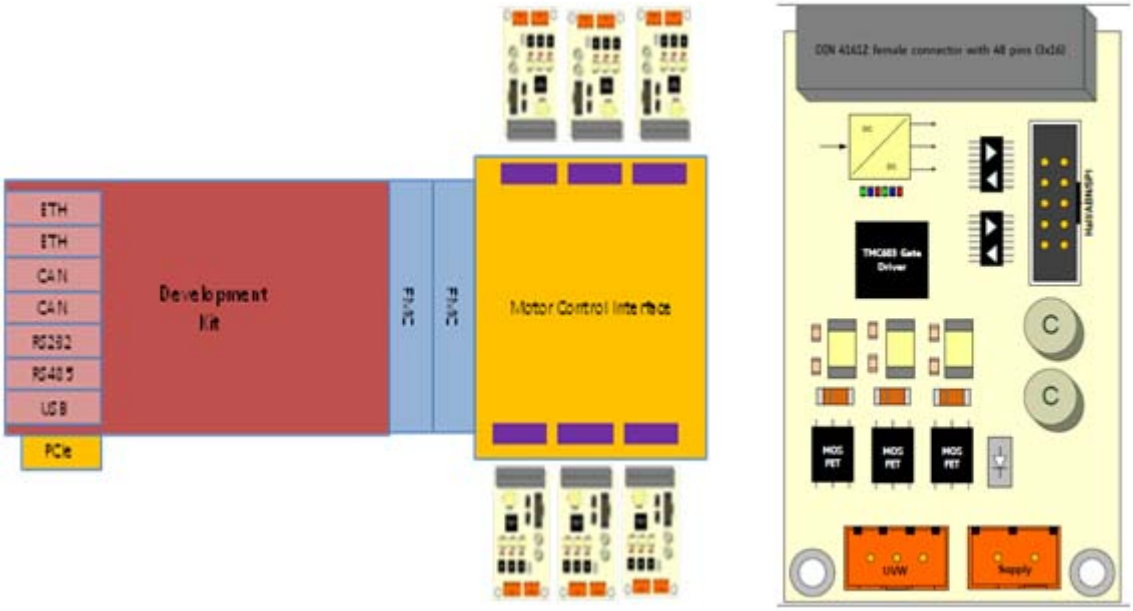


Figure 3-8 • **SmartFusion2 Applications**

4 – Pin Descriptions

SmartFusion2 devices support multi-standard I/Os (MSIO), microcontroller serial interfaces, high speed serial interfaces, and a debugging JTAG interface. SmartFusion2 devices require all the power supplies listed in Table 4-1.

Supply Pins

Table 4-1 • **Supply Pins**

Name	Type	Description	Min. (V)	Max. (V)
VSS	Ground	Ground pad for core and I/Os		
PLL0_VSSA	Ground	VDDA to on-die VSSA high pass filter connection for PLL0. If unused, it must be grounded.		
PLL0_VDDA	Supply	Analog power pad for PLL0	2.5	3.3
PLL1_VSSA	Ground	VDDA to on-die VSSA high pass filter connection for PLL1. If unused, it must be grounded.		
PLL1_VDDA	Supply	Analog power pad for PLL1	2.5	3.3
PLL2_VSSA	Ground	VDDA to on-die VSSA high pass filter connection for PLL2. If unused, it must be grounded.		
PLL2_VDDA	Supply	Analog power pad for PLL2	2.5	3.3
PLL3_VSSA	Ground	VDDA to on-die VSSA high pass filter connection for PLL3. If unused, it must be grounded.		
PLL3_VDDA	Supply	Analog power pad for PLL3	2.5	3.3
PLL4_VSSA	Ground	VDDA to on-die VSSA high pass filter connection for PLL4. If unused, it must be grounded.		
PLL4_VDDA	Supply	Analog power pad for PLL4	2.5	3.3
PLL5_VSSA	Ground	VDDA to on-die VSSA high pass filter connection for PLL5. If unused, it must be grounded.		
PLL5_VDDA	Supply	Analog power pad for PLL5	2.5	3.3
PLL_PCIE_0_VSSA	Ground	VDDA to on-die VSSA high pass filter connection for PLL PCIe0. If unused, it must be grounded.		
PLL_PCIE_0_VDDA	Supply	High supply voltage for PLL PCIe0. If unused, should be connected to +3.3 V.	2.5	3.3
PLL_PCIE_1_VSSA	Ground	VDDA to on-die VSSA high pass filter connection for PLL PCIe1. If unused, it must be grounded		
PLL_PCIE_1_VDDA	Supply	High supply voltage for PLL PCIe1. If unused, should be connected to +3.3 V.	2.5	3.3

Notes:

1. *PCIe0 for SERDESIF_0 and PCIe1 for SERDESIF_1*
2. *VREF is not used in differential mode.*
3. *The M2S050T device has two SERDESIFs (SERDESIF_0, SERDESIF_1), which reside on 2 I/O banks (bank 6 and bank 9) out of a total of 10 I/O banks.*

Table 4-1 • **Supply Pins (continued)**

Name	Type	Description	Min. (V)	Max. (V)
PCIE0VDD	Supply	PCIe/PCS supply. If unused, should be connected to +1.2 V.	1	1.2
PCIE0VDDIOL[1]	Supply	Tx/Rx analog I/O voltage. Low voltage power for PCIe0 for lane0 and lane1 of SERDESIF_0, located on the left side. If unused, should be connected to +1.2 V.	1.2	1.2
PCIE0VDDIOR[1]	Supply	Tx/Rx analog I/O voltage. Low voltage power for PCIe0 for lane2 and lane3 of SERDESIF_0, located on the right side. If unused, should be connected to +1.2 V.	1.2	1.2
PCIE0PLLREFRETL[1]		Local on-chip ground return path for PCIE0VDDPLLL for lane0 and lane1 of SERDESIF_0, located on the left side. **DO NOT short to GND** on the package or PCB. For details, refer to the "High speed board design guidelines"-SERDES I/Os section. If unused, it can be left floating.		
PCIE0VDDPLLL[1]	Supply	Analog power for SERDES PLL of PCIe0 lanes 0&1. If unused, should be connected to +2.5 V	2.5	2.5
PCIE0PLLREFRETR[1]		Local on-chip ground return path for PCIE0VDDPLLR for lanes 2 and 3 of SERDESIF_0 that is located on right side. *DO NOT short to GND* on the package or PCB. If unused, it can be left floating.		
PCIE0VDDPLLR[1]	Supply	Analog power for SERDES PLL of PCIe0 lane2 and lane3. If unused, should be connected to +2.5 V.	2.5	2.5
PCIE1VDD	Supply	PCIe/PCS supply. If unused, should be connected to +1.2 V.	1	1.2
PCIE1VDDIOL[1]	Supply	Tx/Rx analog I/O voltage. Low voltage power for PCIe1 for lane0 and lane1 of SERDESIF_1, located on the left side. If unused, should be connected to+1.2 V.	1.2	1.2
PCIE1VDDIOR[1]	Supply	Tx/Rx analog I/O voltage. Low voltage power for PCIe1 for lane2 and lane3 of SERDESIF_1, located on the right side. If unused, should be connected to +1.2 V.	1.2	1.2
PCIE1PLLREFRETL[1]		Local on-chip ground return path for PCIE1VDDPLLL for lane0 and lane1 of SERDESIF_1, located on left side. **DO NOT short to GND** on the package or PCB. If unused, it can be left floating.		
PCIE1VDDPLLL[1]	Supply	Analog power for SERDES PLL of PCIe1 lane0 and lane1. If unused, connect to +2.5 V.	2.5	2.5

Notes:

1. *PCIe0 for SERDESIF_0 and PCIe1 for SERDESIF_1*
2. *VREF is not used in differential mode.*
3. *The M2S050T device has two SERDESIFs (SERDESIF_0, SERDESIF_1), which reside on 2 I/O banks (bank 6 and bank 9) out of a total of 10 I/O banks.*

Table 4-1 • **Supply Pins (continued)**

Name	Type	Description	Min. (V)	Max. (V)
PCIE1PLLREFRETR[1]		Local on-chip ground return path for PCIE1VDDPLLR for lane2 and lane3 of SERDESIF_1, located on right side. **DO NOT short to GND** on the package or PCB. If unused, it can be left floating.		
PCIE1VDDPLLR[1]	Supply	Analog power for SERDES PLL of PCIe1 lane2 and lane3. If unused, should be connected to +2.5 V.	2.5	2.5
PLL_MDDR_VSSA	Ground	Analog ground pad for PLL MDDR		
PLL_MDDR_VDDA	Supply	Analog power pad for PLL MDDR	2.5	3.3
PLL_FDDR_VSSA	Ground	Analog ground pad for PLL of FDDR		
PLL_FDDR_VDDA	Supply	Analog power pad for PLL of FDDR	2.5	3.3
VREF0[2]	Supply	Reference voltage for FDDR (bank 0)	0.50 * VDDI0	0.50 * VDDI0
VREF5[2]	Supply	Reference voltage for MDDR (bank 5)	0.50 * VDDI5	0.50 * VDDI5
VSSNVM	Ground	eNVM ground		
VPPNVM	Supply	eNVM power pad	2.5	3.3
VDDI0	Supply	VDDI port 0, bank 0 power	1.2	2.5
VDDI1	Supply	VDDI port 1, bank 1 power	1.2	3.3
VDDI2	Supply	VDDI port 2, bank 2 power	1.2	3.3
VDDI3	Supply	VDDI port 3, bank 3 power	1.2	3.3
VDDI4	Supply	VDDI port 4, bank 4 power	1.2	3.3
VDDI5	Supply	VDDI port 5, bank 5 power	1.2	2.5
VDDI6	Supply	VDDI port 6, bank 6 power	1.2	2.5
VDDI7	Supply	VDDI port 7, bank 7 power	1.2	2.5
VDDI8	Supply	VDDI port 8, bank 8 power	1.2	3.3
VDDI9	Supply	VDDI port 9, bank 9 power	1.2	2.5
VDD	Supply	Low voltage supply port	1	1.2
VPP	Supply	Power for charge pumps	2.5	3.3

Notes:

1. *PCIe0 for SERDESIF_0 and PCIe1 for SERDESIF_1*
2. *VREF is not used in differential mode.*
3. *The M2S050T device has two SERDESIFs (SERDESIF_0, SERDESIF_1), which reside on 2 I/O banks (bank 6 and bank 9) out of a total of 10 I/O banks.*

Dedicated Global I/O Naming Conventions

Dedicated global I/Os are dual-use I/Os which can drive the global blocks either directly or through clock conditioning circuits (CCC) or virtual clock conditioning circuits (VCCC). They can also be used as regular I/Os. These global I/Os are the primary source for bringing in the external clock inputs into the SmartFusion2 device. In the M2S050T device, there are 16 global blocks located in the center of the fabric and 32 global I/Os located 8 each on the north, east, south, and west sides of the fabric. There are 6 CCC blocks, located 2 each on northwest, northeast, and southwest side of the fabric and 2 VCCC blocks on the southeast side of the fabric.

Dedicated global I/Os that drive the global blocks (GB) directly are named as **GBn,** where

n is 0 to 15.

Dedicated global I/Os that drive GBs through CCCs are named as **CCC_xyz_lw**, where:

xy is the location—NE, SW, or NW.

z is 0 or 1.

l represents I/O

w refers to one of the four possible output clocks of the associated CCC_xyz—GL0, GL1, GL2, or GL3.

Dedicated global I/Os that drive GBs through VCCCs are named as **VCCC_SEz**, where:

SE is southeast.

z is 0 or 1.

Unused global pins are configured as inputs with pull-up resistors by Libero software.

For further details, refer to the "Fabric Global Routing Resources" chapter of the *SmartFusion2 FPGA Fabric Architecture User's Guide*.

User I/O Naming Conventions

The naming convention used for each FPGA user I/O is IOxyBz, where:

IO is the type of I/O—MSIO, MSIOD, or DDRIO

For the M2S050T device:

MSIO **x** is the I/O pair number in bank **z**, starting at 0 from bank 3 (southeast) and proceeding in a counter-clockwise direction to bank 2 and bank 1.

MSIOD **x** is the I/O pair number in bank z, starting at 93 from bank9 (northwest) and proceeding in a counter-clockwise direction to bank7 and bank6.

DDRIO **x** is the I/O pair number in bank z, starting at 49 from bank0 (north) to bank5 (south).

y is P (positive) or N (negative). In single-ended mode, the I/O pair operates as two separate I/Os named P and N. Differential mode is implemented with a fixed I/O pair and cannot be split with an adjacent I/O.

B is bank.

z is the bank number—0 to 9.

Differential standards are implemented as true differential outputs and complementary single-ended outputs for SSTL/HSTL. In the single-ended mode, the I/O pair operates as two separate I/Os named P and N. All the configuration and data inputs/outputs are then separate and use names ending in P and N to differentiate between the two I/Os.

For more information, refer to the "I/Os" chapter of the *SmartFusion2 FPGA Fabric Architecture User's Guide*.

Multi-Standard I/O

SmartFusion2 devices feature a flexible I/O structure that supports a range of mixed voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V) through bank selection. The MSIO, MSIOD, and DDRIO can be configured as differential I/Os or two single-ended I/Os. These I/Os use one I/O slot to implement single-ended standards and two I/O slots for differential standards. The DDRIO is shared between fabric logic and MDDR/FDDR whereas MSIO/MSIOD is shared between MSS peripherals and fabric logic. When you do not use an MDDR/FDDR controller or MSS peripherals, the respective I/Os are available to fabric logic. For functional block diagrams of MSIO, MSIOD, and DDRIO, refer to the *SmartFusion2 FPGA Fabric Architecture User's Guide*.

For supported I/O standards, refer to the Supported Voltage Standards table in the *SmartFusion2 FPGA Fabric Architecture User's Guide*.

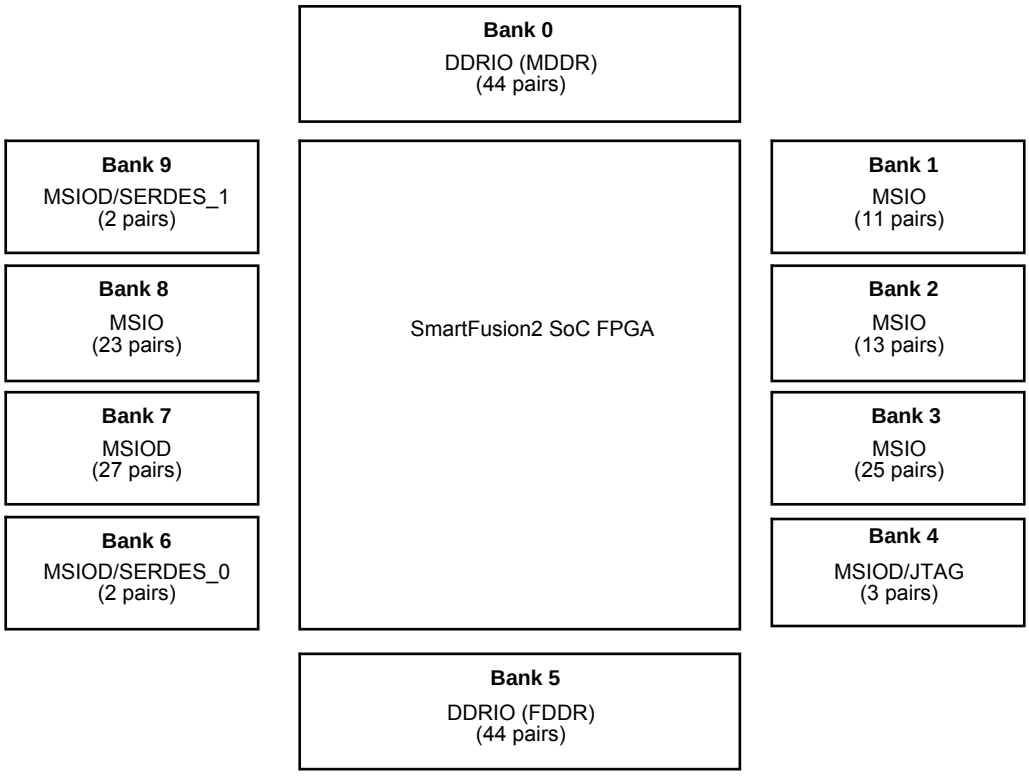


Figure 4-1 • **SmartFusion2 (M2S050T) I/O Bank Location and Naming**

Table 4-2 • **Multi-Standard I/O Types**

Name	Type	Description
MSIOxyBz	In/out	MSIOs provide programmable drive strength, weak pull-up, and weak-pull-down. In single-ended mode, the I/O pair operates as two separate I/Os named P and N. Some of these pins are also multiplexed with integrated peripherals in the MSS (I2C, USB, SPI, UART, CAN, and fabric I/Os).This allows MSIO pins to be multiplexed as I/Os for the FPGA fabric, the ARM Cortex-M3 processor, or for given integrated MSS peripherals. MSIOs can be routed to dedicated I/O buffers (MSSIOBUF) or in some cases to the FPGA fabric interface through an IOMUX. SmartFusion2 I/O ports also support ESD protection.
MSIODxyBz	In/out	MSIOD is very similar to MSIO, but drops 3.3 V and hot-plug support and adds pre-emphasis, in order to achieve higher speeds. MSIODs provide programmable drive strength, weak pull-up, and weak pull-down. MSIOD I/O cells operate at up to 2.5 V and are capable of high-speed LVDS operation. Some of these pins are also multiplexed with the SERDES interface. SmartFusion2 I/O ports support ESD protection.
DDRIOxyBz	In/out	The double data input output (DDRIO) is a multi-standard I/O optimized for LPDDR/DDR2/DDR3 performance. In SmartFusion2 devices there are two DDR subsystems: the fabric DDR and MSS DDR controllers. All DDRIOs can be configured as differential I/Os or two single-ended I/Os. If you select MDDR/FDDR, Libero SoC automatically connects MDDR/FDDR signals to the DDRIOs. DDRIOs can be connected to the respective DDR subsystem PHYs or can be used as user I/Os. Depending on the memory configuration, only the required DDRIOs are used by Libero SoC. The unused DDRIOs are available to connect to the fabric.

I/O Programmable Features

SmartFusion2 devices support different I/O programmable features for MSIO, MSIOD, and DDRIO. Each I/O pair (P, N) supports the following programmable features:

- Programmable drive strength
- Programmable weak pull-up and pull-down
- Configurable ODT and driver impedance
- Programmable input delay
- Programmable Schmitt input and receiver

For more information on SmartFusion2 I/O programmable features, refer to the SmartFusion2 I/O Feature table of the *SmartFusion2 FPGA Fabric Architecture User's Guide*.

Impedance Calibration

There are two DDRIO calibration blocks in each SmartFusion2 M2S050T device. The MDDR and FDDR have a DDRIO calibration block. The DDRIO can use fixed impedance calibration for different drive strengths, and these values can be programmed using Libero SoC for the selected I/O standard. These values are fed to the pull-up/pull-down reference network to match the impedance with an external resistor.

Table 4-3 • **Reference Resistors**

Pin Name	Reference Resistor (Ohm)
FDDR_IMP_CALIB_ECC	Pulled down with 240, 150, 300, or 191 Ohms, depending on voltage/standard desired for optimization.
MDDR_IMP_CALIB_ECC	Pulled down with 240, 150, 300, or 191 Ohms, depending on voltage/standard desired for optimization.

For the different drive modes, refer to the *SmartFusion2 FPGA Fabric Architecture User's Guide* for reference resistor values.

Dedicated I/Os

Dedicated I/Os (Table 4-4 and Table 4-6 on page 4-8) can be used for a single purpose such as SERDES, device reset, or clock functions. SmartFusion2 dedicated I/Os:

- Device reset I/Os
- Crystal oscillator I/Os
- SERDES I/Os

Table 4-4 • **Device Reset and Crystal Oscillator Pin Types and Descriptions**

Pin	Type	I/O	Description
Device Reset I/Os			
DEVRST_N	Analog	Input	Device reset; asserted Low and powered by VPP
Crystal Oscillator I/Os			
EXTLOSC	Analog	Input	Crystal connection or external RC network.
XTLOSC	Analog	Input	Input clock from the main crystal oscillator

Table 4-5 • **Programming SPI Interface**

Name	Type	Description
SC_SPI_SS	Out	SPI slave select
SC_SPI_SDO	Out	SPI data output
SC_SPI_SDI	In	SPI data input
SC_SPI_CLK	Out	SPI clock
FLASH_GOLDEN	In	If pulled High, this indicates that the device is to be re-programmed from an image in the external SPI Flash attached to the SPI interface. If pulled Low, the SPI is put into slave mode.

SERDES I/Os

The SERDES I/Os available in SmartFusion2 devices are dedicated for high speed serial communication protocols. The SERDES I/Os support protocols such as PCI Express 2.0, XAUI, serial gigabit media independent interface (SGMII), serial rapid IO (SRIO), and any user-defined high speed serial protocol implementation in fabric.

Table 4-6 • **SERDES I/O Port Names and Descriptions**

Port Name	Type	Description
Data / Reference Pads		
PCIE_x_RXDP0	Input	Receive data. SERDES differential positive input for each lane. Each SERDESIF consists of 4 RX signals. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1. If unused, can be left floating.
PCIE_x_RXDP1		
PCIE_x_RXDP2		
PCIE_x_RXDP3		
PCIE_x_RXDN0	Input	Receive data. SERDES differential negative input for each lane. Each SERDESIF consists of 4 RX signals. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1. If unused, can be left floating.
PCIE_x_RXDN1		
PCIE_x_RXDN2		
PCIE_x_RXDN3		
PCIE_x_TXDP0	Output	Transmit data. SERDES differential positive output for each lane. Each SERDESIF consists of 4 TX signals. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1. If unused, can be left floating.
PCIE_x_TXDP1		
PCIE_x_TXDP2		
PCIE_x_TXDP3		
PCIE_x_TXDN0	Output	Transmit data. SERDES differential negative output for each lane. Each SERDESIF consists of 4 TX signals. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1. If unused, can be left floating.
PCIE_x_TXDN1		
PCIE_x_TXDN2		
PCIE_x_TXDN3		
Common I/O Pads per SERDES Interface		
PCIE_x_REXTL	Reference	External reference resistor connection to calibrate TX/RX termination value. Each SERDESIF consists of 2 REXT signals—one for lane0 and lane1, and another for lane2 and lane3. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1. If unused, can be left floating.
PCIE_x_REXTR		
PCIE_x_REFCLK0P	Clock	Reference clock differential positive. Each SERDESIF consists of two signals (REFCLK0_P, REFCLK1_P). These are dual purpose I/Os; you can use these lines for MSIOD fabric, if SERDESIF is not activated. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1. If unused, can be left floating.
PCIE_x_REFCLK1P		
PCIE_x_REFCLK0N	Clock	Reference clock differential negative. Each SERDESIF consists of two signals (REFCLK0_P, REFCLK1_P). These are dual purpose I/Os; you can use these lines for MSIOD fabric, if SERDESIF is not activated. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1. If unused, can be left floating.
PCIE_x_REFCLK1N		

JTAG Pins

SmartFusion2 devices have dedicated JTAG pins in bank 4. JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal).

The debug port is implemented using a serial wire JTAG debug port (SWJ-DP) rather than a serial wire debug port (SW-DP). This enables either the M3 JTAG or the SW protocol to be used for debugging.

Table 4-7 • **JTAG Pin Names and Descriptions**

Name	Type	Bus Size	Description
JTAGSEL	In	1	JTAG controller selection. Depending on the state of the JTAGSEL pin, an external JTAG controller will see the FPGA fabric TAP/auxiliary TAP (High) or the Cortex-M3 JTAG debug interface (Low). The JTAGSEL pin should be connected to an external pull-up resistor such that the default configuration selects the FPGA fabric TAP.
JTAG_TCK/ M3_TCK	In	1	Test clock. Serial input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/pull-down resistor. If JTAG is not used, Microsemi recommends tying it off. Connect TCK to GND or +3.3 V through a resistor placed close to the FPGA pin. This prevents totem-pole current on the input buffer and operation in case TMS enters an undesired state. Note that to operate at all +3.3 V voltages, 500 Ω to 1 kΩ will satisfy the requirements.
JTAG_TDI/ M3_TDI	In	1	Test data. Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.
JTAG_TDO/ M3_TDO/ M3_SWO	Out	1	Test data. Serial output for JTAG boundary scan, ISP, and UJTAG usage. The TDO pin does not have an internal pull-up/-down resistor. M3_SWO: Serial Wire Viewer output
JTAG_TMS/ M3_TMS/ M3_SWDIO		1	Test mode select. The TMS pin controls the use of the IEEE1532 boundary scan pins (TCK, TDI, TDO, and TRST). There is an internal weak pull-up resistor on the TMS pin. M3_SWDIO: Serial Wire Debug data input/output
JTAG_TRSTB/ M3_TRSTB		1	Boundary scan reset pin. The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor (1K) could be included to ensure the TAP is held in Reset mode. In critical applications, an upset in the JTAG circuit could allow entering an undesired JTAG state. In such cases, Microsemi recommends that you tie off TRST to GND through a resistor (1K) placed close to the FPGA pin. The TRSTB pin also resets the serial wire JTAG debug port (SWJ-DP) circuitry within the Cortex-M3 processor.

Microcontroller Subsystem (MSS)

Table 4-8 • **MSS Pin Names and Descriptions**

Name	Type	Description
Inter-Integrated Circuit (I2C) Peripherals		
I2C_0_SCL	In/out	I2C bus serial clock output. Can also be used as an MSS GPIO or USB_DATA1_C or fabric I/O.
I2C_0_SDA	In/out	I2C bus serial data input/output. Can also be used as an MSS GPIO or USB_DATA0_C or fabric I/O.
I2C_1_SCL	in/out	I2C bus serial clock output. Can also be used as an MSS GPIO or USB_DATA4_A.
I2C_1_SDA	in/out	I2C bus serial data input/output. Can also be used as an MSS GPIO or USB_DATA3_A.
Universal Asynchronous Receiver/Transmitter (UART) Peripherals		
MMUART_0_CLK	Out	UART clock. Can also be used as an MSS GPIO or USB_NXT_C or fabric I/O.
MMUART_0_TXD	Out	UART transmit data. Can also be used as an MSS GPIO or USB_DIR_C or fabric I/O.
MMUART_0_RXD	In	UART receive data. Can also be used as an MSS GPIO or USB_STP_C or fabric I/O.
MMUART_0_CTS	In	UART clear to send. Can also be used as an MSS GPIO or USB_DATA7_C or fabric I/O.
MMUART_0_RTS	Out	UART request to send. Can also be used as an MSS GPIO or USB_DATA5_C or fabric I/O.
MMUART_0_DTR	Out	Modem data terminal ready. Can also be used as an MSS GPIO or USB_DATA6_C or fabric I/O.
MMUART_0_DCD	In	Modem data carrier detects. Can also be used as an MSS GPIO or fabric I/O.
MMUART_0_DSR	In	Modem data set ready. Can also be used as an MSS GPIO or fabric I/O.
MMUART_0_RI	In	Modem ring indicator. Can also be used as an MSS GPIO or fabric I/O.
MMUART_1_CLK	Out	UART Clock. Can also be used as an MSS GPIO or USB_DATA4_C.
MMUART_1_TXD	Out	UART transmit data. Can also be used as an MSS GPIO or USB_DATA2_C or fabric I/O.
MMUART_1_RXD	In	UART receive data. Can also be used as an MSS GPIO or USB_DATA3_C or fabric I/O.
MMUART_1_CTS	In	UART clear to send. Can also be used as an MSS GPIO or fabric I/O.
MMUART_1_RTS	Out	UART request to send. Can also be used as an MSS GPIO or fabric I/O.
MMUART_1_DTR	Out	Modem data terminal ready. Can also be used as an MSS GPIO or fabric I/O.

Table 4-8 • **MSS Pin Names and Descriptions (continued)**

Name	Type	Description
MMUART_1_DCD	In	Modem data carrier detects. Can also be used as an MSS GPIO or fabric I/O.
MMUART_1_DSR	In	Modem data set ready. Can also be used as an MSS GPIO or fabric I/O.
MMUART_1_RI	In	Modem ring indicator. Can also be used as an MSS GPIO or fabric I/O.
Serial Peripheral Interface (SPI) Controllers		
SPI_0_SS0	Out	SPI slave select0. Can also be used as an MSS GPIO or USB_NXT_A or fabric I/O.
SPI_0_SS1	Out	SPI slave select1. Can also be used as an MSS GPIO or USB_DATA5_A or fabric I/O.
SPI_0_SS2	Out	SPI slave select2. Can also be used as an MSS GPIO or USB_DATA6_A or fabric I/O.
SPI_0_SS3	Out	SPI slave select3. Can also be used as an MSS GPIO or USB_DATA7_A or fabric I/O.
SPI_0_SS4	Out	SPI slave select4. Can also be used as an MSS GPIO or fabric I/O.
SPI_0_SS5	Out	SPI slave select5. Can also be used as an MSS GPIO or fabric I/O.
SPI_0_SS6	Out	SPI slave select6. Can also be used as an MSS GPIO or fabric I/O.
SPI_0_SS7	Out	SPI slave select7. Can also be used as an MSS GPIO or fabric I/O.
SPI_0_CLK	Out	SPI clock. Can also be used as an MSS GPIO or USB_XCLK_A.
SPI_0_SDO	Out	SPI data output. Can also be used as an MSS GPIO or USB_STP_A or fabric I/O.
SPI_0_SDI	In	SPI data input. Can also be used as an MSS GPIO or USB_DIR_A or fabric I/O.
SPI_1_SS0	Out	SPI slave select0. Can also be used as an MSS GPIO or fabric I/O.
SPI_1_SS1	Out	SPI slave select1. Can also be used as an MSS GPIO or fabric I/O.
SPI_1_SS2	Out	SPI slave select2. Can also be used as an MSS GPIO or fabric I/O.
SPI_1_SS3	Out	SPI slave select3. Can also be used as an MSS GPIO or fabric I/O.
SPI_1_SS4	Out	SPI slave select4. Can also be used as an MSS GPIO or fabric I/O.

Table 4-8 • **MSS Pin Names and Descriptions (continued)**

Name	Type	Description
SPI_1_SS5	Out	SPI slave select5. Can also be used as an MSS GPIO or fabric I/O.
SPI_1_SS6	Out	SPI slave select6. Can also be used as an MSS GPIO or fabric I/O.
SPI_1_SS7	Out	SPI slave select7. Can also be used as an MSS GPIO or fabric I/O.
SPI_1_CLK	Out	SPI clock. Can also be used as an MSS GPIO.
SPI_1_SDO	Out	SPI data output. Can also be used as an MSS GPIO or fabric I/O.
SPI_1_SDI	In	SPI data input. Can also be used as an MSS GPIO or fabric I/O.

Multi-Function I/Os

Certain I/Os can have more than one function. Users select the functionality through Libero configuration tools.

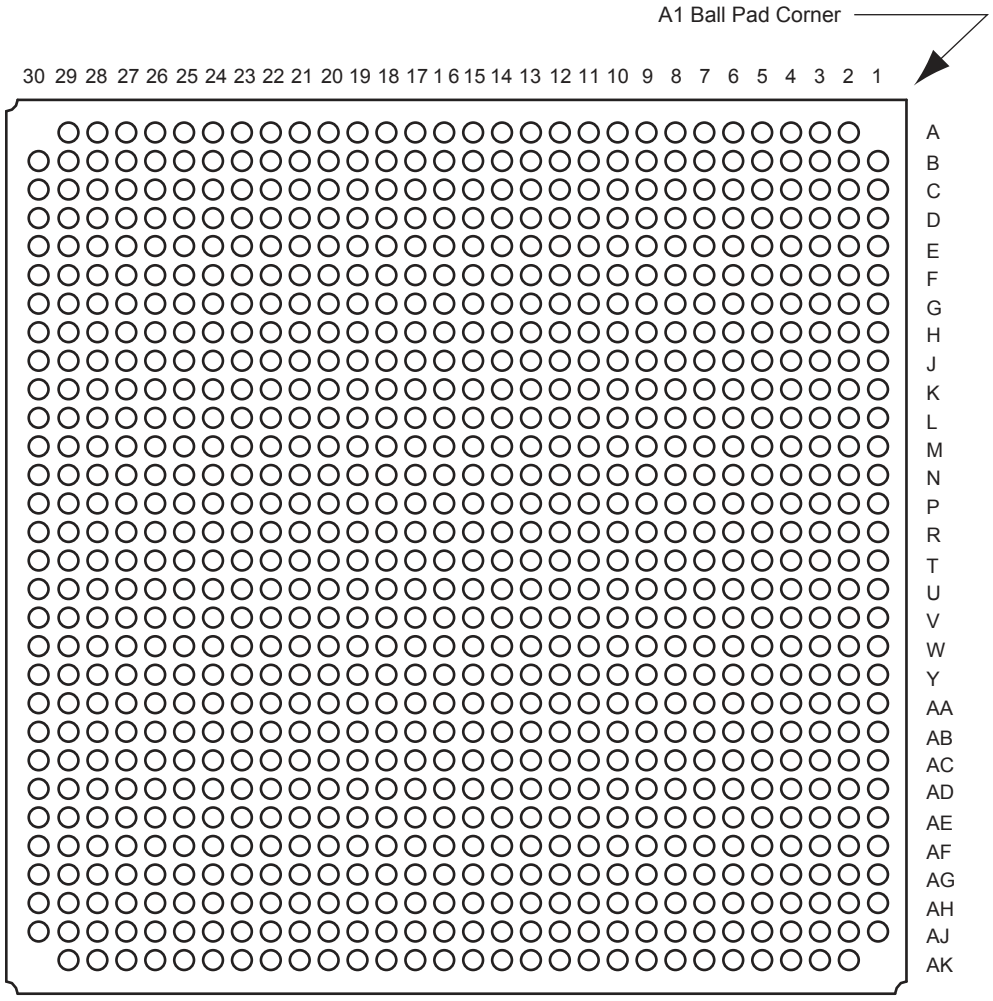
The name of a pin shows the functionalities for which that pin can be configured and used.

Example pin name: **MSIO48NB1/I2C_0_SCL/GPIO_31_B/USB_DATA1_C**

This I/O port is multi-purpose and can be configured as MSIO, I2C0 clock, fabric I/O, or USB_DATA1_C.

Pin Assignment Tables

FG896



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

FG896	
Pin Number	**M2S050T Function**
A2	PCIE_1_TXDN0
A3	VSS
A4	PCIE_1_TXDN1
A5	VSS
A6	PCIE_1_TXDN2
A7	VSS
A8	PCIE_1_TXDN3
A9	DDRIO91PB0/GB0/CCC_NW0_I3
A10	DDRIO90PB0/MDDR_DQS_ECC
A11	DDRIO88PB0/MDDR_DQ32_ECC
A12	DDRIO86PB0/MDDR_DQ0
A13	DDRIO84PB0/MDDR_DQS0
A14	DDRIO83NB0/MDDR_DQ4
A15	DDRIO80PB0/MDDR_DQ8
A16	DDRIO78PB0/GB8/CCC_NE0_I3/MDDR_DQS1
A17	DDRIO76PB0/GB12/CCC_NE1_I2/MDDR_DQ12
A18	DDRIO74PB0/MDDR_DQ16
A19	DDRIO72PB0/MDDR_DQS2
A20	DDRIO71NB0/MDDR_DQ20
A21	DDRIO68PB0/MDDR_DQ24
A22	DDRIO66NB0/MDDR_DQS3_N
A23	DDRIO64PB0/MDDR_DQ28
A24	DDRIO60PB0/MDDR_RST_N
A25	DDRIO59PB0/MDDR_CLK
A26	DDRIO57PB0/MDDR_BA2
A27	DDRIO55PB0/MDDR_ADDR3
A28	DDRIO55NB0/MDDR_ADDR4
A29	VSS
AA1	MSIOD134NB7
AA2	MSIOD134PB7
AA3	MSIOD129NB7
AA4	MSIOD136NB7
AA5	MSIOD141NB7
AA6	PCIE_0_REXTL
AA7	PLL_PCIE_0_VSSA
AA8	PLL_PCIE_0_VDDA

FG896	
Pin Number	**M2S050T Function**
AA9	PCIE_0_REXTR
AA10	PLL4_VSSA
AA11	PCIE0VDDIOL
AA12	PCIE0VDDIOR
AA13	VDDI5
AA14	VDDI5
AA15	VDDI5
AA16	VDDI5
AA17	VDDI5
AA18	VDDI5
AA19	VDDI5
AA20	VDDI5
AA21	VDD
AA22	VSS
AA23	PLL_FDDR_VSSA
AA24	VDDI4
AA25	JTAGSEL
AA26	MSIO2PB3/USB_STP_B
AA27	MSIO2NB3/USB_NXT_B
AA28	MSIO7NB3/CAN_TX/GPIO_2_A/USB_DATA0_A
AA29	MSIO8NB3/CAN_TX_EN_N/GPIO_4_A/USB_DATA2_A
AA30	SC_SPI_CLK
AB1	MSIOD135NB7
AB2	MSIOD135PB7
AB3	VDDI7
AB4	MSIOD137NB7
AB5	PCIE0VDD
AB6	VSS
AB7	VSS
AB8	PCIE_0_RXDP0
AB9	PCIE_0_RXDN0
AB10	PCIE_0_RXDP2
AB11	PCIE_0_RXDN2
AB12	PCIE0VDD
AB13	VSS
AB14	VSS

FG896	
Pin Number	**M2S050T Function**
AB15	VSS
AB16	VSS
AB17	VSS
AB18	VSS
AB19	VSS
AB20	VREF5
AB21	XTLOSC
AB22	EXTLOSC
AB23	PLL_FDDR_VDDA
AB24	VSS
AB25	JTAG_TRSTB/M3_TRSTB
AB26	MSIO0NB3/USB_DATA7_B
AB27	JTAG_TMS/M3_TMS/M3_SWDIO
AB28	VSS
AB29	MSIO6PB3/USB_DATA6_B
AB30	MSIO6NB3
AC1	MSIOD138NB7
AC2	MSIOD138PB7
AC3	MSIOD140NB7
AC4	MSIOD143PB7
AC5	VSS
AC6	VSS
AC7	PCIE0VDDPLLL
AC8	PCIE0PLLREFRETL
AC9	PCIE_0_RXDP1
AC10	PCIE_0_RXDN1
AC11	VPP
AC12	VSS
AC13	VDD
AC14	VDD
AC15	VDD
AC16	VDD
AC17	VDD
AC18	VDD
AC19	VDD
AC20	VSS

FG896	
Pin Number	**M2S050T Function**
AC21	VSS
AC22	VSS
AC23	VSS
AC24	VDDI4
AC25	JTAG_TDO/M3_TDO/M3_SWO
AC26	JTAG_TCK/M3_TCK
AC27	DEVRST_N
AC28	MSIO1PB3/USB_XCLK_B
AC29	MSIO1NB3/USB_DIR_B
AC30	MSIO5NB3/USB_DATA5_B
AD1	MSIOD139NB7
AD2	MSIOD139PB7
AD3	MSIOD143NB7
AD4	VSS
AD5	VSS
AD6	VSS
AD7	VSS
AD8	VSS
AD9	PCIE0PLLREFRETR
AD10	PCIE_0_RXDP3
AD11	PCIE_0_RXDN3
AD12	DDRIO150PB5/FDDR_FIFO_WE_IN_ECC
AD13	VREF5
AD14	VSS
AD15	VSS
AD16	VREF5
AD17	VSS
AD18	VSS
AD19	VSS
AD20	VSS
AD21	VSS
AD22	VSS
AD23	VSS
AD24	VSS
AD25	VSS
AD26	VSS

FG896	
Pin Number	**M2S050T Function**
AD27	VSS
AD28	VSS
AD29	VSS
AD30	MSIO5PB3/USB_DATA4_B
AE1	MSIOD146NB6/PCIE_0_REFCLK1N
AE2	MSIOD144NB7
AE3	VSS
AE4	VSS
AE5	VSS
AE6	VSS
AE7	VSS
AE8	VSS
AE9	PCIE0VDDPLLR
AE10	VDDI5
AE11	DDRIO147PB5/FDDR_FIFO_WE_OUT_ECC
AE12	VSS
AE13	VDDI5
AE14	DDRIO158NB5/FDDR_FIFO_WE_OUT1
AE15	DDRIO162PB5/FDDR_FIFO_WE_IN1
AE16	VDDI5
AE17	VSS
AE18	DDRIO170NB5/FDDR_FIFO_WE_OUT3
AE19	VDDI5
AE20	VSS
AE21	DDRIO174PB5/FDDR_FIFO_WE_IN3
AE22	VDDI5
AE23	DDRIO185NB5/FDDR_ADDR6
AE24	DDRIO185PB5/FDDR_ADDR5
AE25	VDDI5
AE26	VSS
AE27	DDRIO189PB5/FDDR_ADDR12
AE28	VDDI5
AE29	DDRIO178NB5/FDDR_CS_N
AE30	MSIO4NB3/USB_DATA3_B
AF1	MSIOD146PB6/PCIE_0_REFCLK1P
AF2	VSS

FG896	
Pin Number	**M2S050T Function**
AF3	VSS
AF4	VSS
AF5	VSS
AF6	VSS
AF7	VSS
AF8	VSS
AF9	FDDR_IMP_CALIB_ECC
AF10	VDDI5
AF11	DDRIO152PB5/GB3/CCC_SW0_I3/FDDR_DQ34_ECC
AF12	DDRIO154NB5/FDDR_DQ3
AF13	VDDI5
AF14	DDRIO157NB5/FDDR_DQ6
AF15	DDRIO160NB5/FDDR_DQ11
AF16	VDDI5
AF17	DDRIO164PB5/VCCC_SE1/FDDR_DQ14
AF18	DDRIO166NB5/FDDR_DQ19
AF19	VDDI5
AF20	DDRIO169NB5/FDDR_DQ22
AF21	DDRIO172NB5/FDDR_DQ27
AF22	VDDI5
AF23	DDRIO176PB5/FDDR_DQ30
AF24	DDRIO186NB5/FDDR_ADDR7
AF25	DDRIO186PB5/FDDR_ODT
AF26	VSS
AF27	DDRIO189NB5/FDDR_ADDR13
AF28	VDDI5
AF29	DDRIO178PB5/FDDR_CKE
AF30	VSS
AG1	VSS
AG2	VSS
AG3	VSS
AG4	VSS
AG5	VSS
AG6	VSS
AG7	VSS
AG8	VSS

FG896	
Pin Number	**M2S050T Function**
AG9	DDRIO147NB5/CCC_SW0_I2
AG10	DDRIO150NB5/FDDR_DM_RDQS4_ECC
AG11	DDRIO152NB5/GB7/CCC_SW1_I2/FDDR_DQ35_ECC
AG12	DDRIO154PB5/FDDR_DQ2
AG13	DDRIO156PB5/FDDR_DM_RQDS0
AG14	DDRIO157PB5/FDDR_DQ5
AG15	DDRIO160PB5/VCCC_SE0/FDDR_DQ10
AG16	DDRIO162NB5/FDDR_DM_RQDS1
AG17	DDRIO164NB5/FDDR_DQ15
AG18	DDRIO166PB5/FDDR_DQ18
AG19	DDRIO168PB5/FDDR_DM_RQDS2
AG20	DDRIO169PB5/FDDR_DQ21
AG21	DDRIO172PB5/FDDR_DQ26
AG22	DDRIO174NB5/FDDR_DM_RQDS3
AG23	DDRIO176NB5/FDDR_DQ31
AG24	DDRIO181PB5/FDDR_BA0
AG25	DDRIO181NB5/FDDR_BA1
AG26	VDDI5
AG27	DDRIO187PB5/FDDR_ADDR8
AG28	DDRIO187NB5/FDDR_ADDR9
AG29	DDRIO190PB5/FDDR_ADDR14
AG30	DDRIO177PB5/FDDR_RAS_N
AH1	VSS
AH2	VSS
AH3	VSS
AH4	VSS
AH5	VSS
AH6	VSS
AH7	VSS
AH8	VSS
AH9	VSS
AH10	VDDI5
AH11	VSS
AH12	VSS
AH13	VDDI5
AH14	VSS

FG896	
Pin Number	**M2S050T Function**
AH15	VSS
AH16	VDDI5
AH17	VSS
AH18	VSS
AH19	VDDI5
AH20	VSS
AH21	VSS
AH22	VDDI5
AH23	VSS
AH24	VSS
AH25	VDDI5
AH26	VSS
AH27	DDRIO183PB5/FDDR_ADDR1
AH28	VDDI5
AH29	DDRIO190NB5/FDDR_ADDR15
AH30	DDRIO177NB5/FDDR_WE_N
AJ1	VSS
AJ2	PCIE_0_TXDP0
AJ3	VSS
AJ4	PCIE_0_TXDP1
AJ5	VSS
AJ6	PCIE_0_TXDP2
AJ7	VSS
AJ8	PCIE_0_TXDP3
AJ9	DDRIO148NB5/PROBE_B
AJ10	DDRIO149NB5/FDDR_DQS_ECC_N
AJ11	DDRIO151NB5/FDDR_DQ33_ECC
AJ12	DDRIO153NB5/FDDR_DQ1
AJ13	DDRIO155NB5/FDDR_DQS0_N
AJ14	DDRIO158PB5/FDDR_DQ7
AJ15	DDRIO159NB5/FDDR_DQ9
AJ16	DDRIO161NB5/FDDR_DQS1_N
AJ17	DDRIO163NB5/FDDR_DQ13
AJ18	DDRIO165NB5/FDDR_DQ17
AJ19	DDRIO167NB5/FDDR_DQS2_N
AJ20	DDRIO170PB5/FDDR_DQ23

FG896	
Pin Number	**M2S050T Function**
AJ21	DDRIO171NB5/FDDR_DQ25
AJ22	DDRIO173PB5/FDDR_DQS3
AJ23	DDRIO175NB5/FDDR_DQ29
AJ24	DDRIO179NB5/FDDR_CAS_N
AJ25	DDRIO180NB5/FDDR_CLK_N
AJ26	DDRIO182NB5/FDDR_ADDR0
AJ27	DDRIO183NB5/FDDR_ADDR2
AJ28	DDRIO188NB5/FDDR_ADDR11
AJ29	DDRIO188PB5/FDDR_ADDR10
AJ30	VSS
AK2	PCIE_0_TXDN0
AK3	VSS
AK4	PCIE_0_TXDN1
AK5	VSS
AK6	PCIE_0_TXDN2
AK7	VSS
AK8	PCIE_0_TXDN3
AK9	DDRIO148PB5/PROBE_A
AK10	DDRIO149PB5/FDDR_DQS_ECC
AK11	DDRIO151PB5/FDDR_DQ32_ECC
AK12	DDRIO153PB5/FDDR_DQ0
AK13	DDRIO155PB5/FDDR_DQS0
AK14	DDRIO156NB5/FDDR_DQ4
AK15	DDRIO159PB5/CCC_SW1_I3/FDDR_DQ8
AK16	DDRIO161PB5/GB11/VCCC_SE0/FDDR_DQS1
AK17	DDRIO163PB5/GB15/VCCC_SE1/FDDR_DQ12
AK18	DDRIO165PB5/FDDR_DQ16
AK19	DDRIO167PB5/FDDR_DQS2
AK20	DDRIO168NB5/FDDR_DQ20
AK21	DDRIO171PB5/FDDR_DQ24
AK22	DDRIO173NB5/FDDR_DQS3_N
AK23	DDRIO175PB5/FDDR_DQ28
AK24	DDRIO179PB5/FDDR_RST_N
AK25	DDRIO180PB5/FDDR_CLK
AK26	DDRIO182PB5/FDDR_BA2
AK27	DDRIO184PB5/FDDR_ADDR3

FG896	
Pin Number	**M2S050T Function**
AK28	DDRIO184NB5/FDDR_ADDR4
AK29	VSS
B1	VSS
B2	PCIE_1_TXDP0
B3	VSS
B4	PCIE_1_TXDP1
B5	VSS
B6	PCIE_1_TXDP2
B7	VSS
B8	PCIE_1_TXDP3
B9	DDRIO91NB0/GB4/CCC_NW1_I2
B10	DDRIO90NB0/MDDR_DQS_ECC_N
B11	DDRIO88NB0/MDDR_DQ33_ECC
B12	DDRIO86NB0/MDDR_DQ1
B13	DDRIO84NB0/MDDR_DQS0_N
B14	DDRIO81PB0/MDDR_DQ7
B15	DDRIO80NB0/MDDR_DQ9
B16	DDRIO78NB0/MDDR_DQS1_N
B17	DDRIO76NB0/MDDR_DQ13
B18	DDRIO74NB0/MDDR_DQ17
B19	DDRIO72NB0/MDDR_DQS2_N
B20	DDRIO69PB0/MDDR_DQ23
B21	DDRIO68NB0/MDDR_DQ25
B22	DDRIO66PB0/MDDR_DQS3
B23	DDRIO64NB0/MDDR_DQ29
B24	DDRIO60NB0/MDDR_CAS_N
B25	DDRIO59NB0/MDDR_CLK_N
B26	DDRIO57NB0/MDDR_ADDR0
B27	DDRIO56NB0/MDDR_ADDR2
B28	DDRIO51NB0/MDDR_ADDR11
B29	DDRIO51PB0/MDDR_ADDR10
B30	VSS
C1	VSS
C2	VSS
C3	VSS
C4	VSS

FG896	
Pin Number	**M2S050T Function**
C5	VSS
C6	VSS
C7	VSS
C8	VSS
C9	VSS
C10	VDDI0
C11	VSS
C12	VSS
C13	VDDI0
C14	VSS
C15	VSS
C16	VDDI0
C17	VSS
C18	VSS
C19	VDDI0
C20	VSS
C21	VSS
C22	VDDI0
C23	VSS
C24	VSS
C25	VDDI0
C26	VSS
C27	DDRIO56PB0/MDDR_ADDR1
C28	VDDI0
C29	DDRIO49NB0/MDDR_ADDR15
C30	DDRIO62NB0/MDDR_WE_N
D1	VSS
D2	VSS
D3	VSS
D4	VSS
D5	VSS
D6	VSS
D7	VSS
D8	VSS
D9	DDRIO92NB0/CCC_NW0_I2
D10	DDRIO89NB0/MDDR_DM_RQDS4_ECC

FG896	
Pin Number	**M2S050T Function**
D11	DDRIO87NB0/MDDR_DQ35_ECC
D12	DDRIO85PB0/MDDR_DQ2
D13	DDRIO83PB0/MDDR_DM_RQDS0
D14	DDRIO82PB0/MDDR_DQ5
D15	DDRIO79PB0/CCC_NE0_I2/MDDR_DQ10
D16	DDRIO77NB0/MDDR_DM_RQDS1
D17	DDRIO75NB0/MDDR_DQ15
D18	DDRIO73PB0/MDDR_DQ18
D19	DDRIO71PB0/MDDR_DM_RQDS2
D20	DDRIO70PB0/MDDR_DQ21
D21	DDRIO67PB0/MDDR_DQ26
D22	DDRIO65NB0/MDDR_DM_RQDS3
D23	DDRIO63NB0/MDDR_DQ31
D24	DDRIO58PB0/MDDR_BA0
D25	DDRIO58NB0/MDDR_BA1
D26	VDDI0
D27	DDRIO52PB0/MDDR_ADDR8
D28	DDRIO52NB0/MDDR_ADDR9
D29	DDRIO49PB0/MDDR_ADDR14
D30	DDRIO62PB0/MDDR_RAS_N
E1	MSIOD94NB9/PCIE_1_REFCLK0N
E2	VSS
E3	VSS
E4	VSS
E5	VSS
E6	VSS
E7	VSS
E8	VSS
E9	MDDR_IMP_CALIB_ECC
E10	VDDI0
E11	DDRIO87PB0/CCC_NW1_I3/MDDR_DQ34_ECC
E12	DDRIO85NB0/MDDR_DQ3
E13	VDDI0
E14	DDRIO82NB0/MDDR_DQ6
E15	DDRIO79NB0/MDDR_DQ11
E16	VDDI0

FG896	
Pin Number	**M2S050T Function**
E17	DDRIO75PB0/CCC_NE1_I3/MDDR_DQ14
E18	DDRIO73NB0/MDDR_DQ19
E19	VDDI0
E20	DDRIO70NB0/MDDR_DQ22
E21	DDRIO67NB0/MDDR_DQ27
E22	VDDI0
E23	DDRIO63PB0/MDDR_DQ30
E24	DDRIO53NB0/MDDR_ADDR7
E25	DDRIO53PB0/MDDR_ODT
E26	VSS
E27	DDRIO50NB0/MDDR_ADDR13
E28	VDDI0
E29	DDRIO61PB0/MDDR_CKE
E30	VSS
F1	MSIOD94PB9/PCIE_1_REFCLK0P
F2	MSIO108NB8
F3	VSS
F4	VSS
F5	VSS
F6	VSS
F7	VSS
F8	VSS
F9	PCIE1VDDPLLR
F10	VDDI0
F11	DDRIO92PB0/MDDR_FIFO_WE_OUT_ECC
F12	VSS
F13	VDDI0
F14	DDRIO81NB0/MDDR_FIFO_WE_OUT1
F15	DDRIO77PB0/MDDR_FIFO_WE_IN1
F16	VDDI0
F17	VSS
F18	DDRIO69NB0/MDDR_FIFO_WE_OUT3
F19	VDDI0
F20	VSS
F21	DDRIO65PB0/MDDR_FIFO_WE_IN3
F22	VDDI0

FG896	
Pin Number	**M2S050T Function**
F23	DDRIO54NB0/MDDR_ADDR6
F24	DDRIO54PB0/MDDR_ADDR5
F25	VSS
F26	VDDI0
F27	DDRIO50PB0/MDDR_ADDR12
F28	VDDI0
F29	DDRIO61NB0/MDDR_CS_N
F30	MSIO45NB1/MMUART_0_DCD/GPIO_22_B
G1	MSIO100NB8
G2	MSIO95PB8
G3	MSIO95NB8
G4	VSS
G5	VSS
G6	VSS
G7	VSS
G8	VSS
G9	PCIE1PLLREFRETR
G10	PCIE_1_RXDP3
G11	PCIE_1_RXDN3
G12	DDRIO89PB0/MDDR_FIFO_WE_IN_ECC
G13	VREF0
G14	VSS
G15	VSS
G16	VREF0
G17	VSS
G18	VSS
G19	VSS
G20	VSS
G21	VSS
G22	VSS
G23	VSS
G24	VSS
G25	VSS
G26	VSS
G27	VSS
G28	FLASH_GOLDEN

FG896	
Pin Number	**M2S050T Function**
G29	MSIO42NB1/MMUART_1_RXD/GPIO_26_B/USB_DATA3_C
G30	MSIO45PB1/MMUART_0_RI/GPIO_21_B
H1	MSIO99PB8
H2	MSIO99NB8
H3	VDDI8
H4	MSIO96NB8
H5	VSS
H6	VSS
H7	PCIE1VDDPLLL
H8	PCIE1PLLREFRETL
H9	PCIE_1_RXDP1
H10	PCIE_1_RXDN1
H11	VSS
H12	VSS
H13	VDD
H14	VDD
H15	VDD
H16	VDD
H17	VDD
H18	VDD
H19	VDD
H20	VSS
H21	VSS
H22	VSS
H23	VSS
H24	PLL0_VDDA
H25	PLL0_VSSA
H26	MSIO47NB1/MMUART_0_CLK/GPIO_29_B/USB_NXT_C
H27	MSIO46NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C
H28	MSIO40NB1/MMUART_1_DCD/GPIO_16_B
H29	MSIO42PB1/GB14/VCCC_SE1/MMUART_1_CLK/GPIO_25_B/USB_DATA4_C
H30	MSIO41NB1/MMUART_1_TXD/GPIO_24_B/USB_DATA2_C
J1	MSIO102PB8
J2	MSIO102NB8
J3	MSIO98PB8
J4	MSIO98NB8

FG896	
Pin Number	**M2S050T Function**
J5	VSS
J6	VSS
J7	VSS
J8	PCIE_1_RXDP0
J9	PCIE_1_RXDN0
J10	PCIE_1_RXDP2
J11	PCIE_1_RXDN2
J12	PCIE1VDD
J13	VSS
J14	VSS
J15	VSS
J16	VSS
J17	VSS
J18	VSS
J19	VSS
J20	VREF0
J21	VSS
J22	PLL_MDDR_VDDA
J23	PLL_MDDR_VSSA
J24	PLL1_VSSA
J25	PLL1_VDDA
J26	MSIO43NB1/MMUART_0_DTR/GPIO_18_B/USB_DATA6_C
J27	MSIO35NB2/GPIO_6_B
J28	MSIO38NB1/MMUART_1_DTR/GPIO_12_B
J29	MSIO38PB1/MMUART_1_RTS/GPIO_11_B
J30	MSIO41PB1/GB10/VCCC_SE0/USB_XCLK_C
K1	VSS
K2	VDDI8
K3	MSIO101NB8
K4	VSS
K5	MSIO97NB8
K6	PCIE_1_REXTL
K7	PLL_PCIE_1_VSSA
K8	PLL_PCIE_1_VDDA
K9	PCIE_1_REXTR
K10	PLL3_VDDA

FG896	
Pin Number	**M2S050T Function**
K11	PCIE1VDDIOL
K12	PCIE1VDDIOR
K13	VDDI0
K14	VDDI0
K15	VDDI0
K16	VDDI0
K17	VDDI0
K18	VDDI0
K19	VDDI0
K20	VDDI0
K21	VDD
K22	VSS
K23	MSIO48PB1/I2C_0_SDA/GPIO_30_B/USB_DATA0_C
K24	MSIO48NB1/I2C_0_SCL/GPIO_31_B/USB_DATA1_C
K25	MSIO44NB1/MMUART_0_DSR/GPIO_20_B
K26	VDDI1
K27	VSS
K28	MSIO34NB2/GPIO_4_B
K29	MSIO37NB2/GPIO_10_B
K30	MSIO37PB2/GPIO_9_B
L1	MSIO104NB8
L2	MSIO103PB8
L3	MSIO103NB8
L4	MSIO113NB8
L5	VSS
L6	MSIOD93PB9/PCIE_1_REFCLK1P
L7	MSIOD93NB9/PCIE_1_REFCLK1N
L8	PCIE1VDD
L9	PLL2_VSSA
L10	PLL3_VSSA
L11	VSS
L12	VSS
L13	VSS
L14	VSS
L15	VSS
L16	VSS

FG896	
Pin Number	**M2S050T Function**
L17	VSS
L18	VSS
L19	VSS
L20	VSS
L21	VDDI1
L22	VDD
L23	MSIO47PB1/MMUART_0_RXD/GPIO_28_B/USB_STP_C
L24	VSS
L25	VDDI1
L26	MSIO39NB1/MMUART_1_DSR/GPIO_14_B
L27	VDDI2
L28	MSIO34PB2/GPIO_3_B
L29	MSIO33NB2/GPIO_2_B
L30	MSIO33PB2/GPIO_1_B
M1	MSIO107PB8
M2	MSIO107NB8
M3	MSIO106PB8
M4	MSIO106NB8
M5	05NB8
M6	VDDI8
M7	VDDI9
M8	MSIO97PB8
M9	PLL2_VDDA
M10	VDD
M11	VSS
M12	VSS
M13	VSS
M14	VSS
M15	VSS
M16	VSS
M17	VSS
M18	VSS
M19	VSS
M20	VSS
M21	VSS
M22	VSS

FG896	
Pin Number	**M2S050T Function**
M23	MSIO44PB1/MMUART_0_CTS/GPIO_19_B/USB_DATA7_C
M24	MSIO43PB1/MMUART_0_RTS/GPIO_17_B/USB_DATA5_C
M25	MSIO40PB1/CCC_NE1_I1/MMUART_1_RI/GPIO_15_B
M26	MSIO36NB2/GPIO_8_B
M27	MSIO32NB2/GPIO_0_B
M28	MSIO30NB2/USB_DATA7_D/GPIO_23_B
M29	VSS
M30	MSIO29NB2/USB_DATA5_D
N1	MSIO111PB8
N2	MSIO111NB8
N3	MSIO110PB8
N4	MSIO110NB8
N5	MSIO109NB8
N6	MSIO100PB8
N7	MSIO96PB8
N8	MSIO101PB8
N9	MSIO104PB8
N10	VDDI8
N11	VSS
N12	VSS
N13	VSS
N14	VSS
N15	VSS
N16	VSS
N17	VSS
N18	VSS
N19	VSS
N20	VSS
N21	VDDI1
N22	VDD
N23	MSIO39PB1/CCC_NE0_I1/MMUART_1_CTS/GPIO_13_B
N24	MSIO36PB2/GPIO_7_B
N25	MSIO35PB2/GPIO_5_B
N26	MSIO31NB2/GPIO_30_A
N27	MSIO30PB2/USB_DATA6_D
N28	MSIO29PB2/USB_DATA4_D

FG896	
Pin Number	**M2S050T Function**
N29	MSIO28NB2/USB_DATA3_D
N30	MSIO26NB2/USB_NXT_D
P1	MSIO115PB8/GB2/CCC_NW0_I1
P2	MSIO115NB8
P3	MSIO114PB8/GB6/CCC_NW1_I1
P4	MSIO114NB8
P5	MSIO112NB8
P6	MSIO105PB8
P7	MSIO108PB8
P8	MSIO112PB8
P9	MSIO116PB8/CCC_NW1_I0
P10	VDD
P11	VSS
P12	VSS
P13	VSS
P14	VSS
P15	VSS
P16	VSS
P17	VSS
P18	VSS
P19	VSS
P20	VSS
P21	VDDI2
P22	VSS
P23	MSIO32PB2/GPIO_31_A
P24	MSIO31PB2/GPIO_29_A
P25	MSIO28PB2/USB_DATA2_D
P26	MSIO27PB2/USB_DATA0_D
P27	MSIO27NB2/USB_DATA1_D
P28	MSIO26PB2/USB_STP_D
P29	MSIO25NB2/USB_DIR_D
P30	MSIO25PB2/USB_XCLK_D
R1	MSIOD119PB7/GB1/CCC_SW0_I1
R2	MSIOD119NB7
R3	MSIOD118PB7/GB5/CCC_SW1_I1
R4	MSIOD118NB7

FG896	
Pin Number	**M2S050T Function**
R5	MSIO116NB8
R6	MSIO117NB8
R7	MSIO109PB8
R8	MSIO113PB8
R9	MSIO117PB8/CCC_NW0_I0
R10	VDDI8
R11	VSS
R12	VSS
R13	VSS
R14	VSS
R15	VSS
R16	VSS
R17	VSS
R18	VSS
R19	VSS
R20	VSS
R21	VDDI2
R22	VDD
R23	VPP
R24	MSIO24PB3/SPI_1_SS2/GPIO_15_A
R25	MSIO23PB3/SPI_0_SS3/GPIO_10_A/USB_DATA7_A
R26	VDDI2
R27	VSS
R28	MSIO24NB3/SPI_1_SS3/GPIO_16_A
R29	MSIO23NB3/SPI_1_SS1/GPIO_14_A
R30	MSIO22NB3/SPI_0_SS2/GPIO_9_A/USB_DATA6_A
T1	MSIOD120NB7
T2	VSS
T3	VDDI7
T4	MSIOD121NB7
T5	MSIOD125NB7
T6	MSIOD128PB7
T7	MSIOD120PB7/CCC_SW1_I0
T8	MSIOD124PB7
T9	MSIOD133PB7
T10	VDD

FG896	
Pin Number	**M2S050T Function**
T11	VSS
T12	VSS
T13	VSS
T14	VSS
T15	VSS
T16	VSS
T17	VSS
T18	VSS
T19	VSS
T20	VSS
T21	VSS
T22	VSS
T23	VSSNVM
T24	MSIO20PB3/GB9/VCCC_SE0/GPIO_25_A
T25	VDDI3
T26	MSIO21PB3/GPIO_27_A
T27	MSIO21NB3/GPIO_28_A
T28	MSIO20NB3/GB13/VCCC_SE1/GPIO_26_A
T29	VPPNVM
T30	MSIO22PB3/SPI_0_SS1/GPIO_8_A/USB_DATA5_A
U1	MSIOD122NB7
U2	MSIOD122PB7
U3	MSIOD123NB7
U4	MSIOD123PB7
U6	MSIOD136PB7
U7	MSIOD121PB7/CCC_SW0_I0
U8	MSIOD125PB7
U9	MSIOD132PB7
U10	VDDI7
U11	VSS
U12	VSS
U13	VSS
U14	VSS
U15	VSS
U16	VSS
U17	VSS

FG896	
Pin Number	**M2S050T Function**
U18	VSS
U19	VSS
U20	VSS
U21	VDDI3
U22	VDD
U23	MSIO16PB3/SPI_1_CLK
U24	MSIO15PB3/SPI_0_SS6/GPIO_21_A
U25	MSIO19PB3/SPI_1_SS6/GPIO_23_A
U26	MSIO15NB3/SPI_0_SS7/GPIO_22_A
U27	MSIO16NB3/SPI_1_SDI/GPIO_11_A
U28	VDDI3
U29	VSS
U30	MSIO19NB3/SPI_1_SS7/GPIO_24_A
V1	MSIOD127PB7
V2	MSIOD127NB7
V3	MSIOD126NB7
V4	MSIOD126PB7
V5	MSIOD130PB7
V6	MSIOD129PB7
V7	MSIOD144PB7
V8	MSIOD140PB7
V9	MSIOD145PB6/PCIE_0_REFCLK0P
V10	MSIOD145NB6/PCIE_0_REFCLK0N
V11	VSS
V12	VSS
V13	VSS
V14	VSS
V15	VSS
V16	VSS
V17	VSS
V18	VSS
V19	VSS
V20	VSS
V21	VSS
V22	MSIO12PB3/SPI_0_CLK/USB_XCLK_A
V23	MSIO11PB3/CCC_NE0_I0/I2C_1_SDA/GPIO_0_A/USB_DATA3_A

FG896	
Pin Number	**M2S050T Function**
V24	MSIO8PB3/CAN_RX/GPIO_3_A/USB_DATA1_A
V25	VPP
V26	MSIO11NB3/CCC_NE1_I0/I2C_1_SCL/GPIO_1_A/USB_DATA4_A
V27	MSIO17PB3/SPI_1_SDO/GPIO_12_A
V28	MSIO17NB3/SPI_1_SS0/GPIO_13_A
V29	MSIO18PB3/SPI_1_SS4/GPIO_17_A
V30	MSIO18NB3/SPI_1_SS5/GPIO_18_A
W1	MSIOD128NB7
W2	VSS
W3	VDDI7
W4	MSIOD132NB7
W5	MSIOD130NB7
W6	MSIOD133NB7
W7	MSIOD141PB7
W8	MSIOD137PB7
W9	VDDI6
W10	VDDI7
W11	VSS
W12	VSS
W13	VSS
W14	VSS
W15	VSS
W16	VSS
W17	VSS
W18	VSS
W19	VSS
W20	VSS
W21	VDDI3
W22	VDD
W23	MSIO7PB3
W24	MSIO3PB3/USB_DATA0_B
W25	MSIO4PB3/USB_DATA2_B
W26	SC_SPI_SS
W27	MSIO13PB3/SPI_0_SDO/GPIO_6_A/USB_STP_A
W28	MSIO13NB3/SPI_0_SS0/GPIO_7_A/USB_NXT_A
W29	MSIO14PB3/SPI_0_SS4/GPIO_19_A

FG896	
Pin Number	**M2S050T Function**
W30	MSIO14NB3/SPI_0_SS5/GPIO_20_A
Y1	MSIOD131NB7
Y2	MSIOD131PB7
Y3	VDDI7
Y4	VSS
Y5	VSS
Y6	MSIOD142NB7
Y7	MSIOD142PB7
Y8	PLL5_VSSA
Y9	PLL4_VDDA
Y10	PLL5_VDDA
Y11	VSS
Y12	VSS
Y13	VSS
Y14	VSS
Y15	VSS
Y16	VSS
Y17	VSS
Y18	VSS
Y19	VSS
Y20	VSS
Y21	VDDI4
Y22	MSIO0PB3
Y23	JTAG_TDI/M3_TDI
Y24	VPP
Y25	MSIO3NB3/USB_DATA1_B
Y26	VDDI3
Y27	VSS
Y28	SC_SPI_SDI
Y29	SC_SPI_SDO
Y30	MSIO12NB3/SPI_0_SDI/GPIO_5_A/USB_DIR_A

5 – Datasheet Information

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "SmartFusion2 Device Status" table on page VI, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

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