Your Imagination, Our Creation

GL602USB
GL602USB-A

USB KEYBOARD MICROCONTROLLER

SPECIFICATION 1.6
Feb. 28, 2001

Genesys Logic, Inc.
10F, No.11, Ln.3, Tsao Ti Wei, Shenkeng, Taipei, Taiwan
Tel: +886-2-2664-6655 Fax: +886-2-2664-5757
http://www.genesyslogic.com/

Index

Figures

Tables

1. FEATURES

- Low-cost solution for low-speed USB keyboard
- 8-bit micro-controller
  - Operation Speed: 6MHz clock input
  - Performance: 3 MIPS @ 6MHz
  - Single cycle instruction execution
  - RISC-like architecture
  - USB optimized instruction set
- USB Specification Compliance
  - Conforms to USB 12Mbps Specification, Version 1.1
  - Conforms to USB HID Class Specification, Version 1.1
  - Supports 1 device address and 4 endpoints (include endpoint 0)
- I/O ports
  - Up to 7(GL602USB)/5(GL602USB-A) general purpose I/O pins (OTP type is less a GPIO pin than mask type).
  - Up to 8 sense pins and 1 I/O pin with remote wakeup capability
  - Up to 18(GL602USB)/8(GL602USB-A) output pins optimized for key matrix drive pin
  - Up to 8(GL602USB)/4(GL602USB-A) output pins optimized for key matrix sense pin
  - Up to 3(GL602USB)/1(GL602USB-A) I/O pins with LED drive capability
- Internal memory
  - 96 bytes of RAM
  - 4K x 14 of program ROM
- On-chip 3.3v output
  - No external regulator required
- Improved output drivers with slew-rate control to reduce EMI
- 6 MHz external clock
- Internal power-on reset (POR)
- Internal power-fail detector
- Supports suspend/normal mode power management
  - Suspend current lower than 400μA for the whole keyboard system (mask type)
- 8-bit free-running timer
- Available in cost saving 40-pin(GL602USB) PDIP, 24-pin(GL602USB-A) SOP
- Support a PS/2 mouse to USB mouse converter in the default firmware.

2. FUNCTIONAL OVERVIEW

The GL602USB is an 8-bit RISC-like high performance microcontroller with a built-in 1.5Mbps SIE and transceiver. The microcontroller features 33 instructions optimized for USB keyboard. There are 96 bytes on-chip RAM and 4K x 14 bits program ROM incorporated into the micro-controller. The micro-controller features 18 output pins and 8 input pins to make a 18 x 8 key matrix. Additionally, 3 GPIO pins are strong enough to drive LEDs. 4 GPIO pins can be used by any function, for example, support a PS/2 3D mouse to USB 3D mouse converter in the default firmware. Legacy USB cable can be used for keyboard in USB mode. All GPIO ports feature low EMI emissions as a result of improved output drivers with slew-rate control.

3. PIN DEFINITIONS AND DESCRIPTIONS

3.1 GL602USB

Table 3-1 GL602USB Pin Definitions and Descriptions

Pin No.	Name	I/O	Description
1	GND	-	Ground
2	V3.3	O	3.3V output
3	D+	I/O	USB data+
4	D-	I/O	USB data-
5	DRV1	O	Key matrix output drive 1, open drain output
6	DRV2	O	Key matrix output drive 2, open drain output
7	P1.1/MOUSE CLK	I/O	Port 1 bit 1 / PS2 mouse clock input
8	P1.2/MOUSE DATA	I/O	Port 1 bit 2 / PS2 mouse data input
9	P1.3/VPP	I/O	Port 1 bit 3 (for mask) / 12.75V programming power (for OTP)
10	P1.4/PWRCTL	I/O	Port 1 bit 4 / PS2 mouse power control
11	DRV3	O	Key matrix output drive 3, open drain output
12	DRV4	O	Key matrix output drive 4, open drain output
13	DRV5	O	Key matrix output drive 5, open drain output
14	DRV6	O	Key matrix output drive 6, open drain output
15	DRV7	O	Key matrix output drive 7, open drain output
16	DRV8	O	Key matrix output drive 8, open drain output
17	DRV9	O	Key matrix output drive 9, open drain output
18	DRV10	O	Key matrix output drive 10, open drain output
19	DRV11	O	Key matrix output drive 11, open drain output
20	DRV12	O	Key matrix output drive 12, open drain output
21	DRV13	O	Key matrix output drive 13, open drain output
22	DRV14	O	Key matrix output drive 14, open drain output
23	DRV15	O	Key matrix output drive 15, open drain output
24	DRV16	O	Key matrix output drive 16, open drain output
25	DRV17	O	Key matrix output drive 17, open drain output
26	DRV18	O	Key matrix output drive 18, open drain output
27	SENSE1	I	Key matrix input sense 1, internal pull up 10K
28	SENSE2	I	Key matrix input sense 2, internal pull up 10K
29	SENSE3	I	Key matrix input sense 3, internal pull up 10K
30	SENSE4	I	Key matrix input sense 4, internal pull up 10K
31	SENSE5	I	Key matrix input sense 5, internal pull up 10K
32	SENSE6	I	Key matrix input sense 6, internal pull up 10K
33	SENSE7	I	Key matrix input sense 7, internal pull up 10K
34	SENSE8	I	Key matrix input sense 8, internal pull up 10K
35	P1.5/NUMLOCK	I/O	Port 1 bit 5/number lock indicator, internal pull up
36	P1.6/CAPSLOCK	I/O	Port 1 bit 6/caps lock indicator, internal pull up
37	P1.7/SCROLLLOCK	I/O	Port 1 bit 7/scroll lock indicator, internal pull up
38	VDD	-	Voltage supply
39	XTAL1	O	Ceramic resonator or crystal out
40	XTAL2	I	Ceramic resonator or crystal in

Note 1: Name or description after "/" means default function specified by Genesys Logic firmware

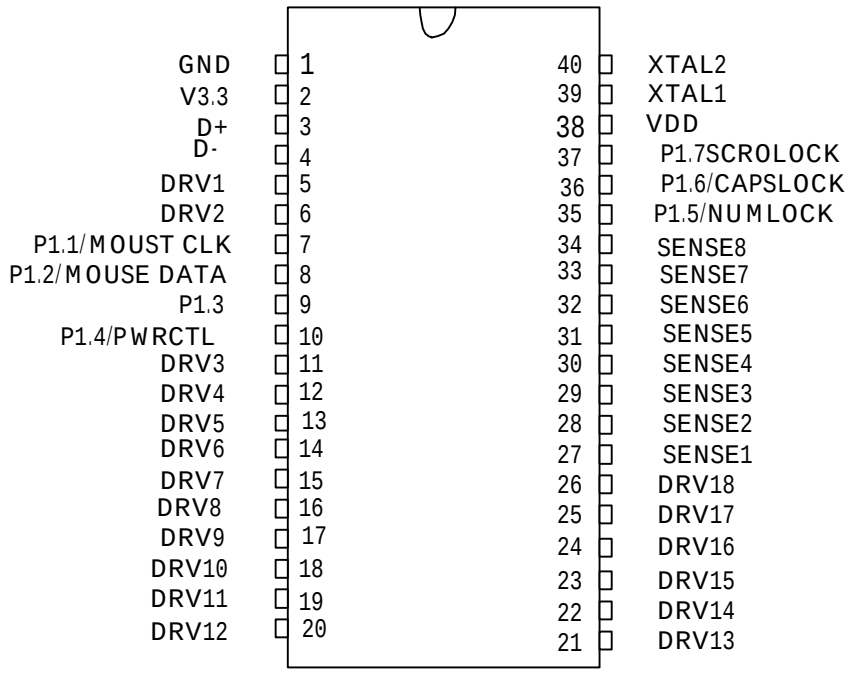


Figure 3-1 40-pin DIP (GL602USB)

3.2 GL602USB-A

Table 3-2 GL602USB-A Pin Definitions and Descriptions

Pin No.	Name	I/O	Description
1	GND	-	Ground
2	V3.3	O	3.3V output
3	D+	I/O	USB data+
4	D-	I/O	USB data-
5	P1.1/MOUSE CLK	I/O	Port 1 bit 1/PS2 mouse clock input
6	P1.2/MOUSE DATA	I/O	Port 1 bit 2/PS2 mouse data input
7	P1.3/VPP	I/O	Port 1 bit 3 (for mask) / 12.75V programming power (for OTP)
8	P1.4/PWRCTL	I/O	Port 1 bit 4 / PS2 mouse power control
9	DRV7	O	Key matrix output drive 7, open drain output
10	DRV8	O	Key matrix output drive 8, open drain output
11	DRV10	O	Key matrix output drive 10, open drain output
12	DRV12	O	Key matrix output drive 12, open drain output
13	DRV13	O	Key matrix output drive 13, open drain output
14	DRV15	O	Key matrix output drive 15, open drain output
15	DRV16	O	Key matrix output drive 16, open drain output
16	DRV17	O	Key matrix output drive 17, open drain output
17	SENSE1	I	Key matrix input sense 1, internal pull up 10K
18	SENSE3	I	Key matrix input sense 3, internal pull up 10K
19	SENSE6	I	Key matrix input sense 6, internal pull up 10K
20	SENSE8	I	Key matrix input sense 8, internal pull up 10K
21	P1.7/LED	I/O	Port 1 bit 7/LED indicator
22	VDD	-	Voltage supply
23	XTAL1	O	Ceramic resonator or crystal out
24	XTAL2	I	Ceramic resonator or crystal in

Note 1: Name or description after "/" means default function specified by Genesys Logic firmware

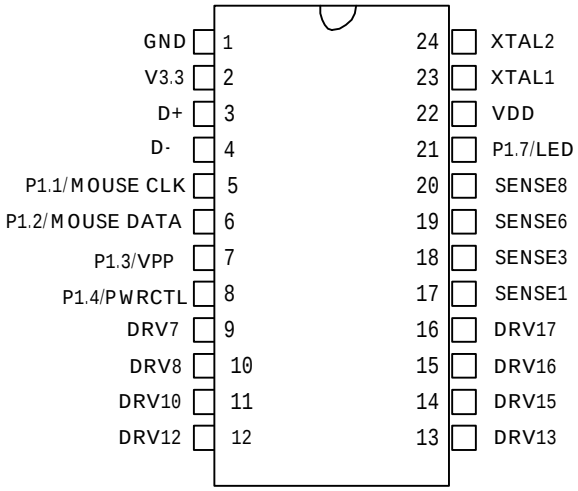


Figure 3-2 24-pin SOP (GL602USB-A)

4. FUNCTIONAL DESCRIPTION

The Genesys Logic GL602USB micro-controller is optimized for PC keyboard. This USB microcontroller conforms to the low-speed (1.5Mbps) requirements of the USB Specification version 1.1. The micro-controller is a self-contained unit with an USB SIE, an USB transceiver, an 8-bit RISC-like microcontroller, a timer, data and program memories. It supports one USB device address and four endpoints (include endpoint 0).

4.1 MEMORY ORGANIZATION

The memory in the microcontroller is organized into user program memory in program ROM and data memory in SRAM space.

4.1.1 Program Memory Organization

The 12-bit Program Counter (PC) is capable of addressing 4K x 14 of program space. All of the 4K * 14 ROM space can be used. The program memory space is divided into two functional groups: Interrupt Vectors and program code. After a reset, the Program Counter points to location zero of the program space and all registers are reset to the default value. After a timer interrupt, the Program Counter points the location 0x0004 of the program space.

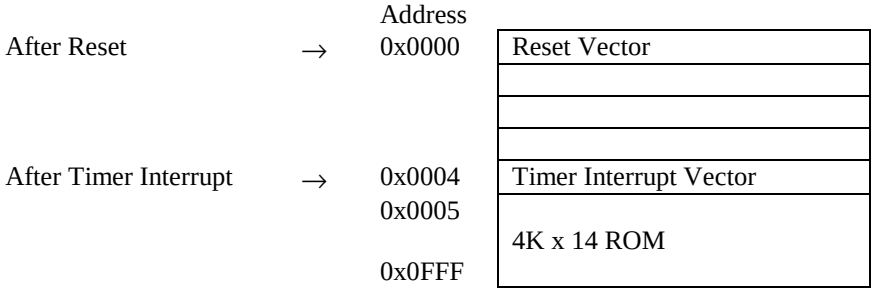


Figure 4-1 Program Memory Space

4.1.2 Data Memory Organization

The data memory is partitioned into two Banks that contain the General Purpose Registers, MCU Function Registers and USB Function Registers. Bit BS is the bank select bit.
BS (STATUS<5>) = 1 → Bank 1
BS (STATUS<5>) = 0 → Bank 0
The lower locations of each Bank are reserved for MCU Function Registers and USB Function Registers. Above the MCU Function Registers and USB Function Registers are General Purpose Registers implemented as SRAM. Both Bank 0 and Bank 1 contain MCU Function Registers. USB Function Registers are located in Bank 0. Some “high use” MCU Function Registers from Bank 0 are mirrored in Bank 1 for code reduction and quicker access.

Data Memory Address		Data Memory Address	
00h	INDR	80h	INDR
01h	TIMER	81h	PSCON
02h	PCL	82h	PCL
03h	STATUS	83h	STATUS
04h	INDAR	84h	INDAR
05h		85h	
06h	PORT1	86h	PORT1CON

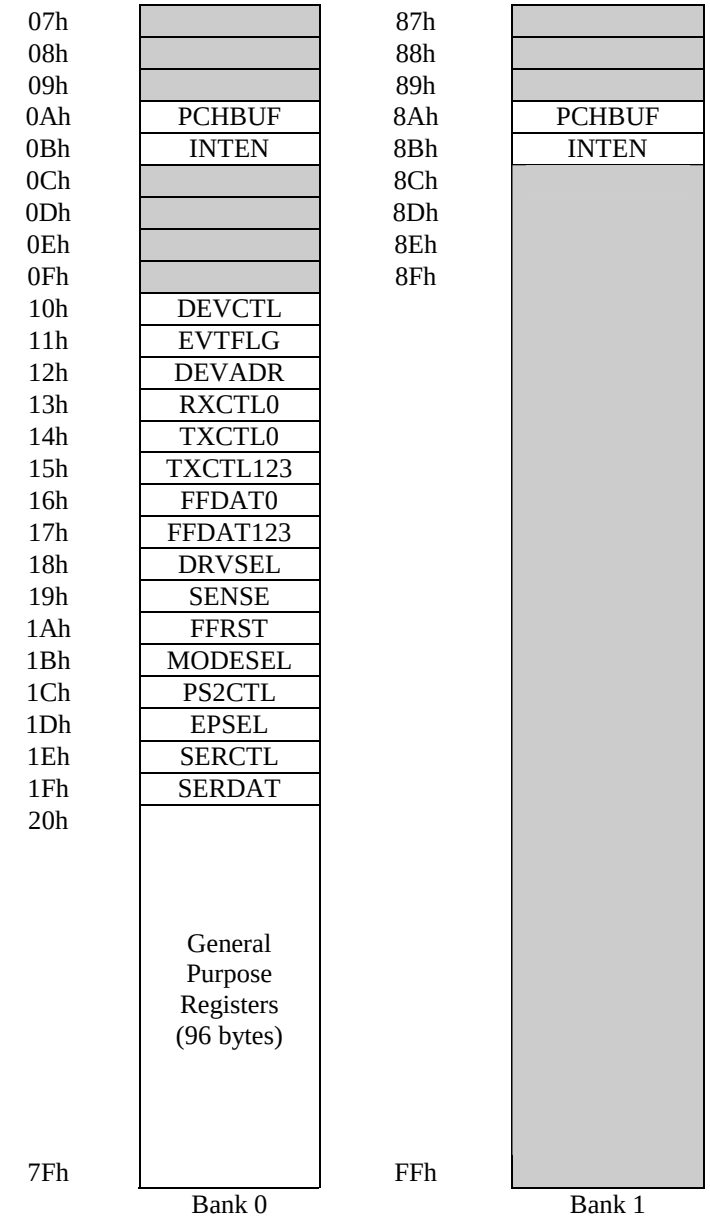


Figure 4-2 Data Memory Space

4.2 USB FUNCTION REGISTERS

Table 4-1 USB Function Register Summary

Address	Name	Function
10h	DEVCTL	Device control register
11h	EVTFLG	Event flag register
12h	DEVADR	USB device address register
13h	RXCTL0	Endpoint 0 receive control register
14h	TXCTL0	Endpoint 0 transmit control register
15h	TXCTL123	Endpoint 1/2/3 transmit control register
16h	FFDAT0	Endpoint 0 FIFO data port
17h	FFDAT123	Endpoint 1/2/3 FIFO data port
18h	DRVSEL	Key matrix drive pin control register
19h	SENSE	Key matrix sense register
1Ah	FFRST	FIFO reset register
1Bh	MODESEL	USB mode select register
1Ch	Reserved	
1Dh	EPSEL	Endpoint select register
1Eh	SERCTL	PS/2 mouse port control register
1Fh	SERDAT	PS/2 mouse port data register

DEVCTL (Address 10h, Device control register)

	R/W[1]	R/W	R/W	R/W	R/W	R/W	R/W
	EP3STL	EP2STL	EP1STL	EP0STL	WAKE	WKDIS	PWRDN

EP3STL: Endpoint 3 stall bit
1: Endpoint 3 will respond with a STALL to a valid transaction
0: Endpoint 3 will not respond with a STALL to a valid transaction
EP2STL: Endpoint 2 stall bit
1: Endpoint 2 will respond with a STALL to a valid transaction
0: Endpoint 2 will not respond with a STALL to a valid transaction
EP1STL: Endpoint 1 stall bit
1: Endpoint 1 will respond with a STALL to a valid transaction
0: Endpoint 1 will not respond with a STALL to a valid transaction
EP0STL: Endpoint 0 stall bit
1: Endpoint 0 will respond with a STALL to a valid transaction.
0: Endpoint 0 will not respond with a STALL to a valid transaction
WAKE: Wake-up bit
1: Set this bit to wake up host controller by placing USB bus into K state
0: Clear this bit to force USB bus leave K state
WKDIS: Wake-up disable bit
1: Disable remote wake-up capability
0: Enable remote wake-up capability
PWRDN: Power-down mode bit
1: Entering power-down mode
If USB suspend is detected, firmware should set this bit to enter power-down mode. In power-down mode, 6MHz crystal clock will be stopped. Hardware will automatically clear PWRDN bit upon hardware reset, USB D+/D- toggle, SENSE1~SENSE8 at logic '0', or Port 1.1 at logic '0'.
Value on POR: "0 0 0 0 0 0 0 0"
Note 1: "R/W" means readable and writable bit

EVTFLG (Address 11h, Event flag register)

R/W1C[1]	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C
WAKEUP	RESUME	SUSPD	EP3TX	EP2TX	EP1TX	EP0TX	EP0RX

WAKEUP: Remote wakeup bit
1: Remote wakeup from P1.1~P1.4 or SENSE1~SENSE8 was detected
0: Remote wakeup was not detected
RESUME: Global resume bit
1: Global resume (USB D+/D- toggle) was detected
0: Global resume was not detected
SUSPD: Global suspend bit
1: Global suspend (USB idle more than 3ms) was detected
0: Global suspend was not detected
EP3TX: Endpoint 3 transmitting status bit
1: Data has been sent from endpoint 3
0: Data has not been sent from endpoint 3
EP2TX: Endpoint 2 transmitting status bit
1: Data has been sent from endpoint 2
0: Data has not been sent from endpoint 2
EP1TX: Endpoint 1 transmitting status bit
1: Data has been sent from endpoint 1
0: Data has not been sent from endpoint 1
EP0TX: Endpoint 0 transmitting status bit
1: Data has been sent from endpoint 0
0: Data has not been sent from endpoint 0
EP0RX: Endpoint 0 receiving status bit
1: Data has been received by endpoint 0
0: Data has not been received by endpoint 0
Value on POR: "0 0 0 0 0 0 0 0"
Note 1: "R/W1C" means read-only and write "1" to clear bit

DEVADR (Address 12h, USB device address register)

	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	DADR6	DADR5	DADR4	DADR3	DADR2	DADR1	DADR0

Write this register to set the USB device address
Value on POR: "0 0 0 0 0 0 0 0"

RXCTL0 (Address 13h, Endpoint 0 receive control register)

R/W	R/O[1]	R/O	R/O	R/W	R/W	R/W	R/W
RXDIS	RXST2	RXST1	RXST0	RXCNT3	RXCNT2	RXCNT1	RXCNT0

RXDIS: Endpoint 0 receiving not available bit
1: Endpoint 0 FIFO is not available. The received data cannot be pushed into FIFO. The USB controller will respond with a NAK to a valid OUT transaction. This bit is set by hardware when endpoint 0 data is received (both SETUP and OUT transaction).
0: Endpoint 0 FIFO is available for data receiving
RXST[2:0]: RXST[2:0] indicate the PID received.

Bit Value	Packet received
100	SETUP token with DATA0 packet
010	OUT token with DATA0 packet
011	OUT token with DATA1 packet

RXCNT[3:0]: Number of bytes received from endpoint 0.
Value on POR: "0 X X X X X X X"
Note 1: "R/O" means read-only bit

TXCTL0 (Address 14h, Endpoint 0 transmit control register)

		R/W	R/W	R/W	R/W	R/W	R/W
		TXSEQ	TXOE	TXCNT3	TXCNT2	TXCNT1	TXCNT0

TXSEQ: Endpoint 0 transmitting sequence bit
1: Transmitting data use DATA1 as PID
0: Transmitting data use DATA0 as PID

TXOE: Endpoint 0 FIFO data ready bit

1: Endpoint 0 FIFO data are ready to be transmitted. Data will be transmitted when a valid IN token is received. This bit is automatically cleared by hardware after the transaction complete (ACK is received).

0: Endpoint 0 FIFO data are not ready to be transmitted and respond with a NAK to a valid IN transaction.

TXCNT[3:0]: Number of bytes to be sent by endpoint 0 when IN token is received

Value on POR: "0 0 0 0 0 0 0 0"

TXCTL123(Address 15h, Endpoint 1/2/3 transmit control register)

		R/W	R/W	R/W	R/W	R/W	R/W
		TXSEQ	TXOE	TXCNT3	TXCNT2	TXCNT1	TXCNT0

TXSEQ: Endpoint 1/2/3 transmitting sequence bit

1: Transmitting data use DATA1 as PID

0: Transmitting data use DATA0 as PID

TXOE: Endpoint 1/2/3 FIFO data ready bit

1: Endpoint 1/2/3 FIFO data are ready to be transmitted. Data will be transmitted when a valid IN token is received. This bit is automatically cleared by hardware after the transaction complete (ACK is received).

0: Endpoint 1/2/3 FIFO data are not ready to be transmitted and respond with a NAK to a valid IN transaction.

TXCNT[3:0]: Number of bytes to be sent by endpoint 0 when IN token is received

Value on POR: "0 0 0 0 0 0 0 0"

FFDAT0 (Address 16h, Endpoint 0 FIFO port)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
FFDAT7	FFDAT6	FFDAT5	FFDAT4	FFDAT3	FFDAT2	FFDAT1	FFDAT0

Endpoint 0 FIFO data port

Endpoint 0 FIFO is a 8 bytes FIFO. Firmware can read/write this port 8 times to get/put the FIFO data.

Value on POR: "X X X X X X X X"

FFDAT1/2/3 (Address 17h, Endpoint 1/2/3 FIFO port)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
FFDAT7	FFDAT6	FFDAT5	FFDAT4	FFDAT3	FFDAT2	FFDAT1	FFDAT0

Endpoint 1/2/3 FIFO data port

Endpoint 1 FIFO is 8 bytes FIFO. Firmware can read this port 8 times to get the FIFO data.

Endpoint 2 FIFO is 6 bytes FIFO. Firmware can read this port 6 times to get the FIFO data.

Endpoint 3 is 2 bytes FIFO only. Firmware can read this port 2 times to get the FIFO data.

Before read this register, firmware should selects endpoint via EPSEL register (address 1Dh).

Value on POR: "X X X X X X X X"

DRVSEL (Address 18h, Key matrix drive pin control register)

	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	INVDRV	DRVOE	DRV4	DRV3	DRV2	DRV1	DRV0

INVDRV: Inverse drive signal. This function can be used to detected ghost keys.

1: Drive all DRV1-18 to low except the selected pin when DRVOE is set

0: Drive the selected pin to low only when DRVOE is set

DRVOE: DRV1-18 output enable

1: Enable DRV1-18 pins to drive key matrix

0: Disable DRV1-18 pins and not to drive key matrix

DRV[4:0]: Select DRV1 to DRV18 port to drive low if DRVOE is set.

5'h00 selects DRV1

5'h01 selects DRV2

5'h0f selects DRV16

5'h10 selects DRV17

5'h11 selects DRV18

5'h12 ~ 5'h1f are invalid.

Value on POR: "0 0 0 0 0 0 0 0"

SENSE (Address 19h, Key matrix sense resister)

R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
SENSE8	SENSE7	SENSE6	SENSE5	SENSE4	SENSE3	SENSE2	SENSE1

Key matrix sense input port

All SENSE1~SENSE8 bits indicate state of the corresponding SENSE1~SENSE8 pins.

Value on POR: "X X X X X X X X"

FFRST (Address 1Ah, FIFO reset register)

				W/O	W/O		
				FFRST123	FFRST0		

FFRST123: Reset endpoint 1/2/3 FIFO read/write pointer

Write "1" to this bit will reset endpoint 1/2/3 FIFO read/write pointer. Data in endpoint 1/2/3 FIFO remain unchanged. Before data are written into endpoint 1/2/3 FIFO, EPSEL should be set correctly then FFRST123 should be set.

FFRST0: Reset endpoint 0 FIFO read/write pointer

Write "1" to this bit will reset endpoint 0 FIFO read/write pointer. Data in endpoint 0 FIFO remain unchanged. Before data are read/written into endpoint 0 FIFO, FFRST0 should be set first.

MODESEL (Address 1Bh, Mode select register)

						R/W	R/W
						OSCSTP	PWRON

OSCSTP: Suspend clock stop control bit

1: Clock is stopped while suspend

0: Clock is not stopped while suspend

PWRON: Power reset indicator

1: Power on reset detected

0: USB bus reset detected

Value on POR: "- - - - - - 0 1"

USBIOCTL (Address 1Ch, I/O control register for USB D+/D-)

				R/W	R/W	R/W	R/W
				DMOE	DPOE	DM	DP

DMOE: D- pin output enable control bit

1: D- pin digital output enable

0: D- pin digital output disable

DPOE: D+ pin output enable control bit

1: D+ pin digital output enable

0: D+ pin digital output disable

DM: Digital output value of D- pin. This pin is open drain output. Output high will be tri-stated.

DP: Digital output value of D+ pin. This pin is open drain output. Output high will be tri-stated.

Value on POR: "- - - - 1 1 0 0"

EPSEL (Address 1Dh, Endpoint select register)

					R/W	R/W	R/W
					EPSEL3	EPSEL2	EPSEL1

EPSEL[3: 1]: Endpoint select control bits

Bit Value	Endpoint to be selected
001	Endpoint 1
010	Endpoint 2
100	Endpoint 3

Value on POR: "- - - - - X X X"

SERCTL (Address 1Eh, PS/2 or RS232 mouse port control register)

					R/WC		R/W
					RXFLG		SRXEN

RXFLG: Data received flag on PS/2 interface

1: Data received and saved in SERBUF

0: No data received

SRXEN: Receiver enable bit for PS/2 interface

1: Enable serial port receiver

0: Disable serial port receiver

Value on POR: "- - - - - 0 - 0"

SERDAT (Address 1Fh, PS/2 mouse port data register)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SERDAT7	SERDAT6	SERDAT5	SERDAT4	SERDAT3	SERDAT2	SERDAT1	SERDAT0

SERDAT[7: 0]: PS/2 mouse data input port. This port is a 2 bytes FIFO. Therefore, about 1 mini-second delay is allowed between RXFLG in SERCTL register set and to read the PS/2 mouse data. If the 2 bytes FIFO full, GL602USB will drive the PS/2 clock low to avoid the mouse send more data.

Value on POR: "X X X X X X X X"

4.3 MCU FUNCTION REGISTERS

Table 4-2 MCU Function Register Summary

Address	Name	Function
00h	INDR	Addressing this location will use the content of INDAR to address data memory (not a physical address)
01h	TIMER	Timer register
02h	PCL	Program Counter's low byte
03h	STATUS	Status register
04h	INDAR	Indirect address register
05h	Reserved	
06h	PORT1	Port 1 data register
0Ah	PCHBUF	Write buffer of Program Counter's bit 11-8
0Bh	INTEN	Interrupt enable register
80h	INDR	Addressing this location will use the content of INDAR to address data memory (not a physical address)
81h	PSCON	Prescaler control register
82h	PCL	Program Counter's low byte
83h	STATUS	Status register
84h	INDAR	Indirect address register
85h	Reserved	
86h	PORT1CON	Port 1 direction control register
8Ah	PCHBUF	Write buffer of Program Counter's bit 12-8
8Bh	INTEN	Interrupt enable register

INDR (Address 00h/80h)
INDR is not a physical register. Addressing INDR register will cause indirect addressing. Any instruction using the INDF register actually accesses the register pointed by the INDAR register. The indirect addressing method only can be used for general purpose registers.

TIMER (Address 01h, Timer register)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
TIMER7	TIMER6	TIMER5	TIMER4	TIMER3	TIMER2	TIMER1	TIMER0

The timer starts to count up after power on reset. The TMROF bit at INTEN register will be set when the TIMER register overflows from FFh to 00h. If both TMROEN and GIE bits at INTEN register are set, an interrupt will be generated when TIMER register overflows.
Value on POR: "0 0 0 0 0 0 0 0"

PCL (Address 02h/82h, Program Counter's low byte)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0

The Program Counter (PC) is 12-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte is not directly readable or writable and comes from PCHBUF. The GL602USB has a 8 level deep x 11-bit wide hardware stake. The stake space is not part of either program or data space and the stack pointer is not readable or writable. The PC is pushed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is poped in the event of a RETIA, RETI or a RET instruction execution. PCHBUF is not affected by a push or pop operation.
Because branch address gotten from stack or direct from instruction is only 11 bits long, the highest bit will be loaded to PC from PCHBUF when branch instruction is executed.
When write to PCL command executed, all 4 bits of PCHBUF will be loaded to PC because PCL is only a 8 bits register.
Value on POR: "0 0 0 0 0 0 0 0"

STATUS (Address 03h, Status register)

		R/W			R/W	R/W	R/W
		BS			ZO	HC	CA

BS: Bank Select. Because only 7 bits (bit 0~bit 6) operand implied by instruction for register address, this bit is used as address bit 7 when register access.
1: Bank 1 (80h-FFh)
0: Bank 0 (00h-7Fh)

ZO: Zero bit
1: The result of last arithmetic or logic operation is zero
0: The result of last arithmetic or logic operation is not zero

HC: Half Carry/Borrow bit
1: Carry or not borrow from the 4th low order bit
0: Borrow or not carry from the 4th low order bit

CA: Carry/Borrow bit
1: Carry or not borrow from the most significant bit
0: Borrow or not carry from the most significant bit

Value on POR: "- - 0 - - 0 0 0"

INDAR: (Address 04h/84h, Indirect address register)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
INDAR7	INDAR6	INDAR5	INDAR4	INDAR3	INDAR2	INDAR1	INDAR0

Any instruction using the INDF register actually accesses the register pointed by the INDAR register.
Value on POR: "x x x x x x x x" [1]
Note 1: "x" means unknown

PORT1 (Address 06h, Port 1 data register)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PORT 1.7	PORT1.6	PORT1.5	PORT1.4	PORT1.3	PORT1.2	PORT1.1	

PORT1 is a 7-bits latch for Port 1.1~Port 1.7. Reading the PORT1 register gets the status on the pins. Writing to it will write to the port latch. All write operations are read-modify-write operations. PORT1CON is used to enable/disable every bits of the port latch.
Value on POR: "x x x x x x x -"

PCHBUF (Address 0Ah/8Ah, Write buffer of Program Counter's bit 11-8)

				R/W	R/W	R/W	R/W
				PCHBUF3	PCHBUF2	PCHBUF1	PCHBUF0

Write buffer for upper 4-bits of Program Counter. The upper byte of Program Counter is not directly accessible. PCHBUF is a holding register for the PC[11:8] that are transferred to the upper byte of the Program Counter when branch occur. Please see PCL register to get more detail information.
Value on POR: "- - - 0 0 0 0 0"

INTEN (Address 0Bh/8Bh, Interrupt enable register)

R/W		R/W			R/W		
GIE		TMROEN			TMROF		

GIE: Global interrupt enable bit
1: Enable all interrupts
0: Disable all interrupts

TMROEN: Timer overflow interrupt enable bit
1: Enable timer interrupt
0: Disable timer interrupt

TMROF: Timer overflow interrupt flag bit. This bit should be cleared to '0' by firmware after it is set by hardware.
1: Timer register has overflowed
0: Timer register did not overflow

Value on POR: "0 - 0 - - 0 - -"

PSCON (Address 81h, Prescaler control register)

				R/W	R/W	R/W	R/W
				PSDIS	PS2	PS1	PS0

PSDIS: Prescaler disable bit
1: Set prescaler disable
0: Set prescaler enable
PS[2:0]: Prescaler rate select bits. These bits are used to control timer speed. The following table means that how many instruction cycles the TIMER register should be added by 1 when PSDIS = 0.

Bit Value	Timer Rate (PSDIS = 0)
000	1:2
001	1:4
010	1:8
011	1:16
100	1:32
101	1:64
110	1:128
111	1:256

Value on POR: "- - - - 1 1 1 1"

PORT1CON (Address 86h, Port 1 direction control register)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	
P1CON7	P1CON6	P1CON5	P1CON4	P1CON3	P1CON2	P1CON1	

There is a data direction control bit to match every pin of Port 1. The direction control bits can configure these pins as output or input. Setting a PORT1CON register bit put the corresponding output driver in a hi-impedance mode. Clearing a bit in the PORT1CON register puts the contents of the output latch on the selected pin.
Value on POR: "1 1 1 1 1 1 1 -"

4.4 GENERAL PURPOSE I/O PORTS

Interface with peripherals is conducted via up to 7 GPIO signals. The 7 signals are located at port 1. The port 1 data register is located at data memory address 06h and direction control register is located at address 86h.
The GL602USB builds in a PS/2 host data receiver. While this receiver enabled, the Port 1.1 is treated as PS/2 CLK and Port 1.2 is treated as PS/2 DATA. Firmware uses these 2 pins to implement a PS/2 mouse host controller. When the PS/2 host want to send command to PS/2 device, firmware should drive the 2 I/O pins directly following PS/2 specification.
There are 2 bytes FIFO used as PS/2 data buffer. When the PS/2 receiver has received a data byte already and firmware does not read it yet, the PS/2 receiver can receive the next data byte into FIFO still. If the firmware cannot process the first byte until the second byte received complete, the PS/2 receiver will drive low on Port 1.1 (PS/2 CLK) automatically to avoid the PS/2 device send data again.
P1.3 is VPP pin at OTP. This I/O pin can be used only at mask type.
The Port 1.5/Port 1.6/Port 1.7 can be treat as general purpose output pins in output mode. There are internal pull up resistors on those pins. Firmware can drive high on these pins to turn off LEDs and drive low to turn off these pins. External resistors are needed for these LED pins to sink current .

4.5 TIMER INTERRUPT

The Timer Interrupt is generated when the TIMER register overflows from FFh to 00h. This overflow sets bit TMROF (INTEN<2>). The interrupt can be masked by clearing bit TMROEN (INTEN<5>). Bit TMROF must be cleared in software by the Timer module interrupt service routine otherwise the Timer Interrupt will not be generated again. If prescaler is disabled, the timer register will increase every instruction cycle. If prescaler is enabled, its increment cycle depends on PS0~PS2 bits in PSCON register.

4.6 USB ENGINE

The USB module contains three functional blocks: a 3.3-volt regulator, a low-speed USB transceiver, and the Serial Interface Engine (SIE). The USB module is only enabled under USB mode. The following description is the function of the regulator, transceiver, and SIE.

4.6.1 Voltage Regulator

The USB data lines are required by the USB specification to have a maximum output voltage between 2.8V and 3.6V. Because the GL602USB is a low speed USB device, the D- lines also are required to have an external 1.5-kΩ pull-up resistor connected between a data line and a voltage source between 3.0 V and 3.6 V. Since the power provided by the USB cable is specified to be between 4.4V and 5.0V, an on-chip regulator is used to drop the voltage to the appropriate level for sourcing the USB transceiver and external pull-up resistor. An output pin driven by the regulator is provided to source the 1.5-kΩ external resistor.

4.6.2 USB Transceiver

The USB transceiver provides the physical interface to the USB D+ and D- data lines. The transceiver is composed of two parts: an output driver circuit and a receiver.
The USB transceiver uses a differential output driver to drive the USB data signal onto the USB cable. The static output swing of the driver in its low state is below the V_{OL} of 0.3V with 1.5-kΩ load to 3.6V and in its high state is above the V_{OH} of 2.8V with 15-kΩ load to ground. The output swings between the differential high and low state are well balanced to minimize signal skew. Slew rate control on the driver is used to minimize the radiated noise and cross talk. The driver's outputs support 3-state operation to achieve bi-directional half-duplex operation. The driver can tolerate a voltage on the signal pins of –0.5V to 3.8V with respect to local ground reference without damage.

The rise and fall time of the signals on this cable are greater than 75ns to keep RFI (radio frequency interference) emissions under FCC (Federal Communications Commission) class B limits and less than 300ns to limit timing delays, signaling skews, and distortions. The driver reaches the specified static signal levels with smooth rise and fall times, and minimal reflections and ringing when driving the cable. This driver is used only on segments between low-speed devices and the ports to which they are connected.

USB data transmission is done with differential signals. A differential input receiver is used to accept the USB data signal. A differential 1 on the bus is represented by D+ being at least 200mV more positive than D- as seen at the receiver, and a differential 0 is represented by D- being at least 200mV more positive than D+ as seen at the receiver. The signal cross over point must be between 1.3V and 2.0V.

The receiver features an input sensitivity of 200mV when both differential data inputs are in the range of 0.8V and 2.5V with respect to the local ground reference. This is called the common mode input voltage range. Proper data reception also is achieved when the differential data lines are outside the common mode range. The receiver can tolerate static input voltage between –0.5V to 3.8V with respect to its local ground reference without damage. In addition to the differential receiver, there is a single-ended receiver for each of the two data lines.

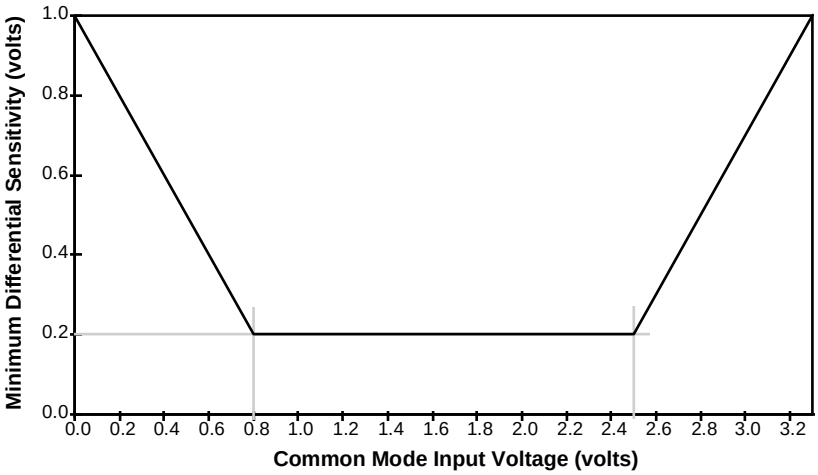


Figure 4-3 Differential Input Sensitivity over Entire Common Mode Range

The data receivers for all types of devices must be able to properly decode the differential data in the presence of jitter. The more of the bit time that any data edge can occupy and still be decoded, the more reliable the data transfer will be. Data receivers are required to decode differential data transitions that occur in a window plus and minus a nominal quarter bit time from the nominal (centered) data edge position. Jitter will be caused by the delay mismatches and by mismatches in the source and destination data rates (frequencies).

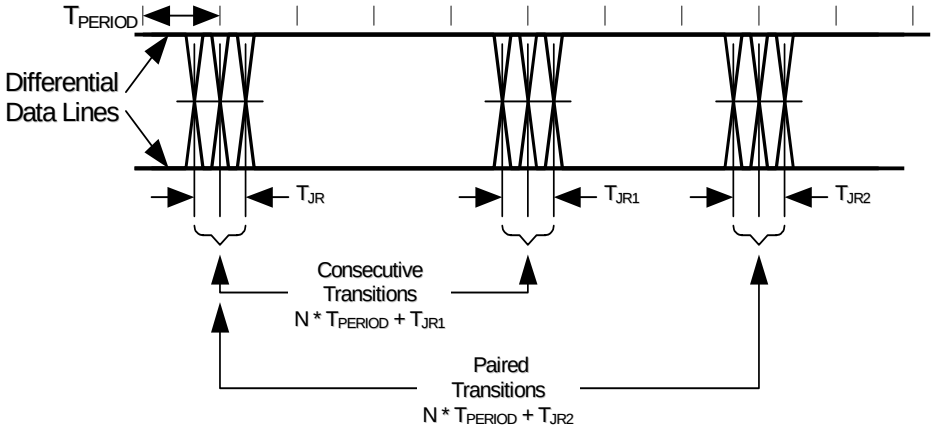


Figure 4-4 Receiver Jitter Tolerance

The source of data can have some variation (jitter) in the timing of edges of the data transmitted. The time between any set of data transitions is $N*T_{Period} \pm$ jitter time, where N is the number of bits between the transitions and T_{Period} is defined as the actual period of the data rate. The data jitter is measured with the same capacitive load used for maximum rise and fall times and is measured at the crossover points of the data lines.

For low-speed transmissions, the jitter time for any consecutive differential data transitions must be within ±25ns and within ±10ns for any set of paired differential data transitions. These jitter numbers include timing variations due to differential buffer delay, rise/fall time mismatches, internal clock source jitter, noise and other random effects.

The output rise time and fall time are measured between 10% and 90% of the signal. Edge transition time for the rising and falling edges of low-speed signals is 75ns (minimum) into a capacitive load (C_L) of 50pF and 300ns (maximum) into a capacitive load of 350pF. The rising and falling edges should be transitioning (monotonic) smoothly when driving the cable to avoid excessive EMI.

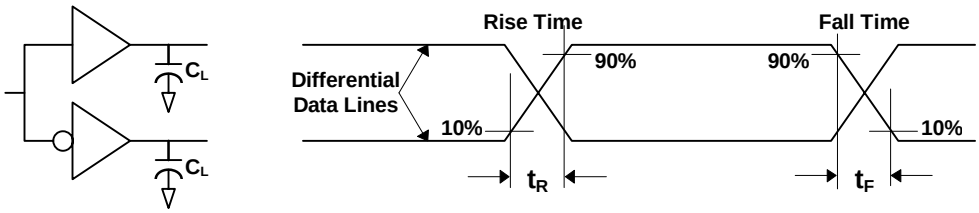


Figure 4-5 Data Signal Rise and Fall Time

4.6.3 Serial Interface Engine (SIE)

The SIE manages data movement between the CPU and the transceiver. The SIE handles both transmit and receive operations on the USB. It contains the logic used to manipulate the transceiver and the endpoint registers.

The byte count buffer is loaded from TXCNT(TXCTL0<3~0>) during endpoint 0 transmit operations. This same buffer is used for receive transactions to count the number of bytes received at endpoint 0 and, upon the end of transaction, transfer the value to RXCNT(RXCTL0<3~0>).

When transmitting, the SIE handles parallel-to-serial conversion, CRC generation, NRZI encoding, and bit stuffing. When receiving, the SIE handles sync detection, packet identification, end-of-packet detection, bit (un)stuffing, NRZI decoding, CRC validation, and serial-to-parallel conversion. Errors detected by the SIE include bad CRC, timeout while waiting for EOP, and bit stuffing violations.

All USB devices are required to have an endpoint 0 that is used to initialize and manipulate the device. Endpoint 0 provides access to the device's configuration information and allows generic USB status and control accesses. Endpoint 0 can receive and transmit data. Both receive and transmit data share the same 8-byte Endpoint 0 FIFO, FFDAT0. Received data may overwrite the data previously in the FIFO. Transmission from endpoint 0 is controlled by TXCTL0 and receiving from endpoint 0 is controlled by RXCTL0.

Endpoint 1/endpoint 2/endpoint 3 are of transmit only. Transmission from endpoint 1/endpoint 2/endpoint 3 is controlled by TXCTL123. The target endpoint should be chosen before writing to FFDAT123 and TXCTL123. There are separated FIFO buffer for the 3 endpoints, but the programming interface for them is unique, via FFDAT123 register. Size of endpoint 1 FIFO is 8 bytes, endpoint 2 FIFO is 6 bytes, and endpoint 3 FIFO is 2 bytes.

4.7 INSTRUCTION SET SUMMARY

4.7.1 Operand Field Descriptions

Field	Description
r	Register address
A	Accumulator
i	Immediate data
b	Bit address within a 8-bit register

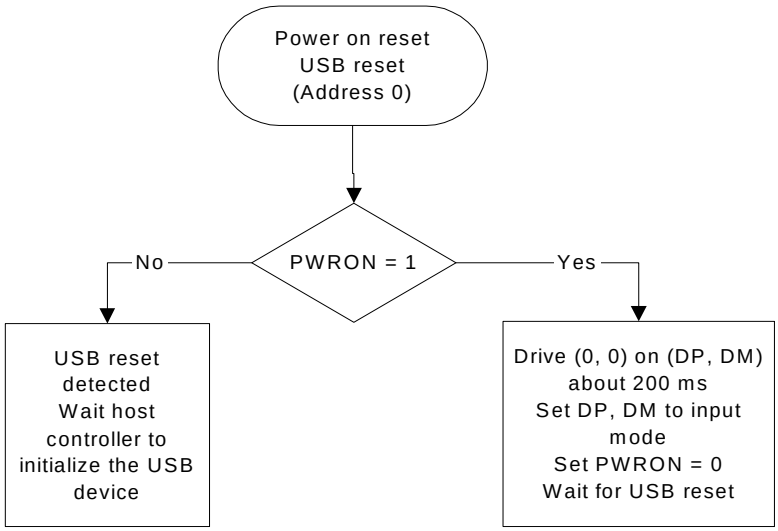
4.7.2 Instruction Set

Mnemonic, Operands	Description	Cycles	Flags Affected
Arithmetic Operations			

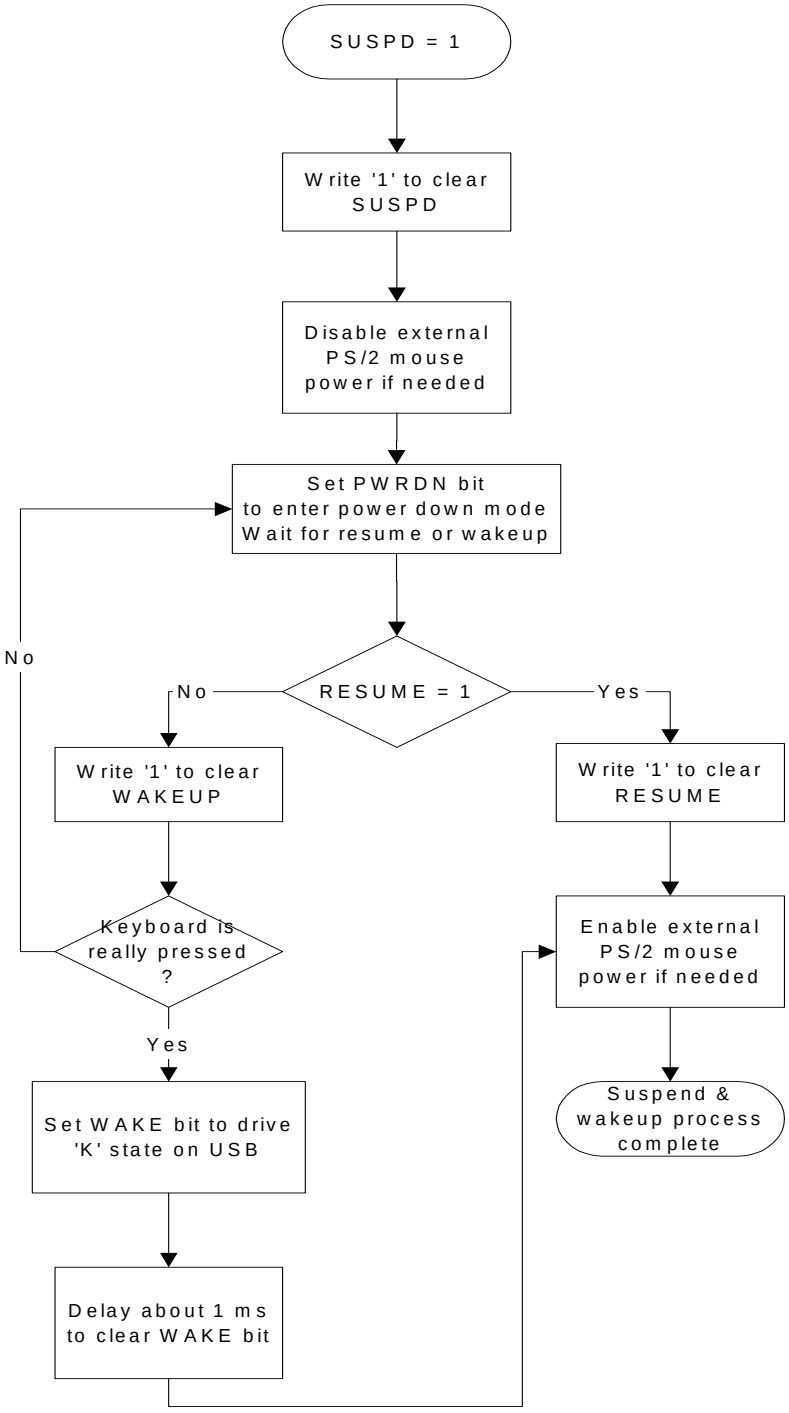
ADDAR r, A	Add r and A, r <- r + A	1	CA, HC, ZO
ADDAR A, r	Add A and r, A <- A + r	1	CA, HC, ZO
ADDAI i	Add A and i, A <- A + i	1	CA, HC, ZO
INCR r	Increment r, r <- r +1	1	ZO
INCR A, r	Increment r, A <- r + 1	1	ZO
INCRSZ r	Increment r, r <- r +1, skip if (r = 0)	1 or 2	
INCRSZ A, r	Increment r, A <- r +1, skip if (A = 0)	1 or 2	
SUBAR r, A	Subtract A from r, r <- r - A	1	CA, HC, ZO
SUBAR A, r	Subtract A from r, A <- r - A	1	CA, HC, ZO
SUBIA i	Subtract A from i, A <- i - A	1	CA, HC, ZO
DECR r	Decrement r, r <- r -1	1	ZO
DECR A, r	Decrement r, A <- r -1	1	ZO
DECRSZ r	Decrement r, r <- r-1, skip if (r = 0)	1 or 2	
DECRSZ A, r	Decrement r, A <- r -1, skip if (A = 0)	1 or 2	
CLRR r	Clear r, r <- 0	1	ZO
CLRA	Clear A, A <- 0	1	ZO
NOP	No operation	1	
Logical Operations			
ANDAR r, A	And r and A, r <- r & A	1	ZO
ANDAR A, r	And A and r, A <- A & r	1	ZO
ANDAI i	And A and i, A <- A & i	1	ZO
CMPR r	Complement r, r <- r ^ FF	1	ZO
CMPR A, r	Complement r, A <- r ^ FF	1	ZO
ORAR r, A	Inclusive OR r with A, r <- r | A	1	ZO
ORAR A, r	Inclusive OR A with r, A <- A | r	1	ZO
ORIA i	Inclusive OR i with A, A <- A | i	1	ZO
XORAR r, A	Exclusive OR r with A, r <- r ^ A	1	ZO
XORAR A, r	Exclusive OR A with r, A <- A ^ r	1	ZO
XORIA i	Exclusive OR i with A, A <- A ^ i	1	ZO
Bit-wise Operations			
BCR r, b	Bit clear r, r.b <- 0	1	
BSR r, b	Bit set r, r.b <- 1	1	
BTRSC r, b	Bit test r, skip if (r.b = 0)	1 or 2	
BTRSS r, b	Bit test r, skip if (r.b =1)	1 or 2	
Data Movement Operations			
MOV r, A	Move A into r, r <- A	1	
MOV A, r	Move r into A, A <- r	1	ZO
MOVIA i	Move i into A, A <- i	1	
Shift Operations			
SWAPR r	Swap high and low nibbles in r, result put into r	1	
SWAPR A, r	Swap high and low nibbles in r, result put into A	1	
RLR r	Rotate r left through C, (C, r) <- (r, C)	1	CA
RLR A, r	Rotate r left through C, (C, A) <- (r, C)	1	CA
RRR r	Rotate r right through C, (r, C) <- (C, r)	1	CA
RRR A, r	Rotate r right through C, (A, C) <- (C, r)	1	CA
Control Transfer Operations			
CALL i	Call subroutine	2	
JUMP i	Jump to address	2	
RETIA	Return and load i to A	2	
RETI	Return from timer interrupt	2	
RET	Return from subroutine	2	

5. FIRMWARE PROGRAMMING GUIDE

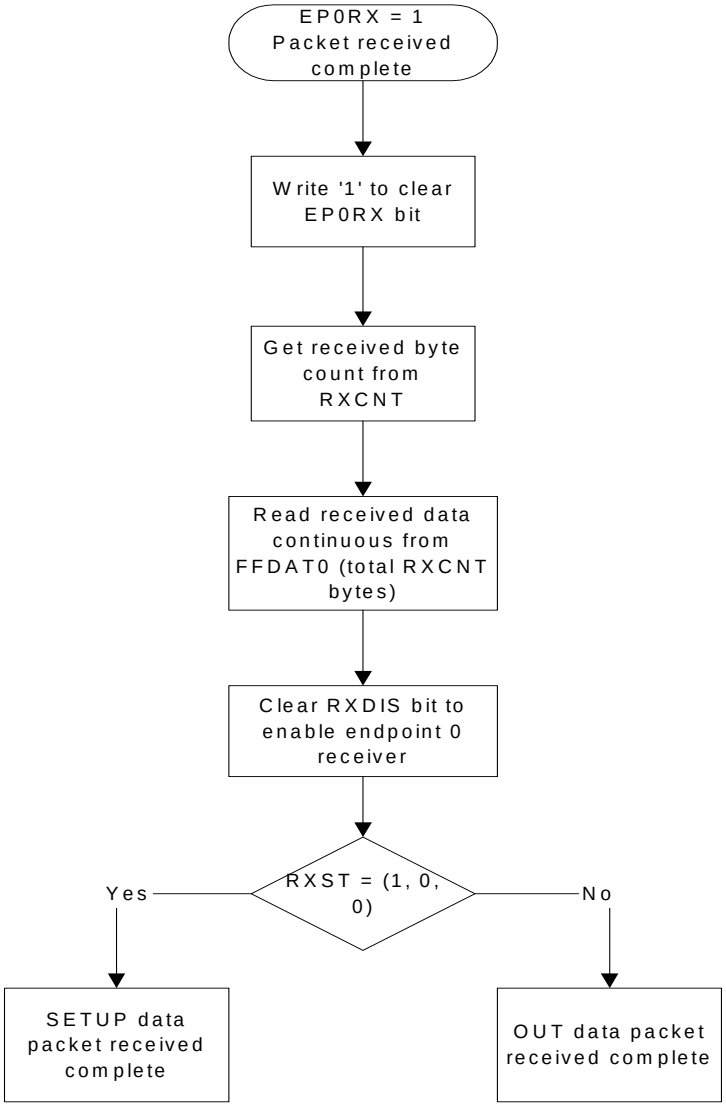
5.1 USB Power On Reset and Bus Reset Initialization



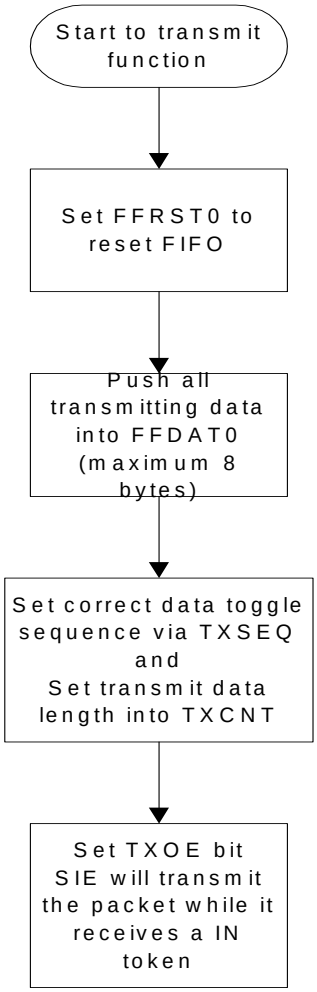
5.2 Suspend/Resume/Wakeup



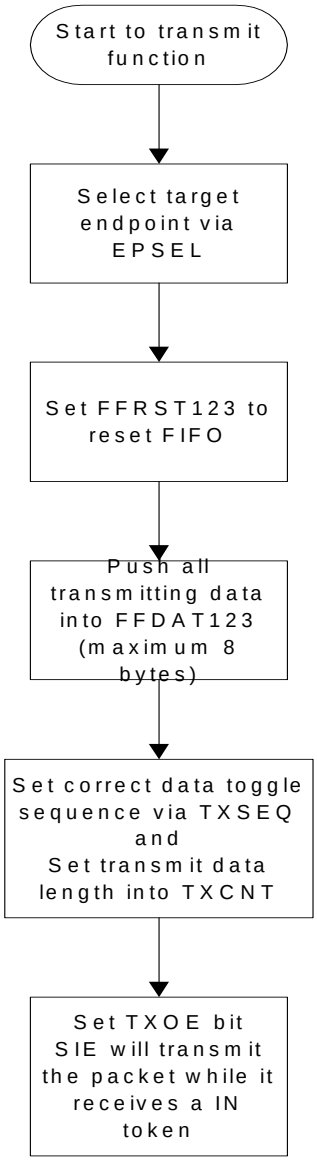
5.3 Receive Packet via Endpoint 0



5.4 Transmit Packet via Endpoint 0



5.5 Transmit Packet via Endpoint 1/2/3



5.6 Timer Interrupt

Because CPU may enter timer interrupt routine at any time, the timer interrupt routine should backup all special registers at its entry point and restore them before return.

```
(Address 0x004)
TIMER_ENTRY:  MOV       A_TEMP, A
              SWAPR     A, STATUS
              BCR       STATUS, BS
              MOV       S_TEMP, A
              MOV       A, INDAR
              MOV       I_TEMP, A
;
; Execute interrupt service routine
;
              MOV       A, I_TEMP
              MOV       INDAR, A
              SWAPR     A, S_TEMP
              MOV       STATUS, A
              SWAPR     A_TEMP
              SWAPR     A, A_TEMP
              BCR       INTEN, TMROF
              RETI
```

5.7 Conditional Branch

Example: Conditional branch can be according to value of Accumulator. Firmware can use this method to return value for lookahead table. Because Accumulator is only 8 bits wide, the higher 5 bits of Program Counter should be load into PCHBUF before the conditional branch executed.

```
(Address 0x540)
LOOKAHEAD:    MOVIA     0x05
              MOV       PCHBUF, A
              MOVIA     LOOKAHEAD_VAL
              ADDAR     PCL, A
              RETIA     0           ; Acc = 0
              RETIA     1           ; Acc = 1
              RETIA     2           ; Acc = 2
              .         .
              .         .
              .         .
```

5.8 Change Register Bank

Usually keeps BS = 0. If firmware want to access register address 0x80 to 0x8F, set BS = 1. After process register address 0x80 to 0x8F complete, clear BS = 0 to address 0x00 to 0x7F.

```
              BSR       STATUS, BS
              MOV       PORT1CON, A
              BCR       STATUS, BS
```

5.9 Change Code Bank

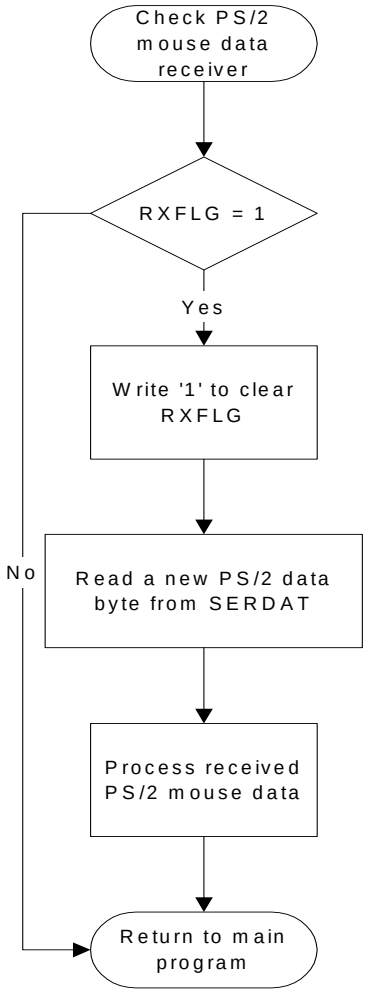
Because PCL is only 11 bits wide, Program Counter can only jump in 2K boundary directly. If Program Counter want to jump over 2K boundary, firmware should set PCHBUF to correct bank first.

(Address 0x375)

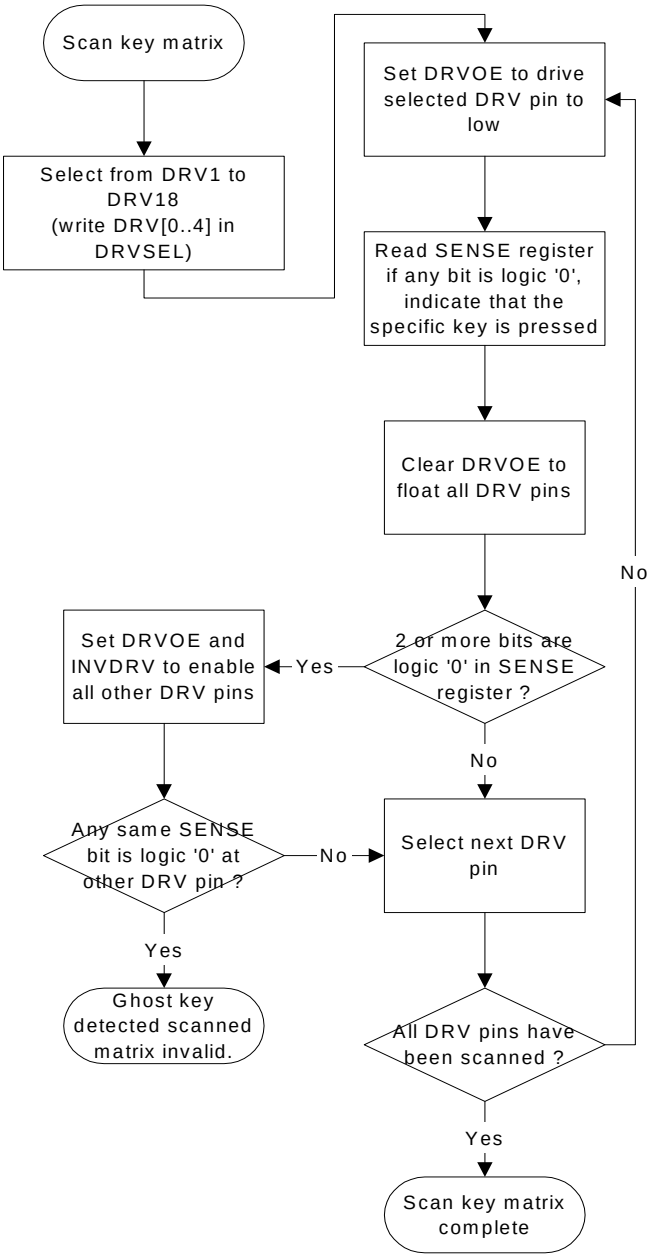
```
MOVIA     0x08
MOV       PCHBUF, A
JUMP      DEST_ADDR
```

(Address 0x83A)
DEST_ADDR:

5.10 Receive Data from PS/2 Mouse Port



5.11 Scan Key Matrix



5.12 Turn LED On/Off

To turn LEDs on, the firmware should set corresponding I/O pins (Port 1.5~Port 1.7) to output low. An external resistor should be added on every LED pins to limit sink current. To turn LEDs off, the firmware should output high to corresponding I/O pins (Port 1.5~Port 1.7).

6. ABSOLUTE MAXIMUM RATINGS

Maximum ratings are the extreme limits to which the micro-controller can be exposed without permanently damaging it. The micro-controller contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table. Keep V_{IN} and V_{OUT} within the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Connect unused inputs to the appropriate voltage level, either GND or V_{DD}.

Symbol	Characteristic	Value	Unit
T_{STG}	Storage temperature	-55 to +150	°C
T_{OP}	Operating temperature	0 to +70	°C
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	DC input voltage	-0.5 to +V_{CC} + 0.5	V
I	Maximum current per pin excluding V_{DD} and V_{SS}	25	mA
I_{MGND}	Maximum current out of GND	100	mA
I_{MVCC}	Maximum current out of V_{CC}	100	mA
V_{ESD}	Static discharge voltage	>4000	V

7. ELECTRICAL CHARACTERISTICS

F_{OSC} = 6MHz; Operating Temperature = 0 to 85°C; V_{CC} = 4.4 to 5.5V

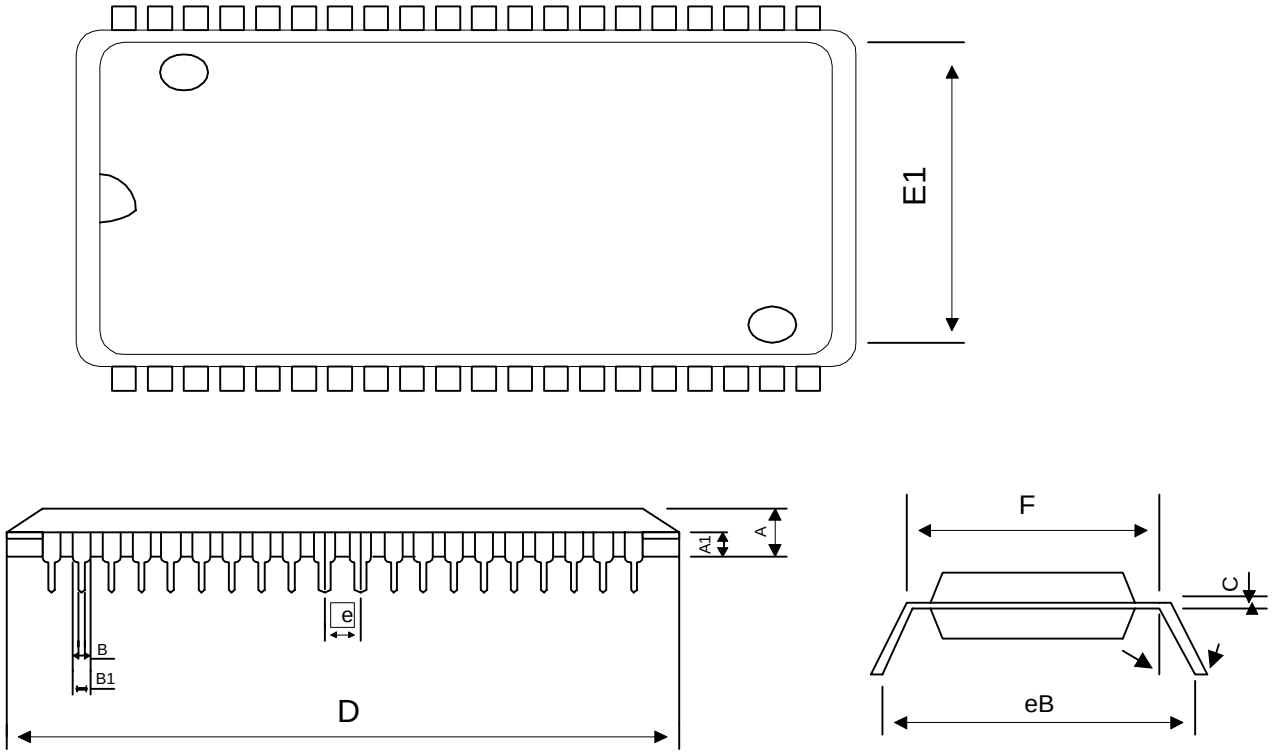
Symbol	Characteristic	Min	Max	Units	Conditions
	General				
I_{CC}	Operating supply current		10	mA	
I_{SB}	Supply current – suspend mode		360	µA	See note 1
	USB Interface				
V_{OH}	Static output high	2.8	3.6	V	R_L of 15KΩ to GND
V_{OL}	Static output low		0.3	V	R_L of 1.5KΩ to V3.3
V_{DI}	Differential input sensitivity	0.2		V	|(D+) – (D-)|
V_{CM}	Differential common mode range	0.8	2.5	V	Include V_{DI} range
V_{SE}	Single ended receiver threshold	0.8	2.0	V	
I_{LO}	Hi-Z state data line leakage	-10	+10	V	0V < V_{IN} < 3.3V
V3.3	Regulator supply voltage	3.0	3.6	V	I_L = 4mA
	GPIO Interface				
V_{OH1}	Static output high for PORT1.1-4	2.4		V	V_{CC} = 5V; I_{OH} = 4mA
V_{OL1}	Static output low for PORT1.1-4		0.4	V	V_{CC} = 5V; I_{OL} = 4mA
V_{OH2}	Static output high for PORT1.5-7	2.4		V	V_{CC} = 5V; I_{OH} = 20mA
V_{OL2}	Static output low for PORT1.5-7		0.4	V	V_{CC} = 5V; I_{OL} = 20mA
V_{IH}	Static input high	2.0		V	V_{CC} = 5V
V_{IL}	Static input low		0.9	V	V_{CC} = 5V
I_{SINK1}	Sink current for PORT1.1-4	4		mA	V_{OUT} = 0.4V;
I_{SINK2}	Sink current for PORT1.5-7	20		mA	V_{OUT} = 0.4V;
I_{IN}	Input leakage current	-1	+1	µA	V_{OUT} = 0V or V_{CC}
	USB Low-speed Source				
f_{OP}	Internal operating	1.5	1.5	MHz	

	frequency				
	Transition time				
t_R	Rise time	75		ns	C_L = 50pF
			300	ns	C_L = 350pF
t_F	Fall time	75		ns	C_L = 50pF
			300	ns	C_L = 350pF
t_{RFM}	Rise/Fall time matching	80	120	%	t_R / t_F
V_{CRS}	Output signal crossover voltage	1.3	2.0	V	
t_{DRATE}	Low speed data rate	1.4775 676.8	1.5225 666.0	Mbs ns	1.5Mbs ± 1.5%
	Source differential driver jitter				
t_{UDJ1}	To next transition	-25	25	ns	C_L = 350pF measured at crossover point
t_{UDJ2}	For paired transition	-10	10	ns	
	Receiver data jitter tolerance				
t_{DJR1}	To next transition	-75	75	ns	C_L = 350pF measured at crossover point
t_{DJR2}	For paired transition	-45	45	ns	
t_{EOPT}	Source EOP width	1.25	1.50	μs	Measured at crossover point
t_{DEOP}	Differential to EOP transition skew	-40	100	ns	Measured at crossover point
	Receiver EOP width				
t_{EOPR1}	Must reject as EOP	330		ns	Measured at crossover point
t_{EOPR2}	Must accept	675		ns	

Notes:
1. I_{SB} measured with USB in suspend mode; using external square wave clock source (F_{OSC} = 6MHz); transceiver pull-up resistor of 1.5KΩ between V3.3 and D- and 15KΩ termination resistors on D+ and D- pins; no port pins sourcing current. The I_{SB} value is including power consumed by external resistors.

8. PACKAGE DIAGRAMS

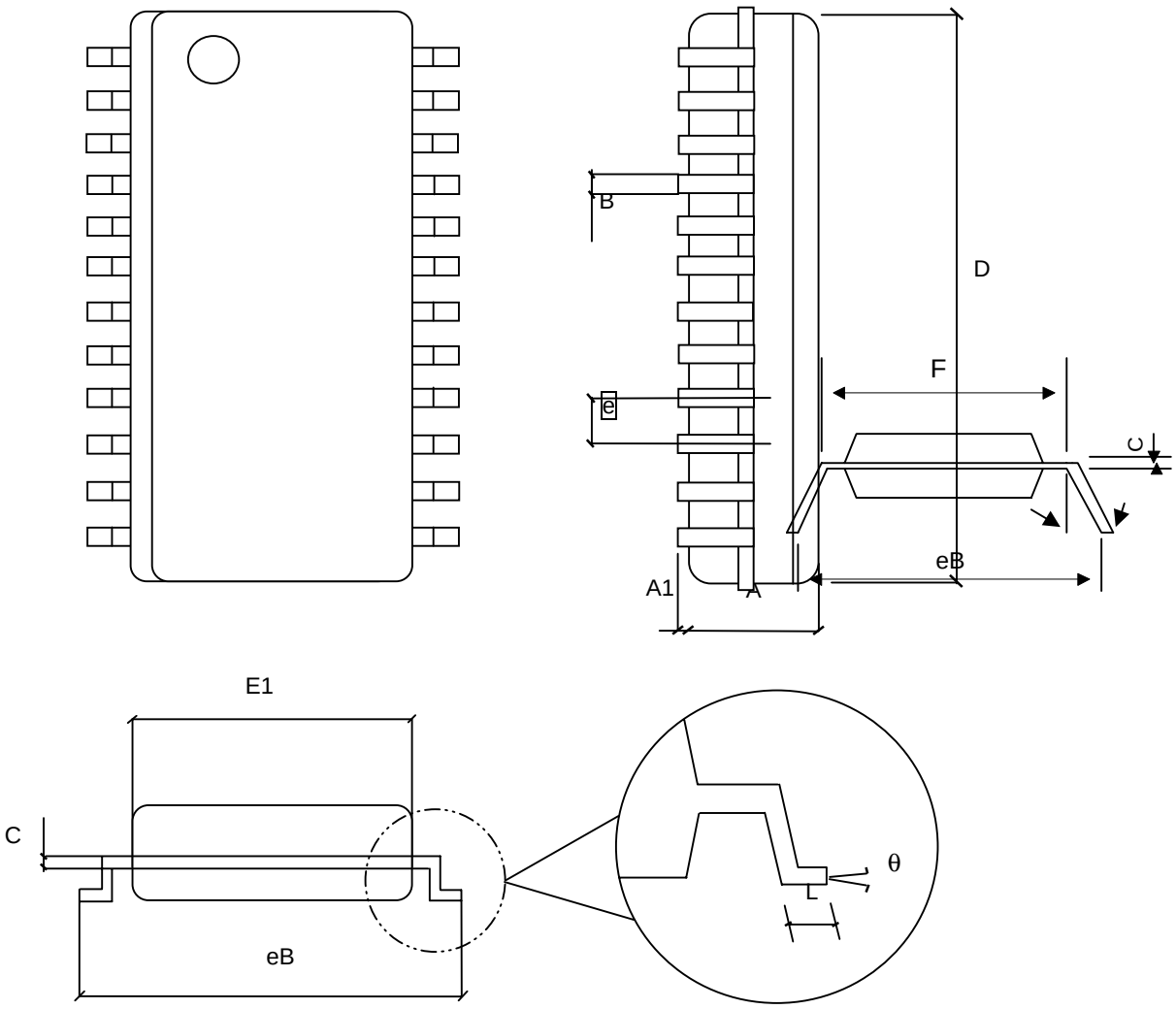
8.1 40-pin P-DIP



Symbol	Dimension in mil			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	*160*	--	--	*4.064*	--
A1	*74*	*75*	*76*	*1.880*	*1.905*	*1.930*
B	--	*18*	--	--	*0.457*	--
B1	--	*50*	--	--	*1.270*	--
C	--	*10*	--	--	*0.254*	--
D	*2040*	*2050*	*2060*	*51.816*	*52.07*	*52.324*
E1	*549*	*550*	*551*	*13.945*	*13.970*	*13.995*
F	*590*	*600*	*610*	*14.986*	*15.240*	*15.494*
e	--	*100*	--	--	*2.540*	--
eB	*640*	*650*	*660*	*16.256*	*16.510*	*16.764*
θ	*0°*	*7.5°*	*15°*	*0°*	*7.5°*	*15°*

Figure 7-3 Package outline dimension for 40-pin P-DIP

8.2 24-pin SOP



Symbol	Dimension in mils			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	98	100	102	2.489	2.540	2.591
A1	6	---	---	0.152	---	---
A2	39	41	43	0.991	1.041	1.092
B	---	16	---	---	0.406	---
C	---	10	---	---	0.254	---
D	598	600	602	15.189	15.240	15.291
E1	298	300	302	7.569	7.620	7.671
e	---	50	---	---	1.270	---
eB	406	410	414	10.312	10.414	10.516
L	30	32	34	0.762	0.813	0.864
θ	---	5°	---	---	5°	---

Figure 7-4 Package outline dimension for 24-pin SOP