BLF6G22L-40P; BLF6G22LS-40P

Power LDMOS transistor

Rev. 1 — 22 September 2011 Product data sheet

1. Product profile

1.1 General description

LDMOS power transistor for base station applications at frequencies from 2110 MHz to 2170 MHz and 1805 MHz to 1880 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a common source class-AB production test circuit.

Mode of operation	f (MHz)	I_{Dq} (mA)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR (dBc)
2-carrier W-CDMA	2110 to 2170	410	28	13.5	19	30	–30 [2]
	1805 to 1880 [1]	410	28	5	20.3	18.3	–34.9 [2]
1-carrier W-CDMA	2110 to 2170	410	28	15	19	32	–37 [3]
	1805 to 1880 [1]	410	28	5	20.5	18.0	–42.3 [3]

[1] The performance is tested on the Class AB demo board as depicted in Figure 11.

[2] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF; carrier spacing 5 MHz.

[3] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

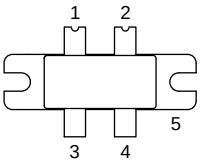
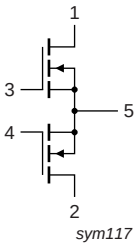
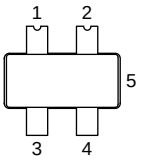
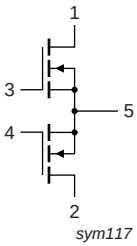
- Excellent ruggedness
- High efficiency
- Low R_{th} providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifier for base stations and multi carrier applications in the 2110 MHz to 2170 MHz frequency band
- RF driver amplifier in the 1805 MHz to 1880 MHz frequency band

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
BLF6G22L-40P (SOT1121A)				
1	drain1			
2	drain2			
3	gate1			
4	gate2			
5	source	[1]		
BLF6G22LS-40P (SOT1121B)				
1	drain1			
2	drain2			
3	gate1			
4	gate2			
5	source	[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF6G22L-40P	-	flanged LDMOST ceramic package; 2 mounting holes; 4 leads	SOT1121A
BLF6G22LS-40P	-	earless flanged LDMOST ceramic package; 4 leads	SOT1121B

4. Limiting values

Table 4. Limiting values (2 sections combined)

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
I_D	drain current		-	16	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 40 W	0.7	K/W

6. Characteristics

Table 6. Characteristics (per section)

T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.4 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 40 mA	1.4	1.9	2.4	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	2	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	6	7	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	200	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 2.0 A	1.8	2.9	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 1.4 A	0.14	0.37	0.57	Ω

7. Application information

Table 7. Application information (2 sections combined)

Mode of operation: 2-carrier W-CDMA; PAR 8.4 dB at 0.01 % probability on CCDF; 3GPP test model 1; 64 DPCH; f_1 = 2112.5 MHz; f_2 = 2117.5 MHz; f_3 = 2162.5 MHz; f_4 = 2167.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 410 mA; T_{case} = 25 °C; in a class-AB production test circuit.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 13.5 W	[1]	17.8	19	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 13.5 W	[1]	-	–15	–9	dB
η_D	drain efficiency	$P_{L(AV)}$ = 13.5 W	[1]	26.5	30	-	%
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	$P_{L(AV)}$ = 13.5 W	[1]	-	–30	–27	dBc
$ACPR_{10M}$	adjacent channel power ratio (10 MHz)	$P_{L(AV)}$ = 13.5 W	[1]	-	–39	–36	dBc

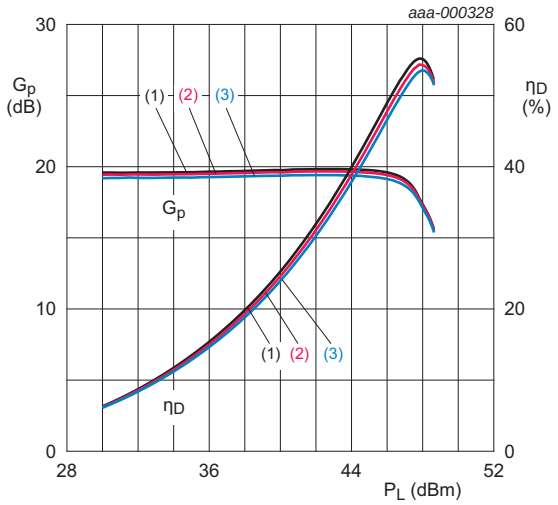
[1] In production, all testing are only performed at 2110 MHz to 2170 MHz frequency band.

7.1 Ruggedness in class-AB operation

The BLF6G22L-40P and BLF6G22LS-40P are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 410 mA; P_L = 40 W (CW); f = 2110 MHz.

The BLF6G22L-40P and BLF6G22LS-40P are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 410 mA; P_L = 40 W (CW pulse, 10 %); f = 1842 MHz.

7.2 CW



V_{DS} = 28 V; I_{Dq} = 410 mA.

(1) f = 2110 MHz

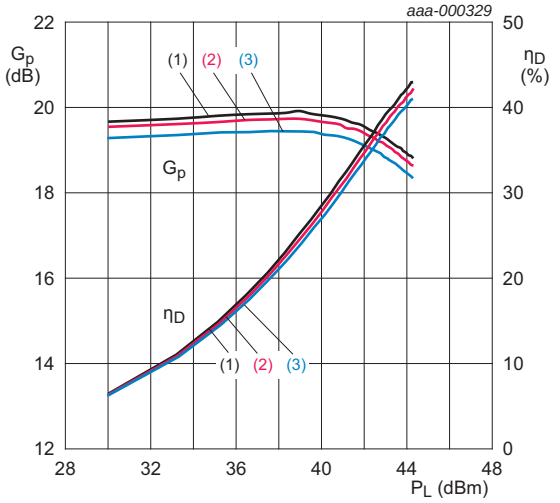
(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 1. Power gain and drain efficiency as function of load power; typical values

7.3 IS-95

Single carrier IS-95; PAR = 9.7 dB at 0.01 % probability on the CCDF.



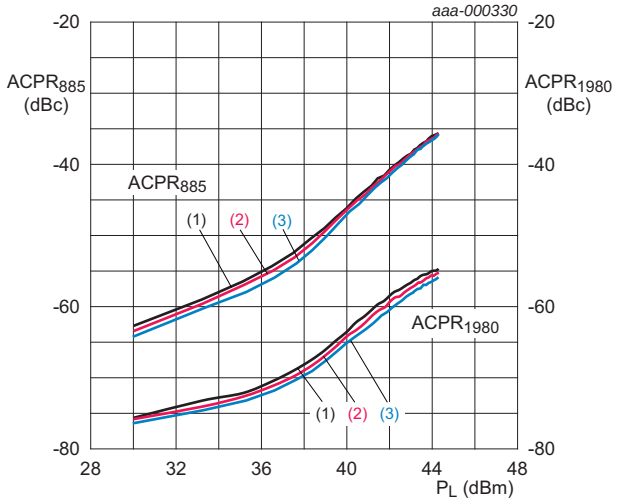
V_{DS} = 28 V; I_{Dq} = 410 mA.

(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 2. Single carrier IS-95 power gain and drain efficiency as function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 410 mA.

(1) f = 2110 MHz

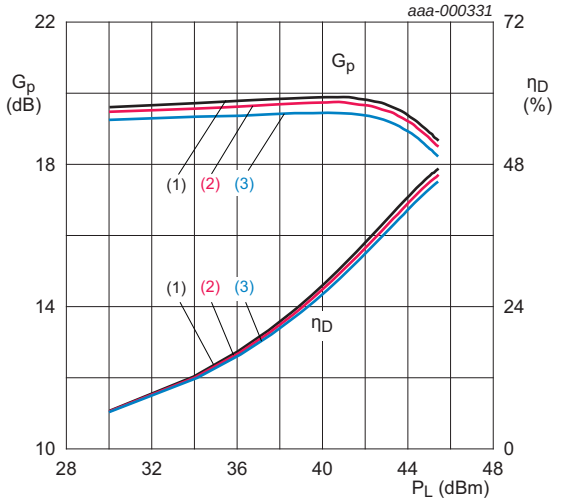
(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 3. Single carrier IS-95 adjacent channel power ratio as a function of output power; typical values

7.4 1-carrier W-CDMA

Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.



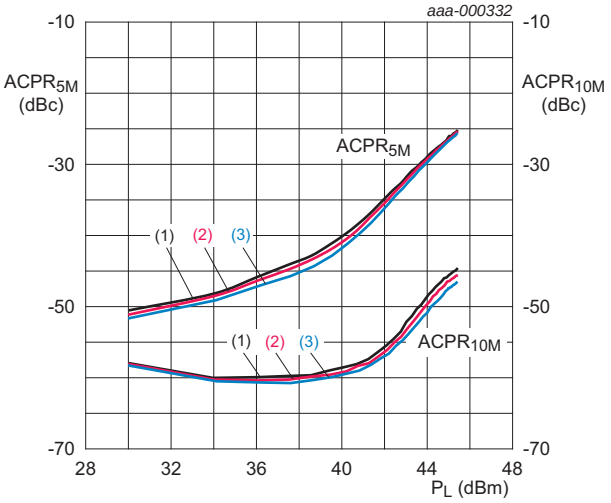
V_{DS} = 28 V; I_{Dq} = 410 mA.

(1) f = 2112.5 MHz

(2) f = 2140 MHz

(3) f = 2167.5 MHz

Fig 4. 1-carrier W-CDMA power gain and drain efficiency as function of output power; typical values



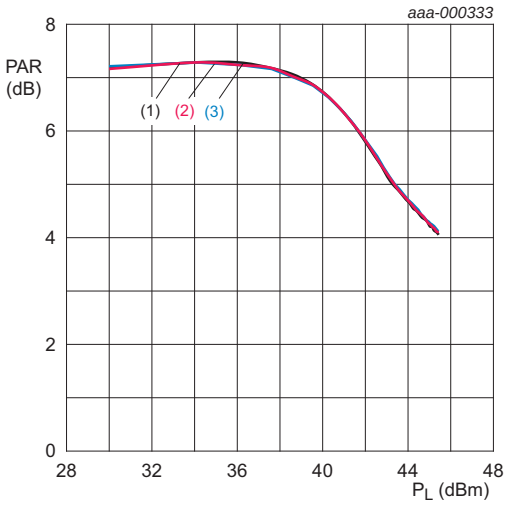
V_{DS} = 28 V; I_{Dq} = 410 mA.

(1) f = 2112.5 MHz

(2) f = 2140 MHz

(3) f = 2167.5 MHz

Fig 5. 1-carrier W-CDMA adjacent channel power ratio as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 410 mA.

(1) f = 2112.5 MHz

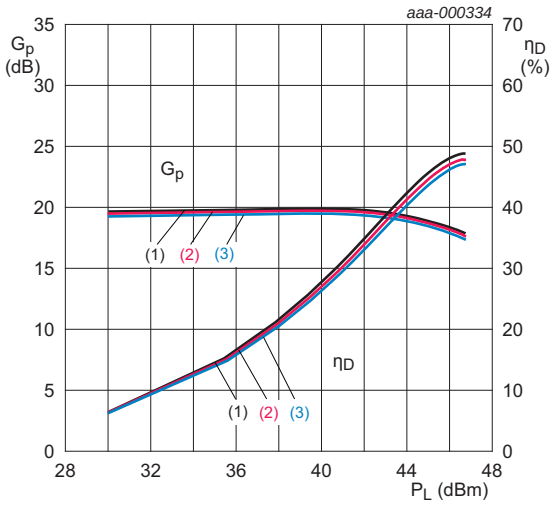
(2) f = 2140 MHz

(3) f = 2167.5 MHz

Fig 6. 1-carrier W-CDMA power gain and drain efficiency as function of output power; typical values

7.5 2-carrier W-CDMA

Test signal: 3GPP; test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF; carrier spacing 5 MHz.



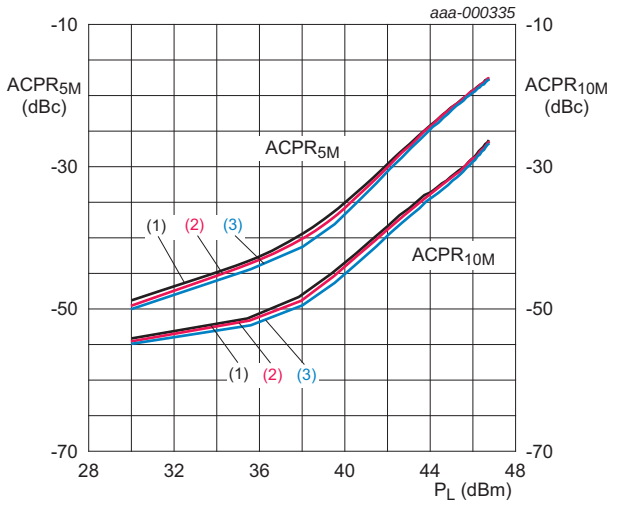
V_{DS} = 28 V; I_{Dq} = 410 mA.

(1) f = 2115 MHz

(2) f = 2140 MHz

(3) f = 2165 MHz

Fig 7. 2-carrier W-CDMA power gain and drain efficiency as function of output power; typical values



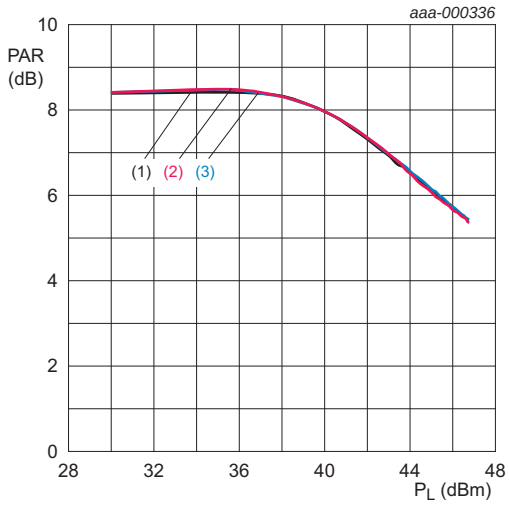
V_{DS} = 28 V; I_{Dq} = 410 mA.

(1) f = 2115 MHz

(2) f = 2140 MHz

(3) f = 2165 MHz

Fig 8. 2-carrier W-CDMA adjacent channel power ratio as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 410 mA.

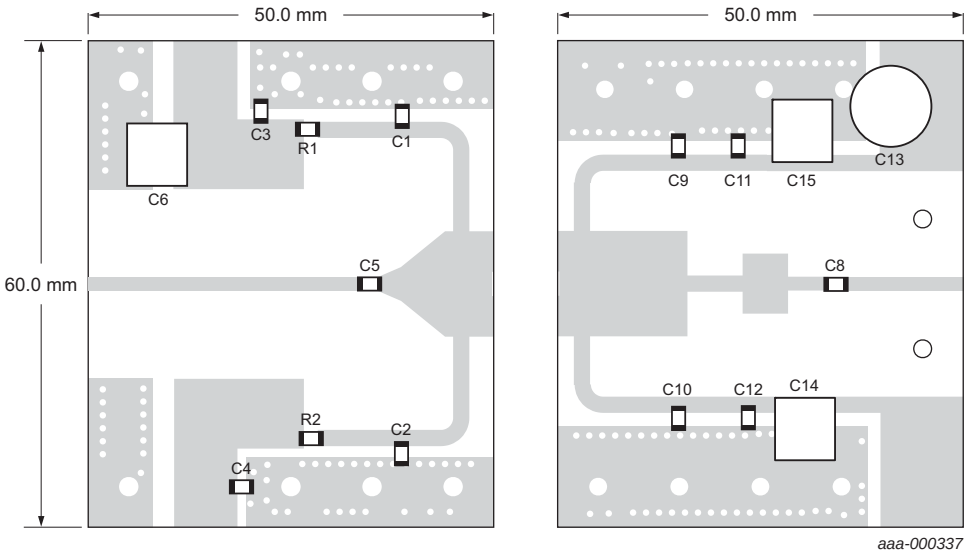
(1) f = 2115 MHz

(2) f = 2140 MHz

(3) f = 2165 MHz

Fig 9. 2-carrier W-CDMA peak-to-average power ratio as function of output power; typical values

8. Test information



Printed-Circuit Board (PCB): Rogers RO4350; ε_r = 3.5 F/m; thickness = 0.762 mm; thickness copper plating = 35 μm.

The vias can be as a reference to place components.

The above layout shows the test circuit used to measure the devices in production. A more appropriate application demonstration for specific customer needs can be provided.

See Table 8 for list of components.

Fig 10. Component layout

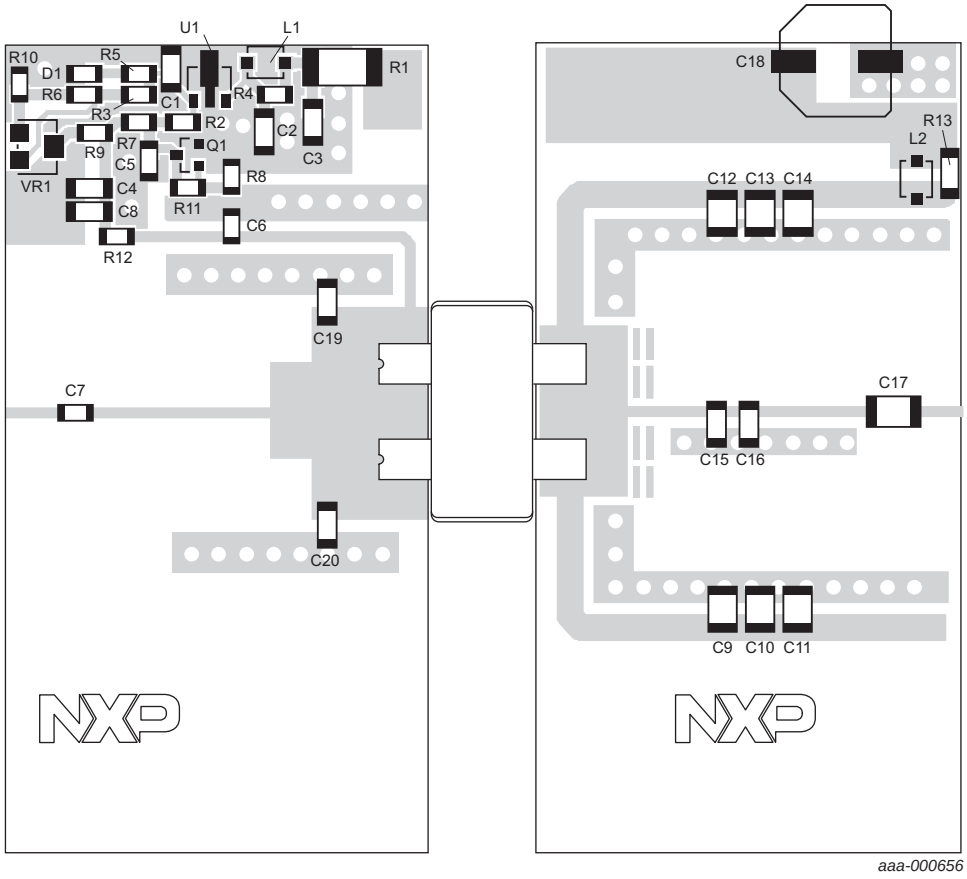
Table 8. List of components

See Figure 10 for component layout.

Component	Description	Value		Remarks
C1, C2, C9, C10	multilayer ceramic chip capacitor	68 pF	[1]	
C3, C4, C11, C12	multilayer ceramic chip capacitor	820 pF	[2]	
C5, C8	multilayer ceramic chip capacitor	4.7 pF	[1]	
C6, C14, C15	multilayer ceramic chip capacitor	10 μF		TDK
C13	electrolytic capacitor	470 μF; 63 V		
R1, R2	chip resistor	12 Ω		Philips 1206

[1] American Technical Ceramics type 800B or capacitor of same quality.

[2] American Technical Ceramics type 100A or capacitor of same quality.



Printed-Circuit Board (PCB): Rogers RO4350; ε_r = 3.5 F/m; thickness = 0.762 mm; thickness copper plating = 35 μm.

The vias can be as a reference to place components.

The above layout shows the test circuit used to measure the devices in production. A more appropriate application demonstration for specific customer needs can be provided.

See Table 9 for list of components.

Fig 11. 1.8 GHz Demo board layout

Table 9. List of components

See Figure 11 for component layout.

Component	Description	Value	Remarks
C1, C2, C5, C8	multilayer ceramic chip capacitor	100 nF	Murata
C3, C4, C11, C14	multilayer ceramic chip capacitor	1 μF	Murata
C6	multilayer ceramic chip capacitor	47 pF	ATC
C7	multilayer ceramic chip capacitor	10 pF	ATC
C9, C12	multilayer ceramic chip capacitor	12 pF	ATC
C10, C13	multilayer ceramic chip capacitor	330 pF	Murata
C15, C16	multilayer ceramic chip capacitor	1.5 pF	ATC
C17	multilayer ceramic chip capacitor	10 pF	ATC
C18	electrolytic capacitor	2200 μF, 50 V	Panasonic
C19, C20	multilayer ceramic chip capacitor	1 pF	ATC

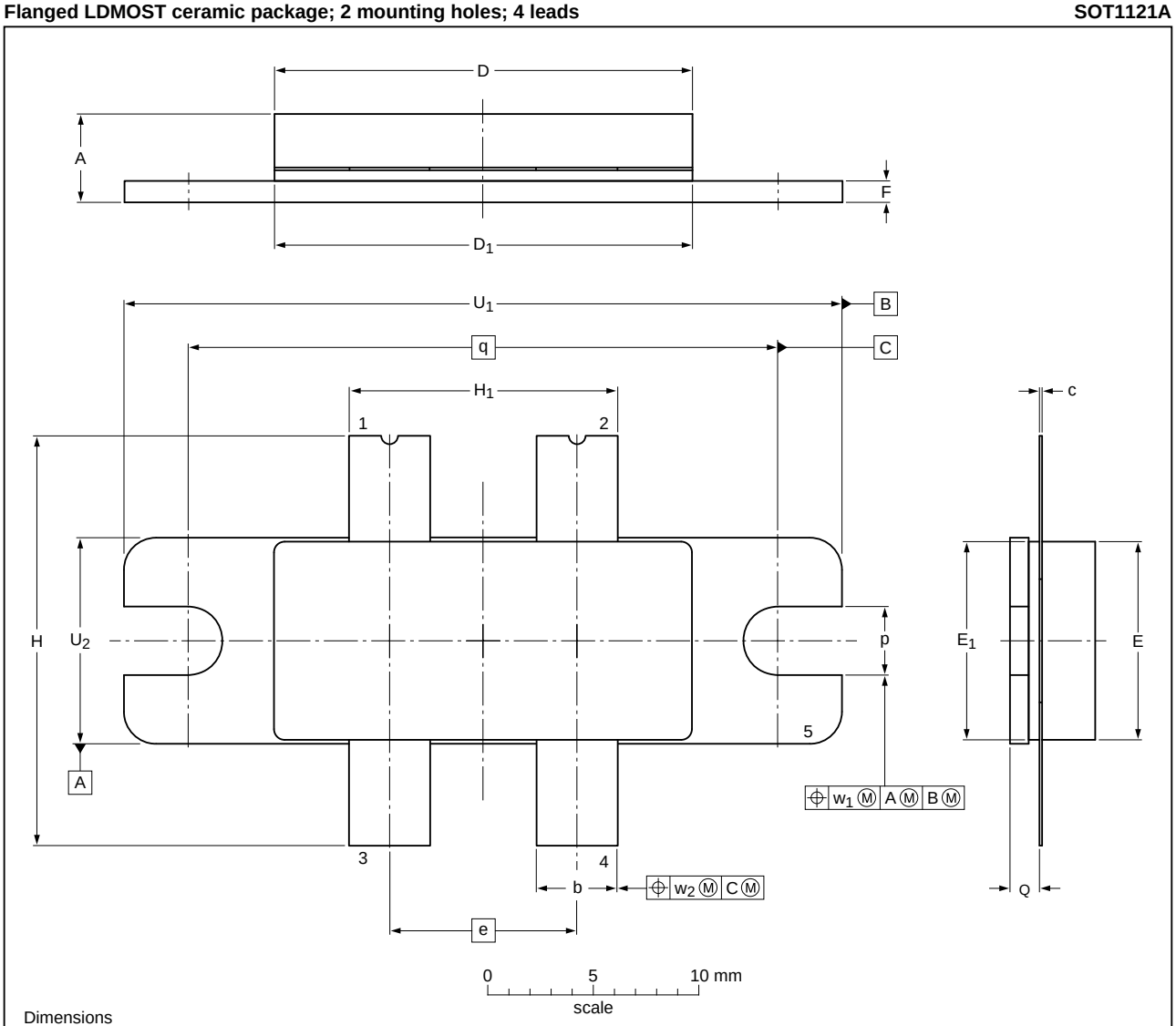
Table 9. List of components

See Figure 11 for component layout.

Component	Description	Value	Remarks
L1, L2	ferrite bead	5 A	Fair Rite
R1	chip resistor	500 Ω	Vishay Dale
R2, R5	chip resistor	1.1 kΩ	Vishay Dale
R3, R6	chip resistor	432 Ω	Vishay Dale
R4, R11	chip resistor	9.1 Ω	Vishay Dale
R9	chip resistor	2 kΩ	Vishay Dale
R10	chip resistor	75 Ω	Vishay Dale
R12	chip resistor	1.5 Ω	Vishay Dale
VR1	potentiometer	200 Ω	Bourns
U1	voltage regulator		NJR

9. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 4 leads **SOT1121A**



Dimensions

Unit[1]		A	b	c	D	D1	e	E	E1	F	H	H1	p	Q[2]	q	U1	U2	w1	w2
mm	max	4.75	3.94	0.18	20.02	19.96		9.53	9.53	1.14	19.94	12.83	3.38	1.70		34.16	9.91		
	nom						8.89								27.94			0.25	0.51
	min	3.45	3.68	0.10	19.61	19.66		9.27	9.27	0.89	18.92	12.57	3.12	1.45		33.91	9.65		
inches	max	0.187	0.155	0.007	0.788	0.786		0.375	0.375	0.045	0.785	0.505	0.133	0.067		1.345	0.39		
	nom						0.35								1.1			0.01	0.02
	min	0.136	0.145	0.004	0.772	0.774		0.365	0.365	0.035	0.745	0.495	0.123	0.057		1.335	0.38		

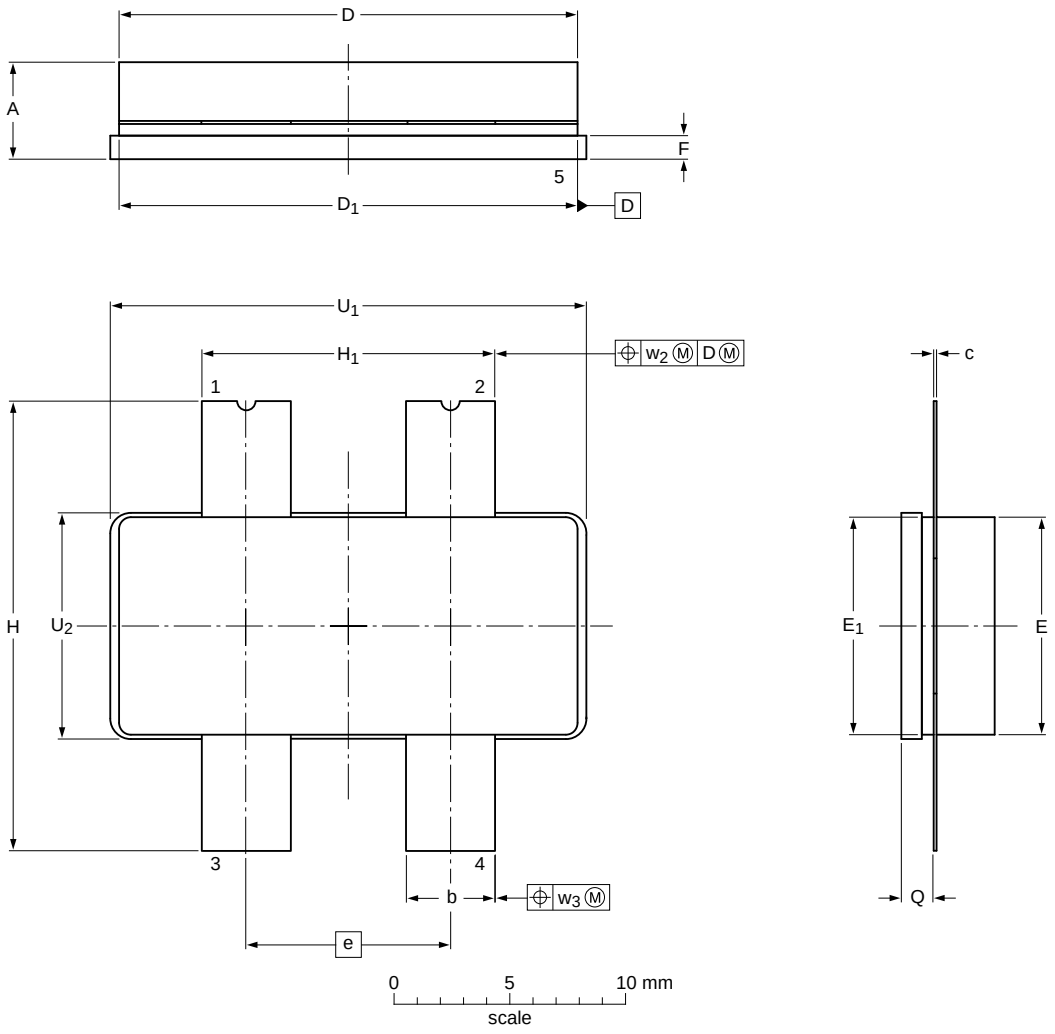
Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1121a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1121A						~~09-10-12~~ 10-02-02

Fig 12. Package outline SOT1121A

Earless flanged LDMOST ceramic package; 4 leads **SOT1121B**



Dimensions

Unit[1]		A	b	c	D	D_1	e	E	E_1	F	H	H_1	Q	U_1	U_2	w_2	w_3
mm	max	4.75	3.94	0.18	20.02	19.96		9.53	9.53	1.14	19.94	12.83	1.70	20.70	9.91		
	nom						8.89									0.51	0.25
	min	3.45	3.68	0.08	19.61	19.66		9.27	9.27	0.89	18.92	12.57	1.45	20.45	9.65		
inches	max	0.187	0.155	0.007	0.788	0.786		0.375	0.375	0.045	0.785	0.505	0.067	0.815	0.39		
	nom						0.35									0.02	0.01
	min	0.136	0.145	0.003	0.772	0.774		0.365	0.365	0.035	0.745	0.495	0.057	0.805	0.38		

Note

1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1121b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1121B						~~09-10-12~~ 09-12-14

Fig 13. Package outline SOT1121B

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
IS-95	Interim Standard 95
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
RF	Radio Frequency
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF6G22L-40P_6G22LS-40P v.1	20110922	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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13. Contact information

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For sales office addresses, please send an email to: **salesaddresses@nxp.com**

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