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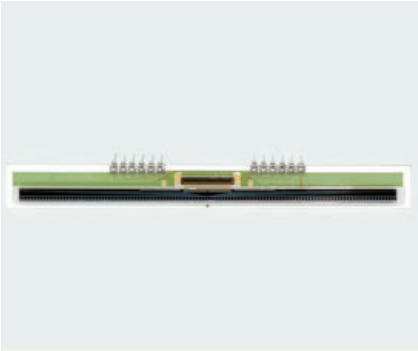
Photodiode arrays with amplifier



S8866-64/-128

Photodiode array combined with signal processing IC

The S8866-64 and S8866-128 are Si photodiode arrays combined with a signal processing IC chip. The signal processing IC chip is formed by CMOS process and incorporates a timing generator, shift register, charge amplifier array, clamp circuit and hold circuit, making the external circuit configuration simple. For X-ray detection applications, types (S8866-64G-02, S8866-128G-02) with phosphor sheet affixed on the photosensitive area are also available.

Features

- **Large element pitch: 2 types available**
  S8866-64: 1.6 mm pitch × 64 ch
  S8866-128: 0.8 mm pitch × 128 ch
- **5 V power supply operation**
- **Simultaneous integration by using a charge amplifier array**
- **Sequential readout with a shift register**
  (Data rate: 500 kHz max.)
- **Low dark current due to zero-bias photodiode operation**
- **Integrated clamp circuit allows low noise and wide dynamic range**
- **Integrated timing generator allows operation at two different pulse timings**

Applications

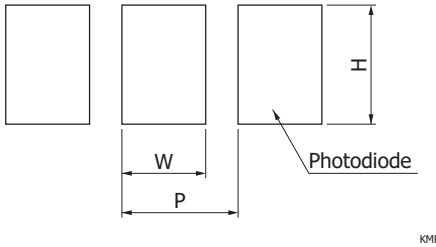
- **Long and narrow line sensors**

Structure

Parameter	Symbol*1	S8866-64	S8866-128	Unit
Element pitch	P	1.6	0.8	mm
Element diffusion width	W	1.5	0.7	mm
Element height	H	1.6	0.8	mm
Number of elements	-	64	128	-
Effective photosensitive area length	-	102.4	102.4	mm
Board material	-	Ceramic		-

*1: Refer to following figure.

Enlarged drawing of photosensitive area



KMPDC0072EA

Absolute maximum ratings

Parameter	Symbol	Value	Unit
Supply voltage	Vdd	-0.3 to +6	V
Reference voltage	Vref	-0.3 to +6	V
Photodiode voltage	Vpd	-0.3 to +6	V
Gain selection terminal voltage	Vgain	-0.3 to +6	V
Master/slave selection voltage	Vms	-0.3 to +6	V
Clock pulse voltage	V(CLK)	-0.3 to +6	V
Reset pulse voltage	V(RESET)	-0.3 to +6	V
External start pulse voltage	V(EXTSP)	-0.3 to +6	V
Operating temperature*2	Topr	-5 to +60	°C
Storage temperature	Tstg	-10 to +70	°C

*2: No condensation

Recommended terminal voltage

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Vdd	4.75	5	5.25	V
Reference voltage		Vref	4	4.5	4.6	V
Photodiode voltage		Vpd	-	Vref	-	V
Gain selection terminal voltage	High gain	Vgain	Vdd - 0.25	Vdd	Vdd + 0.25	V
	Low gain		0	-	0.4	V
Master/slave selection voltage	High level*3	Vms	Vdd - 0.25	Vdd	Vdd + 0.25	V
	Low level*4		0	-	0.4	V
Clock pulse voltage	High level	V(CLK)	3.3	Vdd	Vdd + 0.25	V
	Low level		0	-	0.4	V
Reset pulse voltage	High level	V(RESET)	3.3	Vdd	Vdd + 0.25	V
	Low level		0	-	0.4	V
External start pulse voltage	High level	V(EXTSP)	Vdd - 0.25	Vdd	Vdd + 0.25	V
	Low level		0	-	0.4	V

*3: Parallel
*4: Serial at 2nd or later stages

Electrical characteristics [Ta=25 °C, Vdd=5 V, V(CLK)=V(RESET)=5 V]

Parameter		Symbol	S8866-64			S8866-128			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock pulse frequency*5		f(CLK)	40	-	2000	40	-	2000	kHz
Line rate		LR	-	7800	-	-	3900	-	lines/s
Output impedance		Zo	-	3	-	-	3	-	kΩ
Power consumption		P	-	100	-	-	180	-	mW
Charge amp feedback capacitance	High gain	Cf	-	0.5	-	-	0.5	-	pF
	Low gain		-	1	-	-	1	-	

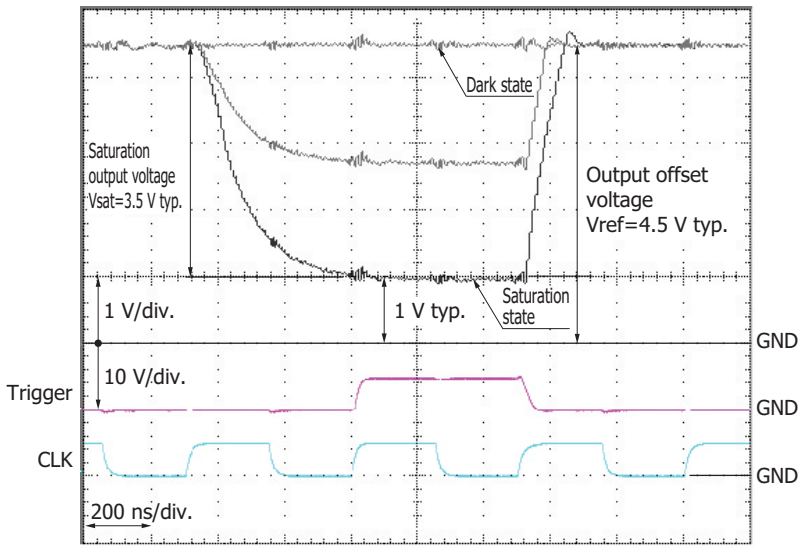
*5: Video data rate is 1/4 of clock pulse frequency f(CLK).

Electrical and optical characteristics [Ta=25 °C, Vdd=5 V, V (CLK)=V (RESET)=5 V, Vgain=5 V (High gain), 0 V (Low gain)]

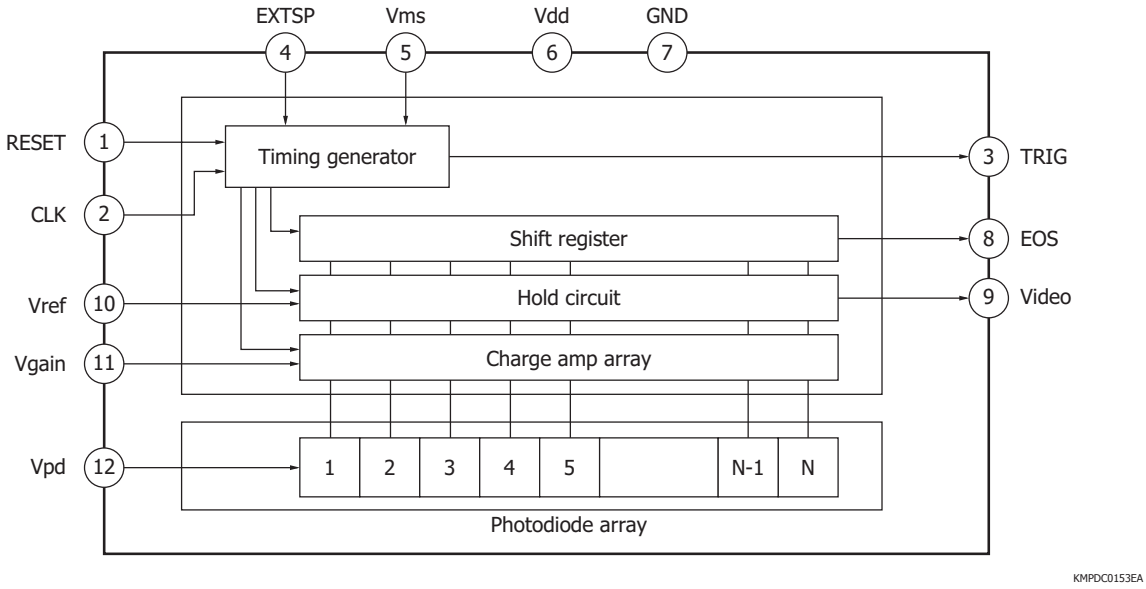
Parameter		Symbol	S8866-64			S8866-128			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Spectral response range		λ		300 to 1000			300 to 1000		nm
Peak sensitivity wavelength		λp	-	720	-	-	720	-	nm
Dark output voltage*6	High gain	Vd	-	0.01	0.2	-	0.01	0.2	mV
	Low gain		-	0.005	0.1	-	0.005	0.1	
Saturation output voltage		Vsat	3	3.5	-	3	3.5	-	V
Saturation exposure*7	High gain	Esat	-	0.2	0.25	-	0.8	1.0	m*lx* · s
	Low gain		-	0.4	0.5	-	1.6	2.0	
Photo sensitivity	High gain	S	14400	18000	-	3520	4400	-	V/*lx* · s
	Low gain		7200	9000	-	1760	2200	-	
Photo response non-uniformity*8		PRNU	-	-	±10	-	-	±10	%
Noise*9	High gain	N	-	2.0	3.0	-	1.3	2.0	mVrms
	Low gain		-	1.1	1.7	-	0.7	1.1	
Output offset voltage*10		Vos	-	Vref	-	-	Vref	-	V

*6: Integration time ts=1 ms
*7: Measured with a 2856 K tungsten lamp.
*8: When the photodiode array is exposed to uniform light which is 50% of the saturation exposure, the photo response non-uniformity (PRNU) is defined as follows:
PRNU = ΔX/X × 100 [%]
X: average output of all elements, ΔX: difference between X and the maximum or minimum output, whichever is larger.
*9: Measured with a video data rate of 50 kHz and ts=1 ms in dark state.
*10: Video output is negative-going output with respect to the output offset voltage.

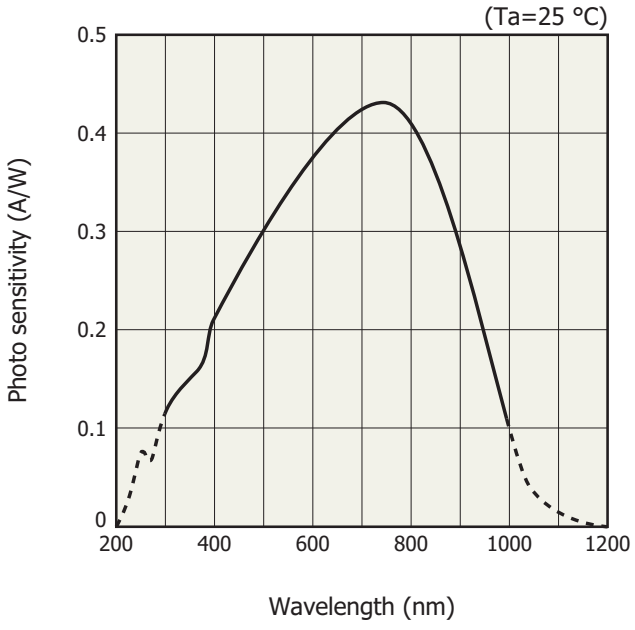
Output waveform of one element



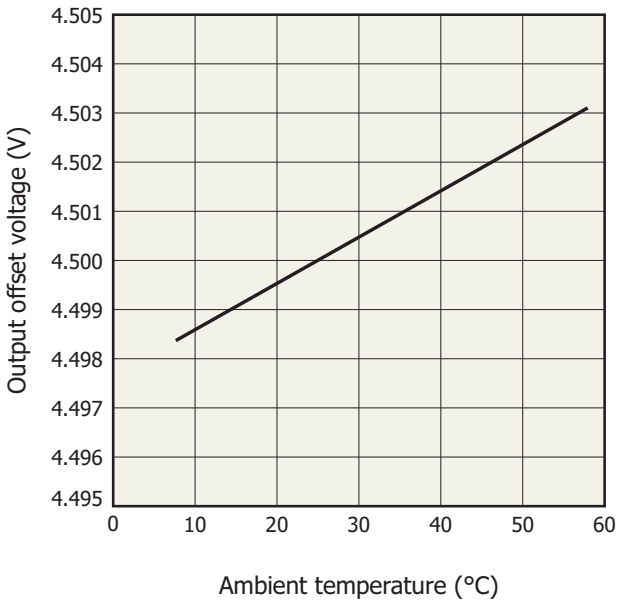
Block diagram



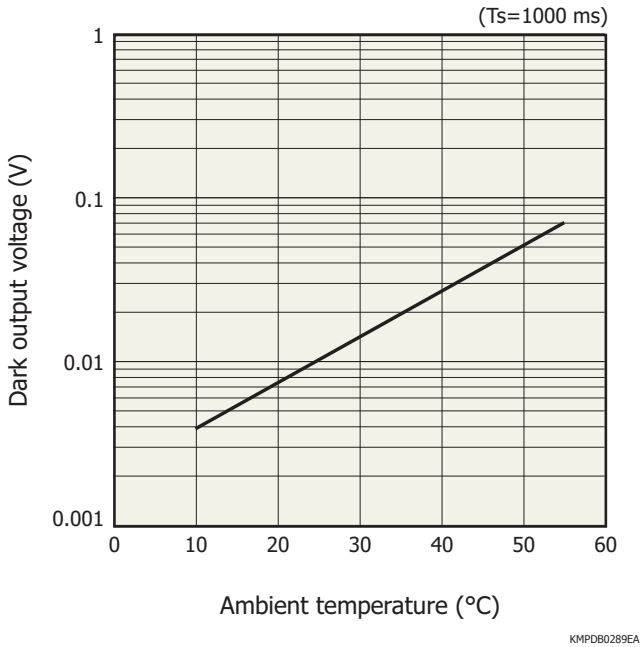
Spectral response (measurement example)



Output offset voltage vs. ambient temperature (measurement example)

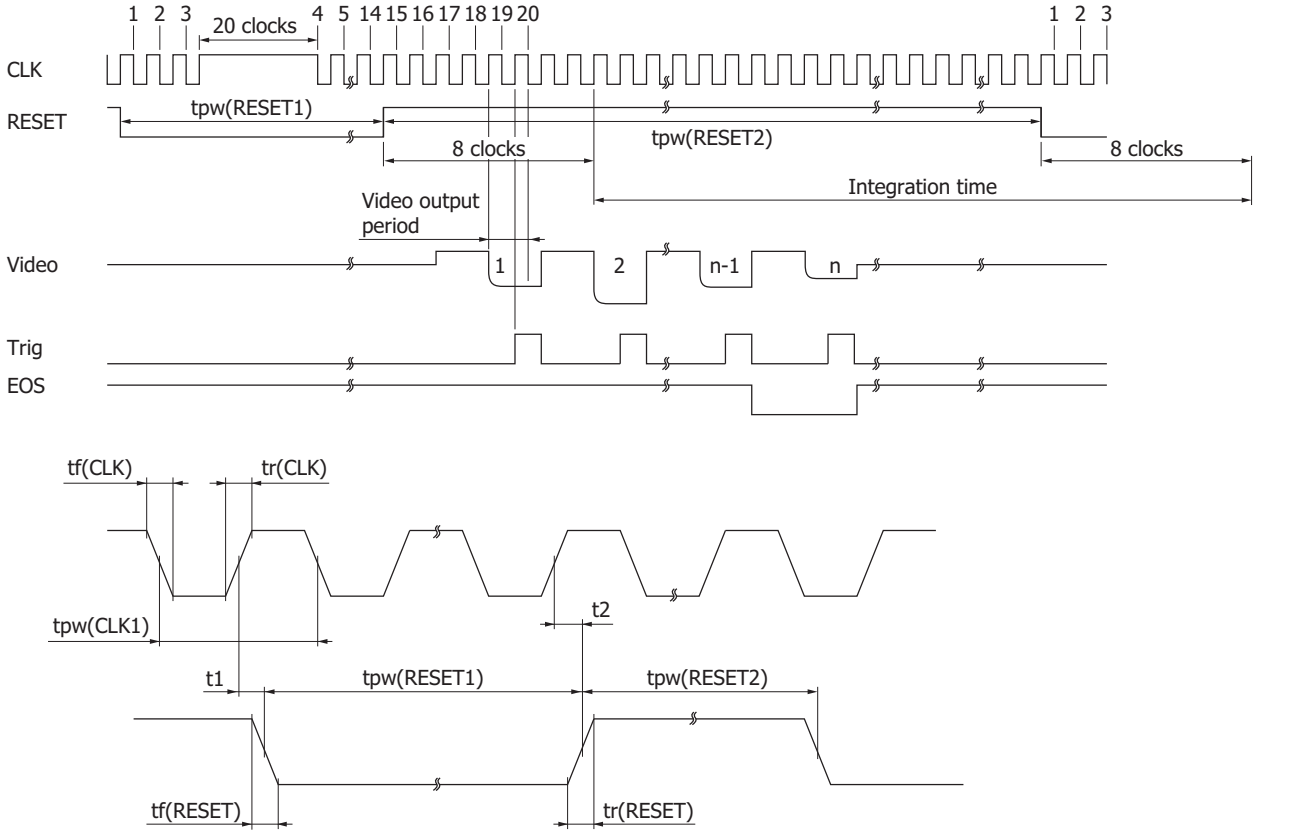


Dark output voltage vs. ambient temperature (measurement example)



Timing chart

S8866-64

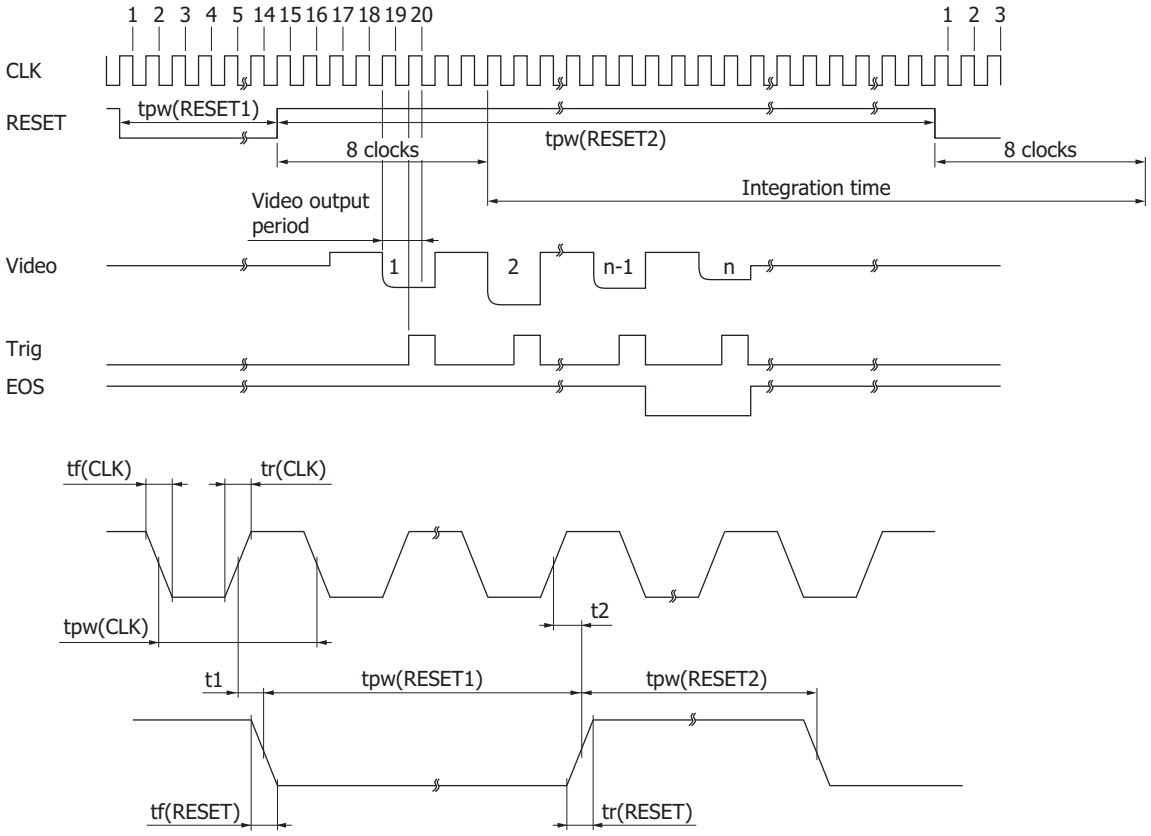


KMPDC0278EA

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse width	tpw(CLK)	500	-	25000	ns
Clock pulse rise/fall times	tr(CLK), tf(CLK)	0	20	30	ns
Reset pulse width 1	tpw(RESET1)	21	-	-	CLK
Reset pulse width 2	tpw(RESET2)	20	-	-	CLK
Reset pulse rise/fall times	tr(RESET), tf(RESET)	0	20	30	ns
Clock pulse-reset pulse timing 1	t1	-20	0	20	ns
Clock pulse-reset pulse timing 2	t2	-20	0	20	ns

1. The internal timing circuit starts operation at the falling edge of CLK immediately after a RESET pulse goes Low.
2. When the falling edge of each CLK is counted as "1 clock", the video signal of the 1st channel appears between "18.5 clocks and 20 clocks". Subsequent video signals appear every 4 clocks.
3. To obtain video signals, extend the High period 3 clocks from the falling edge of CLK immediately after the RESET pulse goes Low, to a 20 clock period.
4. The trigger pulse for the 1st channel rises at a timing of 19.5 clocks and then rises every 4 clocks. The rising edge of each trigger pulse is the recommended timing for data acquisition.
5. Signal charge integration time equals the High period of a RESET pulse. However, the charge integration does not start at the rise of a RESET pulse but starts at the 8th clock after the rise of the RESET pulse and ends at the 8th clock after the fall of the RESET pulse. After the RESET pulse next changes from High to Low, signals integrated within this period are sequentially read out as time-series signals by the shift register operation. The rise and fall of a RESET pulse must be synchronized with the rise of a CLK pulse, but the rise of a RESET pulse must be set outside the video output period. One cycle of RESET pulses cannot be set shorter than the time equal to "36.5 + 4 × N (number of elements)" clocks.
6. The video signal after an EOS signal output becomes a high impedance state, and the video output will be indefinite.

S8866-128

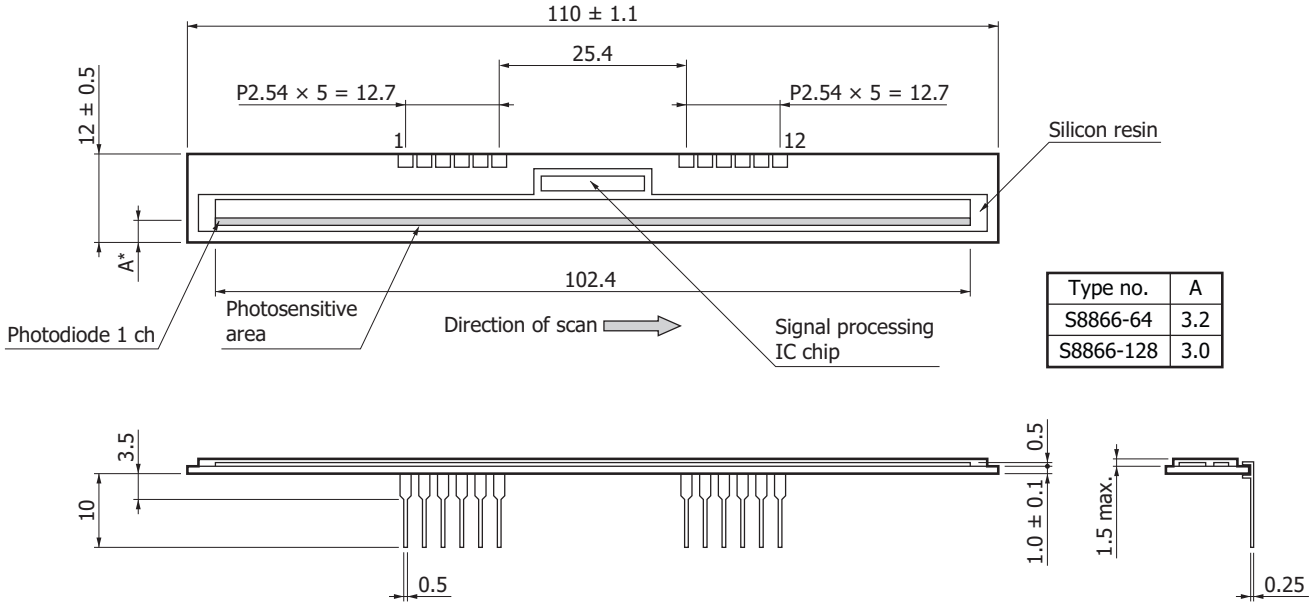


KMPDC0289EA

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse width	tpw(CLK)	500	-	25000	ns
Clock pulse rise/fall times	tr(CLK), tf(CLK)	0	20	30	ns
Reset pulse width 1	tpw(RESET1)	21	-	-	CLK
Reset pulse width 2	tpw(RESET2)	20	-	-	CLK
Reset pulse rise/fall times	tr(RESET), tf(RESET)	0	20	30	ns
Clock pulse-reset pulse timing 1	t1	-20	0	20	ns
Clock pulse-reset pulse timing 2	t2	-20	0	20	ns

1. The internal timing circuit starts operation at the falling edge of CLK immediately after a RESET pulse goes Low.
2. When the falling edge of each CLK is counted as "1 clock", the video signal of the 1st channel appears between "18.5 clocks and 20 clocks". Subsequent video signals appear every 4 clocks.
3. The trigger pulse for the 1st channel rises at a timing of 19.5 clocks and then rises every 4 clocks. The rising edge of each trigger pulse is the recommended timing for data acquisition.
4. Signal charge integration time equals the High period of a RESET pulse. However, the charge integration does not start at the rise of a RESET pulse but starts at the 8th clock after the rise of the RESET pulse and ends at the 8th clock after the fall of the RESET pulse. After the RESET pulse next changes from High to Low, signals integrated within this period are sequentially read out as time-series signals by the shift register operation. The rise and fall of a RESET pulse must be synchronized with the rise of a CLK pulse, but the rise of a RESET pulse must be set outside the video output period. One cycle of RESET pulses cannot be set shorter than the time equal to "16.5 + 4 × N (number of elements)" clocks.
5. The video signal after an EOS signal output becomes a high impedance state, and the video output will be indefinite.

Dimensional outline (unit: mm)



Type no.	A
S8866-64	3.2
S8866-128	3.0

* Length from the bottom of the board to the center of photosensitive area
Board: Ceramic

KMPDA0225EB

Pin connections

Pin no.	Symbol	Name	Note
1	RESET	Reset pulse	Pulse input
2	CLK	Clock pulse	Pulse input
3	Trig	Trigger pulse	Positive-going pulse output
4	EXTSP	External start pulse	Pulse input
5	Vms	Master/slave selection supply voltage	Voltage input
6	Vdd	Supply voltage	Voltage input
7	GND	Ground	
8	EOS	End of scan	Negative-going pulse output
9	Video	Video output	Negative-going output with respect to Vref
10	Vref	Reference voltage	Voltage input
11	Vgain	Gain selection terminal voltage	Voltage input
12	Vpd	Photodiode voltage	Voltage input

Gain selection terminal voltage setting

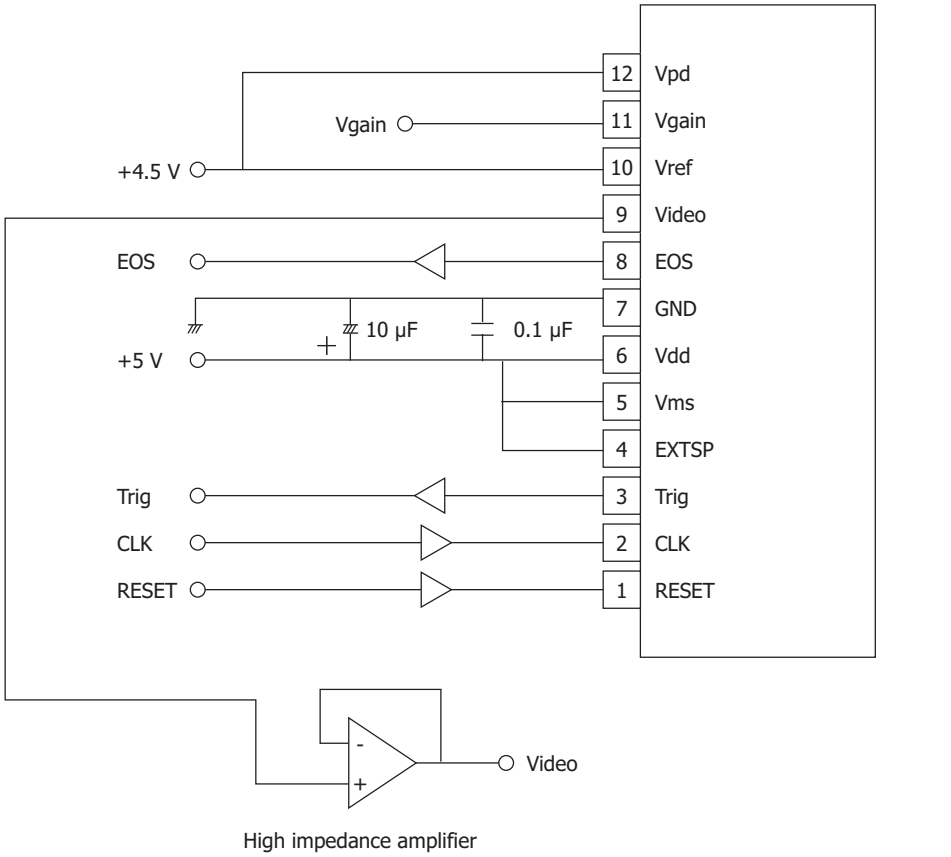
Vdd: High gain (Cf=0.5 pF) GND: Low gain (Cf=1 pF)

Setting for each readout method

Set to A in the table below in most cases.
To serially read out signals from two or more sensors linearly connected, set the 1st sensor to A and the 2nd or later sensors to B.
The CLK and RESET pulses should be shared with each sensor and the video output terminal of each sensor connected together.

Setting	Readout method	Vms	EXTSP
A	All stages of parallel readout, serial readout at 1st sensor	Vdd	Vdd
B	Serial readout at 2nd and later sensors	GND	Preceding sensor EOS should be input

[Figure 1] Connection example (parallel readout)



Readout circuit

Check that pulse signals meet the required pulse conditions before supplying them to the input terminals.
Video output should be amplified by an operational amplifier that is connected close to the sensor.

Precautions for use

(1) The signal processing IC chip is protected against static electricity. However, in order to prevent possible damage to the IC chip, take electrostatic countermeasures such as grounding yourself, as well as workbench and tools. Also protect the IC chip from surge voltages from peripheral equipment.

(2) Gold wires for wire bonding are very thin, so they easily break if subjected to mechanical stress. The signal processing IC chip, wire bonding section and photodiode array chip are covered with resin for protection. However, never touch these portions. Excessive force, if applied, may break the wires or cause malfunction.
Blow air to remove dust or debris if it gets on the protective resin. Never wash them with solvent.
Signals may not be obtained if dust or debris is left or a scratch is made on the protective resin, or the signal processing IC chip or photodiode array chip is nicked.

(3) The photodiode array characteristics may deteriorate when operated at high humidity, so put it in a hermetically sealed enclosure or case.
When installing the photodiode array on a board, be careful not to cause the board to warp.

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