Freescale Semiconductor
Product Brief

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PXS20 Product Brief

32-bit Power Architecture® Microcontrollers for Highly Reliable and Safe Operation Across a Range of Industrial, Medical, and Transportation Safety Critical Applications

The PXS20 series microcontrollers are system-on-chip devices that are built on Power Architecture® technology, are 100% user-mode compatible with the classic Power Architecture® instruction set, contain enhancements that improve the architecture's fit in embedded applications, include additional instruction support for digital signal processing (DSP), and integrate technologies to support highly reliable and safe operation across a range of industrial, medical and transportation safety critical applications. These microcontrollers include a rich set of peripherals for complex real time control, such as an enhanced timer unit, analog-to-digital converters, and multiple serial communications modules.

The PXS20 is designed for applications requiring a high Safety Integrity Level (SIL).

All devices in this family are built around a dual core safety platform with an innovative safety concept that reduces system cost and effort for the customer to achieve IEC61511 or IEC61508 certification of their

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system. In order to minimize software overhead and improve operational reliability, all major systems such as CPU core, DMA controller, interrupt controller, crossbar bus system, memory systems, peripheral systems, and memory protection unit, include built in redundancy and or robust system monitoring. Lock Step Redundancy Checking Units are implemented at each output of this Sphere of Replication (SoR). ECC is available for on-chip RAM and flash memories. A programmable fault collection and control unit monitors the integrity status of the device and provides flexible safe state control.

The host processor core of the PXS20 is the latest CPU from the e200 family of compatible Power Architecture® cores. The e200z4d 5-stage pipeline dual issue core provides a very high level of efficiency, allowing high performance with minimum power consumption.

The peripheral set provides high-end electrical motor control capability with very low CPU intervention, thanks to the on-chip Cross Triggering Unit (CTU).

This device incorporates high-performance 90 nm embedded flash-memory technology to provide substantial cost reduction per feature and significant performance improvement.

1 Application Examples

The PXS20 can be used for a variety of safety applications such as:

- Safety shutdown systems
- Solar inverters
- Motor drives
- Factory automation
- Aerospace
- Robotics

2 Features

This section describes the features of the PXS20 family.

2.1 PXS20 Features

Table 1 displays the PXS20 feature set.

Table 1. PXS20 Family Feature Set

Feature		PXS20
CPU	Type	2 × e200z4 (in lock-step or decoupled operation)
	Architecture	Harvard
	Execution speed	0 – 120 MHz (+2% FM)
	DMIPS intrinsic performance	> 240 MIPS
	SIMD (DSP + FPU)	Yes
	MMU	16 entry
	Instruction set PPC	Yes
	Instruction set VLE	Yes
	Instruction cache	4 KB, EDC
	MPU-16 regions	Yes, replicated module
	Semaphore unit (SEMA4)	Yes
Buses	Core bus	AHB, 32-bit address, 64-bit data
	Internal periphery bus	32-bit address, 32-bit data
Crossbar	Master × slave ports	Lock Step Mode: 4 × 3 Decoupled Parallel Mode: 6 × 3
Memory	Code/data flash	1 MB, ECC, RWW
	Static RAM (SRAM)	128 KB, ECC
Modules	Interrupt controller (INTC)	16 interrupt levels, replicated module
	Periodic Interrupt Timer (PIT)	1 × 4 channels
	System timer module (STM)	1 × 4 channels, replicated module
	Software watchdog timer (SWT)	Yes, replicated module
	eDMA	16 channels, replicated module
	FlexRay	1 × 64 message buffers, dual channel
	CAN	2 × 32 message buffers
	UART with DMA support	2
	Clock out	Yes
	Fault control & collection unit (FCCU)	Yes
	Cross triggering unit (CTU)	Yes
	eTimer	3 × 6 channels
	PWM	2 Module 4 × (2 + 1) channels
	Analog-to-digital converter (ADC)	2 × 12-bit ADC, 16 channels per ADC (3 internal, 4 shared and 9 external)

Table 1. PXS20 Family Feature Set (continued)

Feature		PXS20
Modules (cont.)	Sine-wave generator (SWG)	32 point
	Serial peripheral interface (SPI)	3 × SPI as many as 8 chip selects
	Cyclic redundancy checker (CRC) unit	Yes
	Junction temperature sensor (TSENS)	Yes, replicated module
	Digital I/Os	≥ 16
Supply	Device power supply	3.3 V with integrated bypassable ballast transistor External ballast transistor not needed for bare die
	Analog reference voltage	3.0 V – 3.6 V and 4.5 V – 5.5 V
Clocking	Frequency-modulated phase-locked loop (FMPLL)	2
	Internal RC oscillator	16 MHz
	External crystal oscillator	4 – 40 MHz
Debug	Nexus	Level 3+
Packages	Type	144 LQFP 257 MAPBGA
Temperature	Temperature range (junction)	–40 to 150 °C
	Ambient temperature range using external ballast transistor (LQFP)	–40 to 125 °C
	Ambient temperature range using external ballast transistor (BGA)	TBD

2.2 Block Diagram

Figure 1 and Figure 2 show the block diagram of the PXS20 microcontrollers.

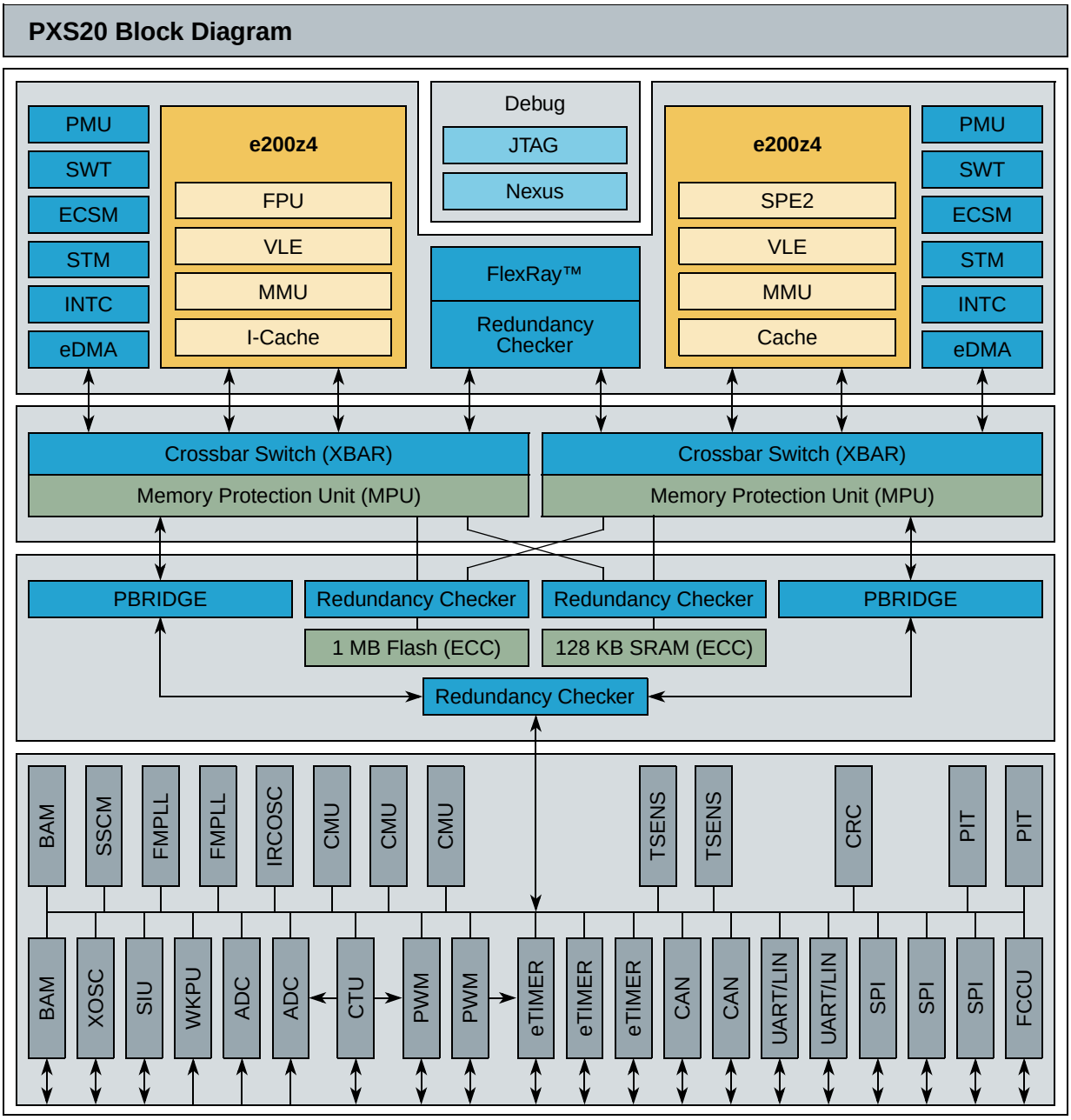


Figure 1. PXS20 block diagram

ADC – Analog-to-digital converter
BAM – Boot assist module
CAN – Controller area network controller
CMU – Clock monitoring unit
CRC – Cyclic redundancy check unit
CTU – Cross Triggering Unit
ECC – Error correction code
ECSM – Error correction status module
eDMA – Enhanced direct memory access controller
FCCU – Fault collection and control unit
FMPLL – Frequency modulated phase locked loop
INTC – Interrupt controller
IRCOSC – Internal RC oscillator
JTAG – Joint Test Action Group interface
MC – Mode entry, clock, reset, & power
PBRIDGE – Peripheral I/O bridge
PIT – Periodic interrupt timer
PMU – Power management unit
PWM – Pulse width modulator module
RC – Redundancy checker
RTC – Real time clock
SEMA4 – Semaphore unit
SIUL – System integration unit lite
SPI – Serial peripherals interface controller
SSCM – System status and configuration module
STM – System timer module
SWG – Sine wave generator
SWT – Software watchdog timer
TSENS – Temperature sensor
UART/LIN – Universal asynchronous receiver/transmitter/ local interconnect network
WKPU – Wakeup unit
XOSC – Crystal oscillator

Figure 2. PXS20 block diagram (continued)

2.3 Operating Parameters

The PXS20 operating parameters are listed as follows:

- Operating range 0 – 120 MHz
- –40 to +105 °C ambient temperature
- Fabricated in 90 nm low power process
- 1.2 V internal logic
- Internal voltage regulator (VREG) with integrated ballast transistor
  - — Single-supply designs offering high integration level to the customer
- 3.3 V ±10% for digital I/O input supply voltage
- Low power design
  - — Dynamic clock gating of core and peripherals
  - — Software controlled clock gating of peripherals
  - — Power consumption less than 400 mA
- Selectable current slew rate (slow/medium/fast)
- 3.3 V ± 10% Nexus pin rail. Same as digital I/O rail
- Unused pins configurable as GPIO or GPI for unused A/D channel inputs
- 3.3–5 V ±10% for A/D converter reference and analog input pins
- Designed with EMI reduction techniques
  - — Phase-locked loop (PLL)
  - — System clock with frequency modulation
  - — On-chip by-pass capacitance
  - — Software selectable current slew rate control
  - — Schmitt trigger on selected inputs
- Configurable pins

  - — Selectable pull-up, pull-down or no pull on all pins on all SIU controlled pins
  - — Selectable open drain
- Redundant temperature sensors in separate safety channels
- Multiple low/high voltage detector and inhibit units
  - — High voltage detection and inhibit with off-line testing capability on 1.2 V only
  - — Low voltage detection and inhibit with off-line testing capability on 1.2 V and 3.3 V supply
- Redundant bandgap to duplicate internal reference
- Deep N-well and wide column multiplexing where required to reduce Soft error rate (SER) effect for SRAM
- Physical separation of replicated functional blocks achieved by layout

2.4 Modes of Operation

PXS20 devices can operate in two modes of operation:

- Lock Step Mode (LSM)
- Decoupled Parallel Mode (DPM)

One of the two modes is statically selected at power-up. The selected mode may be changed only going through a full power-on reset.

2.4.1 Lock Step Mode (LSM)

Lock Step Mode (LSM) allows reaching the highest safety level. It has been defined to allow reaching SIL3 with minimum software overhead.

The Sphere of Replication (SoR) refers to a set of replicated IP modules where at the outputs a formal check is performed to ensure that the same operations or transactions are executed on a clock per clock basis (Lock Step Mode of operation).

The current concept assumes as premise that the most important goal for a functional safety SIL3-capable device is to detect (or diagnose) faults as they leave the SoR. In fact, a fault as long as it remains confined within the SoR and therefore will not generate an action visible outside the SoC or influence the effective operability of the periphery (and so the ECU), is not to be considered as a dangerous fault.

The presence of checkers (RC) at the outputs of the SoR for the periphery bus, the flash-memory subsystem and the SRAM subsystem represents a minimum guarantee that non-common cause faults are detected when the two channels redundantly are merged into a single actuator or recipient, on the action that is to be performed.

2.4.2 Decoupled Parallel Mode (DPM)

In Decoupled Parallel Mode (DPM) , each CPU core and connected channel run independently from the other one and redundancy checkers (RC) are disabled.

The DPM mode increased performances can be estimated in first approximation as about 1.6× the performance of the LSM mode at the same frequency for shared program flash configuration (up to 2×, depending on software).

PXS20 devices support only static configuration at power-on (either LSM or DPM).

2.4.3 Mode-Specific Performance Parameters

- LSM:
  - Up to 240 million integer instructions per second (dual integer unit)
  - Up to 240 million floating point instructions per second (FPU)
  - Up to 480 million multiply and accumulate instructions per second (SPE)
- DPM:
  - 384–480 million integer/floating point instructions per second
  - 768–960 million multiply and accumulate instructions per second

2.4.4 Functional Safety Suitability

The PXS20 has been successfully assessed by Exida Certification (Official Certification issued on Nov. 30th 2007) to be fit for purpose to achieve a safety integrity level 3 (SIL3) as per IEC61508-part 2 standard with an overall SoC PFH of 0.1 FIT in LSM mode.

The mode of operation which allows to reach the highest safety level with minimum software requirement is the Lock Step mode (LSM).

SIL3 innovative safety concept:

- LockStep mode and Fail-safe protection
- Sphere of replication (SoR) for key components (such as CPU core, eDMA, crossbar switch)
- Fault collection and control unit (FCCU)
- Redundancy control and checker unit (RCCU) on outputs of the SoR connected to FCCU
- Boot-time Built-In Self-Test for Memory (MBIST) and Logic (LBIST) triggered by hardware
- Boot-time Built-In Self-Test for ADC and flash memory triggered by software
- Replicated safety enhanced watchdog
- Replicated junction temperature sensor
- Non-maskable interrupt (NMI)
- 16-region memory protection unit (MPU)
- Clock monitoring units (CMU)
- Power management unit (PMU)
- Cyclic redundancy check (CRC) unit

2.5 Module Features

2.5.1 High-Performance e200z4d Core

The e200z4d Power Architecture® core provides the following features:

- 2 independent execution units, both supporting fixed-point and floating-point operations
- Dual issue 32-bit Power Architecture® technology compliant
  - 5-stage pipeline (IF, DEC, EX1, EX2, WB)
  - In-order execution and instruction retirement
- Full support for Power Architecture® instruction set and Variable Length Encoding (VLE)
  - Mix of classic 32-bit and 16-bit instruction allowed
  - Optimization of code size possible
- Thirty-two 64-bit general purpose registers (GPRs)
- Harvard bus (32-bit address, 64-bit data)
  - I-Bus interface capable of one outstanding transaction plus one piped with no wait-on-data return
  - D-Bus interface capable of two transactions outstanding to fill AHB pipe
- I-cache and I-cache controller
  - 4 KB, 256-bit cache line (programmable for 2- or 4-way)
- No data cache
- 16-entry MMU
- 8-entry branch table buffer
- Branch look-ahead instruction buffer to accelerate branching
- Dedicated branch address calculator
- 3 cycles worst case for missed branch
- Load/store unit
  - Fully pipelined
  - Single-cycle load latency
  - Big- and little-endian modes supported
  - Misaligned access support
  - Single stall cycle on load to use
- Single-cycle throughput (2-cycle latency) integer 32 × 32 multiplication
- 4 – 14 cycles integer 32 × 32 division (average division on various benchmark of nine cycles)
- Single precision floating-point unit
  - 1 cycle throughput (2-cycle latency) floating-point 32 × 32 multiplication
  - Target 9 cycles (worst case acceptable is 12 cycles) throughput floating-point 32 × 32 division
  - Special square root and min/max function implemented
- Signal processing support: APU-SPE 1.1
  - Support for vectorized mode: as many as two floating-point instructions per clock
- Vectored interrupt support

- Reservation instruction to support read-modify-write constructs
- Extensive system development and tracing support via Nexus debug port

2.5.2 Crossbar Switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between four master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows four concurrent transactions to occur from any master port to any slave port, although one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions.

The crossbar provides the following features:

- 4 masters and 3 slaves supported per each replicated crossbar
  - — Masters allocation for each crossbar: e200z4d core with two independent bus interface units (BIU) for I and D access (2 masters), one eDMA, one FlexRay
  - — Slaves allocation for each crossbar: a redundant flash-memory controller with 2 slave ports to guarantee maximum flexibility to handle Instruction and Data array, one redundant SRAM controller with 1 slave port each and 1 redundant peripheral bus bridge
- 32-bit address bus and 64-bit data bus
- Programmable arbitration priority
  - — Requesting masters can be treated with equal priority and are granted access to a slave port in round-robin method, based upon the ID of the last master to be granted access or a priority order can be assigned by software at application run time
- Temporary dynamic priority elevation of masters

The XBAR is replicated for each processor.

2.5.3 Memory Protection Unit (MPU)

The Memory Protection Unit splits the physical memory into 16 different regions. Each master (eDMA, FlexRay, CPU) can be assigned different access rights to each region.

- 16-region MPU with concurrent checks against each master access
- 32-byte granularity for protected address region

The memory protection unit is replicated for each processor.

2.5.4 Enhanced Direct Memory Access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware microarchitecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based

memory containing the transfer control descriptors (TCD) for the channels. This implementation is used to minimize the overall block size.

The eDMA module provides the following features:

- 16 channels supporting 8-, 16-, and 32-bit value single or block transfers
- Support variable sized queues and circular buffered queue
- Source and destination address registers independently configured to post-increment or stay constant
- Support major and minor loop offset
- Support minor and major loop done signals
- DMA task initiated either by hardware requestor or by software
- Each DMA task can optionally generate an interrupt at completion and retirement of the task
- Signal to indicate closure of last minor loop
- Transfer control descriptors mapped inside the SRAM

The eDMA controller is replicated for each processor.

2.5.5 On-Chip Flash Memory with ECC

This device includes programmable, non-volatile flash memory. The non-volatile memory (NVM) can be used for instruction storage or data storage, or both. The flash memory module interfaces with the system bus through a dedicated flash memory array controller. It supports a 64-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains four 128-bit prefetch buffers. Prefetch buffer hits allow no-wait responses. Buffer misses incur a 3 wait state response at 120 MHz.

The flash memory module provides the following features

- 1 MB of flash memory in unique multi-partitioned hard macro
- Sectorization: 16 KB + 2 × 48 KB + 16 KB + 2 × 64 KB + 2 × 128 KB + 2 × 256 KB
- EEPROM emulation (in software) within same module but on different partition
- 16 KB test sector and 16 KB shadow sector for test, censorship device and user option bits
- Wait states:
  - 3 wait states at 120 MHz
  - 2 wait states at 80 MHz
  - 1 wait state at 60 MHz
- Flash memory line 128-bit wide with 8-bit ECC on 64-bit word (total 144 bits)
- Accessed via a 64-bit wide bus for write and a 128-bit wide array for read operations
- 1-bit error correction, 2-bit error detection

2.5.6 On-Chip SRAM with ECC

The PXS20 SRAM provides a general-purpose single port memory.

ECC handling is done on a 32-bit boundary for data and it is extended to the address to have the highest possible diagnostic coverage including the array internal address decoder.

The SRAM module provides the following features:

- System SRAM: 128 KB
- ECC on 32-bit word (syndrome of 7 bits)
  - — ECC covers SRAM bus address
- 1-bit error correction, 2-bit error detection
- Wait states:
  - — 1 wait state at 120 MHz
  - — 0 wait states at 80 MHz and 60 MHz

2.5.7 Platform Flash Memory Controller

The following list summarizes the key features of the flash memory controller:

- Single AHB port interface supports a 64-bit data bus. All AHB aligned and unaligned reads within the 32-bit container are supported. Only aligned word writes are supported.
- Array interfaces support a 128-bit read data bus and a 64-bit write data bus for each bank.
- Code flash (bank0) interface provides configurable read buffering and page prefetch support.
  - — Four page-read buffers (each 128 bits wide) and a prefetch controller support speculative reading and optimized flash access.
- Single-cycle read responses (0 AHB data-phase wait states) for hits in the buffers. The buffers implement a least-recently-used replacement algorithm to maximize performance.
- Data flash (bank1) interface includes a 128-bit register to temporarily hold a single flash page. This logic supports single-cycle read responses (0 AHB data-phase wait states) for accesses that hit in the holding register.
  - — No prefetch support is provided for this bank.
- Programmable response for read-while-write sequences including support for stall-while-write, optional stall notification interrupt, optional flash operation abort , and optional abort notification interrupt.
- Separate and independent configurable access timing (on a per bank basis) to support use across a wide range of platforms and frequencies.
- Support of address-based read access timing for emulation of other memory types.
- Support for reporting of single- and multi-bit error events.
- Typical operating configuration loaded into programming model by system reset.

The platform flash controller is replicated for each processor.

2.5.8 Platform Static RAM Controller (SRAMC)

The SRAMC module is the platform SRAM array controller, with integrated error detection and correction.

The main features of the SRAMC provide connectivity for the following interfaces:

- XBAR Slave Port (64-bit data path)
- ECSM (ECC Error Reporting, error injection and configuration)
- SRAM array

The following functions are implemented:

- ECC encoding (32-bit boundary for data and complete address bus)
- ECC decoding (32-bit boundary and entire address)
- Address translation from the AHB protocol on the XBAR to the SRAM array

The platform SRAM controller is replicated for each processor.

2.5.9 Memory Subsystem Access Time

Every memory access the CPU performs requires at least one system clock cycle for the data phase of the access. Slower memories or peripherals may require additional data phase wait states. Additional data phase wait states may also occur if the slave being accessed is not parked on the requesting master in the crossbar.

Table 2 shows the number of additional data phase wait states required for a range of memory accesses.

Table 2. Platform Memory Access Time Summary

AHB transfer	Data phase wait states	Description
e200z4d instruction fetch	0	Flash memory prefetch buffer hit (page hit)
e200z4d instruction fetch	3	Flash memory prefetch buffer miss (based on 4-cycle random flash array access time)
e200z4d data read	0–1	SRAM read
e200z4d data write	0	SRAM 32-bit write
e200z4d data write	0	SRAM 64-bit write (executed as 2 x 32-bit writes)
e200z4d data write	0–2	SRAM 8-,16-bit write (Read-modify-Write for ECC)
e200z4d flash memory read	0	Flash memory prefetch buffer hit (page hit)
e200z4d flash memory read	3	Flash memory prefetch buffer miss (at 120 MHz; includes 1 cycle of program flash memory controller arbitration)

2.5.10 Error Correction Status Module (ECSM)

The ECSM on this device manages the ECC configuration and reporting for the platform memories (flash memory and SRAM). It does not implement the actual ECC calculation. A detected error (double error for flash memory or SRAM) is also reported to the FCCU. The following errors and indications are reported into the ECSM dedicated registers:

- ECC error status and configuration for flash memory and SRAM
- ECC error reporting for flash memory

- ECC error reporting for SRAM
- ECC error injection for SRAM

2.5.11 Peripheral Bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access right per peripheral (per master: read access enable; write access enable)
- Write buffering for peripherals
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

2.5.12 Interrupt Controller (INTC)

The INTC provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high-priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

The INTC provides the following features:

- Duplicated periphery
- Unique 9-bit vector per interrupt source
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resource

The INTC is replicated for each processor.

2.5.13 System Clocks and Clock Generation

The following list summarizes the system clock and clock generation on this device:

- Lock status continuously monitored by lock detect circuitry
- Loss-of-clock (LOC) detection for reference and feedback clocks
- On-chip loop filter (for improved electromagnetic interference performance and fewer external components required)
- Programmable output clock divider of system clock (÷1, ÷2, ÷4, ÷8)

- PWM module and as many as three eTimer modules running on an auxiliary clock independent from system clock (with max frequency 120 MHz)
- On-chip crystal oscillator with automatic level control
- Dedicated internal 16 MHz internal RC oscillator for rapid start-up
  - Supports automated frequency trimming by hardware during device startup and by user application
- Auxiliary clock domain for motor control periphery (PWM, eTimer, CTU, ADC, and SWG)

2.5.14 Frequency-Modulated Phase-Locked Loop (FMPLL)

Each device has two FMPLLs.

Each FMPLL allows the user to generate high speed system clocks starting from a minimum reference of 4 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The FMPLL multiplication factor, output clock divider ratio are all software configurable. The FMPLLs have the following major features:

- Input frequency: 4–40 MHz continuous range (limited by the crystal oscillator)
- Voltage controlled oscillator (VCO) range: 256–512 MHz
- Frequency modulation via software control to reduce and control emission peaks
  - Modulation depth ±2% if centered or 0% to –4% if downshifted via software control register
  - Modulation frequency: triangular modulation with 25 kHz nominal rate
- Option to switch modulation on and off via software interface
- Reduced frequency divider (RFD) for reduced frequency operation without re-lock
- 3 modes of operation
  - Bypass mode
  - Normal FMPLL mode with crystal reference (default)
  - Normal FMPLL mode with external reference
- Lock monitor circuitry with lock status
- Loss-of-lock detection for reference and feedback clocks
- Self-clocked mode (SCM) operation
- On-chip loop filter
- Auxiliary FMPLL
  - Used for FlexRay due to precise symbol rate requirement by the protocol
  - Used for motor control periphery and connected IP (A/D digital interface CTU) to allow independent frequencies of operation for PWM and timers and jitter-free control
  - Option to enable/disable modulation to avoid protocol violation on jitter and/or potential unadjusted error in electric motor control loop
  - Allows to run motor control periphery at different (precisely lower, equal or higher as required) frequency than the system to ensure higher resolution

2.5.15 Main Oscillator

The main oscillator provides these features:

- Input frequency range 4–40 MHz
- Crystal input mode
- External reference clock (3.3 V) input mode
- FMPLL reference

2.5.16 Internal Reference Clock (RC) Oscillator

The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared to the stable bandgap reference voltage. The RC oscillator is the device safe clock.

The RC oscillator provides these features:

- Nominal frequency 16 MHz
- ±5% variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the FMPLL
- RC oscillator is used as the default system clock during startup and can be used as back-up input source of FMPLL(s) in case XOSC fails

2.5.17 Clock, Reset, Power Mode, and Test Control Modules (MC_CGM, MC_RGM, MC_PCU, and MC_ME)

These modules provide the following:

- Clock gating and clock distribution control
- Halt, stop mode control
- Flexible configurable system and auxiliary clock dividers
- Various execution modes
  - — Reset, Idle, Test, Safe
  - — Various RUN modes with software selectable powered modules
  - — No stand-by mode implemented (no internal switchable power domains)

2.5.18 Periodic Interrupt Timer Module (PIT)

The PIT module implements the following features:

- 4 general purpose interrupt timers
- 32-bit counter resolution
- Can be used for software tick or DMA trigger operation

2.5.19 System Timer Module (STM)

The STM implements the following features:

- Up-counter with 4 output compare registers
- OS task protection and hardware tick implementation per AUTOSAR[1] requirement

The STM is replicated for each processor.

2.5.20 Software Watchdog Timer (SWT)

This module implements the following features:

- Fault tolerant output
- Safe internal RC oscillator as reference clock
- Windowed watchdog
- Program flow control monitor with 16-bit pseudorandom key generation
- Allows a high level of safety (SIL3 monitor)

The SWT module is replicated for each processor.

2.5.21 Fault Collection and Control Unit (FCCU)

The FCCU module has the following features:

- Redundant collection of hardware checker results
- Redundant collection of error information and latch of faults from critical modules on the device
- Collection of self-test results
- Configurable and graded fault control
  - — Internal reactions (no internal reaction, IRQ, Functional Reset, Destructive Reset, or Safe mode entered)
  - — External reaction (failure is reported to the external/surrounding system via configurable output pins)

2.5.22 System Integration Unit Lite (SIUL)

The SIUL controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

The SIU provides the following features:

- Centralized pad control on a per-pin basis
  - — Pin function selection

1.Open System Architecture

  - Configurable weak pull-up/down
  - Configurable slew rate control (slow/medium/fast)
  - Hysteresis on GPIO pins
  - Configurable automatic safe mode pad control
- Input filtering for external interrupts

2.5.23 Non-Maskable Interrupt (NMI)

The non-maskable interrupt with de-glitching filter supports high-priority core exceptions.

2.5.24 Boot Assist Module (BAM)

The BAM is a block of read-only memory with hard-coded content. The BAM program is executed only if serial booting mode is selected via boot configuration pins.

The BAM provides the following features:

- Enables booting via serial mode (CAN or UART/LIN)
- Supports programmable 64-bit password protection for serial boot mode
- Supports serial bootloading of either classic PowerPC Book E code (default) or Freescale VLE code
- Automatic switch to serial boot mode if internal flash memory is blank or invalid

2.5.25 System Status and Configuration Module (SSCM)

The SSCM on this device features the following:

- System configuration and status
- Debug port status and debug port enable
- Multiple boot code starting locations out of reset through implementation of search for valid Reset Configuration Half Word
- Sets up the MMU to allow user boot code to execute as either classic PowerPC Book E code (default) or as Freescale VLE code out of flash memory
- Triggering of device self-tests during reset phase of device boot

2.5.26 Controller Area Network Module (CAN)

The CAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. Although the CAN interface was designed to be used primarily as a vehicle networking bus, it is widely used in industrial and other transport applications due to its robust operation, time determinism, cost effectiveness, and optional redundant physical layer implementation.

The CAN module provides the following features:

- Full implementation of the CAN protocol specification, version 2.0B
  - Standard data and remote frames

  - Extended data and remote frames
  - 0 to 8 bytes data length
  - Programmable bit rate as fast as 1Mbit/s
- 32 message buffers of 0 to 8 bytes data length
- Each message buffer configurable as receive or transmit buffer, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- 3 programmable mask registers
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification
- Receive features
  - Individual programmable filters for each mailbox
  - 8 mailboxes configurable as a 6-entry receive FIFO
  - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid FMPLL jitter

2.5.27 FlexRay

The FlexRay module provides the following features:

- Full implementation of FlexRay Protocol Specification 2.1 Rev. A
- 64 configurable message buffers can be handled
- Dual channel or single channel mode of operation, each as fast as 10 Mbit/s data rate
- Message buffers configurable as transmit or receive
- Message buffer size configurable
- Message filtering for all message buffers based on Frame ID, cycle count, and message ID
- Programmable acceptance filters for receive FIFO

- Message buffer header, status, and payload data stored in system memory (SRAM)
- Internal FlexRay memories have error detection and correction

2.5.28 Serial Communication Interface Module (UART)

The UART module with DMA support on this device features the following:

- UART features:
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit or 9-bit words)
  - Error detection and flagging
    - Parity, noise and framing errors
  - Interrupt driven operation with 4 interrupts sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - 2 receiver wake-up methods
- LIN features:
  - Autonomous LIN frame handling
  - Message buffer to store identifier and up to eight data bytes
  - Supports message length of up to 64 bytes
  - Detection and flagging of LIN errors
  - Sync field; Delimiter; ID parity; Bit, Framing; Checksum and Timeout errors
  - Classic or extended checksum calculation
  - Configurable Break duration of up to 36-bit times
  - Programmable Baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features
    - Loop back
    - Self Test
    - LIN bus stuck dominant detection
  - Interrupt driven operation with 16 interrupt sources
  - LIN slave mode features
    - Autonomous LIN header handling
    - Autonomous LIN response handling
    - Discarding of irrelevant LIN responses using up to 16 ID filters

2.5.29 Serial Peripheral Interface (SPI)

The SPI modules provide a synchronous serial interface for communication between the PXS20 and external devices.

A SPI module provides these features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- As many as 8 chip select lines available, depending on package and pin multiplexing
- 4 clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for de-glitching
- FIFOs for buffering as many as 5 transfers on the transmit and receive side
- Queueing operation possible through use of the eDMA
- General purpose I/O functionality on pins when not used for SPI

2.5.30 Pulse Width Modulator (PWM)

The PWM module contains four PWM channels, each of which is configured to control a single half-bridge power stage. Two modules are included on 257 MAPBGA devices; on the 144 LQFP package, only one module is present. Additionally, four fault input channels are provided per PWM module.

This PWM is capable of controlling most motor types, including:

- AC induction motors (ACIM)
- Permanent Magnet AC motors (PMAC)
- Brushless (BLDC) and brush DC motors (BDC)
- Switched (SRM) and variable reluctance motors (VRM)
- Stepper motors

A PWM module implements the following features:

- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs
- Maximum operating frequency as high as 120 MHz
  - Clock source not modulated and independent from system clock (generated via secondary FMPLL)
- Fine granularity control for enhanced resolution of the PWM period
- PWM outputs can operate as complementary pairs or independent channels
- Ability to accept signed numbers for PWM generation

- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM supported
- Double buffered PWM registers
  - — Integral reload rates from 1 to 16
  - — Half cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software control for each PWM output
- All outputs can be forced to a value simultaneously
- PWMX pin can optionally output a third signal from each channel
- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual edge capture functionality
- Option to supply the source for each complementary PWM signal pair from any of the following:
  - — External digital pin
  - — Internal timer channel
  - — External ADC input, taking into account values set in ADC high- and low-limit registers
- DMA support

2.5.31 eTimer Module

The PXS20 provides three eTimer modules on the 257 MAPBGA device, and two eTimer modules on the 144 LQFP package. Six 16-bit general purpose up/down timer/counters per module are implemented with the following features:

- Maximum clock frequency of 120 MHz
- Individual channel capability
  - — Input capture trigger
  - — Output compare
  - — Double buffer (to capture rising edge and falling edge)
  - — Separate prescaler for each counter
  - — Selectable clock source
  - — 0–100% pulse measurement
  - — Rotation direction flag (Quad decoder mode)
- Maximum count rate

  - Equals peripheral clock divided by 2 for external event counting
  - Equals peripheral clock for internal clock counting
- Cascadeable counters
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Preloadable counters
- Pins available as GPIO when timer functionality not in use
- DMA support

2.5.32 Sine Wave Generator (SWG)

A digital-to-analog converter is available to generate a sine wave based on 32 stored values for external devices (ex: resolver).

- Frequency range from 1 kHz to 50 kHz
- Sine wave amplitude from 0.47 V to 2.26 V

2.5.33 Analog-to-Digital Converter Module (ADC)

The ADC module features include:

Analog part:

- 2 on-chip ADCs
  - 12-bit resolution SAR architecture
  - A/D Channels: 9 external, 3 internal and 4 shared with other A/D (total 16 channels)
  - One channel dedicated to each T-sensor to enable temperature reading during application
  - Separated reference for each ADC
  - Shared analog supply voltage for both ADCs
  - One sample and hold unit per ADC
  - Adjustable sampling and conversion time

Digital part:

- 4 analog watchdogs comparing ADC results against predefined levels (low, high, range) before results are stored in the appropriate ADC result location
- 2 modes of operation: Motor Control Mode or Regular Mode
- Regular mode features
  - Register based interface with the CPU: one result register per channel
  - ADC state machine managing three request flows: regular command, hardware injected command, software injected command
  - Selectable priority between software and hardware injected commands

  - 4 analog watchdogs comparing ADC results against predefined levels (low, high, range)
  - DMA compatible interface
- Motor control mode features
  - Triggered mode only
  - 4 independent result queues (1 × 16 entries, 2 × 8 entries, 1 × 4 entries)
  - Result alignment circuitry (left justified; right justified)
  - 32-bit read mode allows to have channel ID on one of the 16-bit parts
  - DMA compatible interfaces
- Built-in self-test features triggered by software

2.5.34 Junction Temperature Sensor

The junction temperature sensor provides a value via an ADC channel that can be used by software to calculate the device junction temperature.

The key parameters of the junction temperature sensor include:

- Nominal temperature range from –40 to 150 °C
- Software temperature alarm via analog ADC comparator possible

2.5.35 Cross Triggering Unit (CTU)

The ADC cross triggering unit allows automatic generation of ADC conversion requests on user selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

The CTU implements the following features:

- Cross triggering between ADC, PWM, eTimer, and external pins
- Double buffered trigger generation unit with as many as 8 independent triggers generated from external triggers
- Maximum operating frequency less than or equal to 120 MHz
- Trigger generation unit configurable in sequential mode or in triggered mode
- Trigger delay unit to compensate the delay of external low pass filter
- Double buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double buffered ADC command list pointers to minimize ADC-trigger unit update
- Double buffered ADC conversion command list with as many as 24 ADC commands
- Each trigger capable of generating consecutive commands
- ADC conversion command allows control of ADC channel from each ADC, single or synchronous sampling, independent result queue selection
- DMA support with safety features

2.5.36 Cyclic Redundancy Checker (CRC) Unit

The CRC module is a configurable multiple data flow unit to compute CRC signatures on data written to its input register.

The CRC unit has the following features:

- 3 sets of registers to allow 3 concurrent contexts with possibly different CRC computations, each with a selectable polynomial and seed
- Computes 16- or 32-bit wide CRC on the fly (single-cycle computation) and stores result in internal register.
  The following standard CRC polynomials are implemented:
  — $x^{16} + x^{12} + x^5 + 1$ [16-bit CRC-CCITT]
  — $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$ [32-bit CRC-ethernet(32)]
- Key engine to be coupled with communication periphery where CRC application is added to allow implementation of safe communication protocol
- Offloads core from cycle-consuming CRC and helps checking configuration signature for safe start-up or periodic procedures
- CRC unit connected as peripheral bus on internal peripheral bus
- DMA support

2.5.37 Redundancy Control and Checker Unit (RCCU)

The RCCU checks all outputs of the sphere of replication (addresses, data, control signals). It has the following features:

- Duplicated module to guarantee highest possible diagnostic coverage (check of checker)
- Multiple times replicated IPs are used as checkers on the SoR outputs

2.5.38 Voltage Regulator / Power Management Unit (PMU)

The on-chip voltage regulator module provides the following features:

- Single external rail required
- Single high supply required: nominal 3.3 V for packaged option
  — Packaged option requires external ballast transistor due to reduced dissipation capacity at high temperature but can use embedded transistor if power dissipation is maintained within package dissipation capacity (lower frequency of operation)
- All I/Os are at same voltage as external supply (3.3 V nominal)
- Duplicated Low-Voltage Detectors (LVD) to guarantee proper operation at all stages (reset, configuration, normal operation) and, to maximize safety coverage, one LVD can be tested while the other operates (on-line self-testing feature)

2.5.39 Built-In Self-Test (BIST) Capability

This device includes the following protection against latent faults:

- Boot-time Memory Built-In Self-Test (MBIST)
- Boot-time scan-based Logic Built-In Self-Test (LBIST)
- Run-time ADC Built-In Self-Test (BIST)
- Run-time Built-In Self Test of LVDs

2.5.40 IEEE 1149.1 JTAG Controller (JTAGC)

The JTAGC block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE standard.

The JTAG controller provides the following features:

- IEEE Test Access Port (TAP) interface with 5 pins:
  - TDI
  - TMS
  - TCK
  - TDO
  - JCOMP
- Selectable modes of operation include JTAGC/debug or normal system operation
- 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS
  - IDCODE
  - EXTEST
  - SAMPLE
  - SAMPLE/PRELOAD
- 3 test data registers: a bypass register, a boundary scan register, and a device identification register. The size of the boundary scan register is parameterized to support a variety of boundary scan chain lengths.
- TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry

2.5.41 Nexus Port Controller (NPC)

The NPC module provides real-time development support capabilities for this device in compliance with the IEEE-ISTO 5001-2008 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility.

The NPC block interfaces to the host processor and internal buses to provide development support as per the IEEE-ISTO 5001-2008 Class 3+, including selected features from Class 4 standard.

The development support provided includes program trace, data trace, watchpoint trace, ownership trace, run-time access to the MCUs internal memory map and access to the Power Architecture® internal registers during halt. The Nexus interface also supports a JTAG only mode using only the JTAG pins. The following features are implemented:

- Full and reduced port modes
- MCKO (message clock out) pin
- 4 or 12 MDO (message data out) pins[1]
- 2 $\overline{\text{MSEO}}$ (message start/end out) pins
- $\overline{\text{EVTO}}$ (event out) pin
  - — Auxiliary input port
- $\overline{\text{EVTI}}$ (event in) pin
- 5-pin JTAG port (JCOMP, TDI, TDO, TMS, and TCK)
  - — Supports JTAG mode
- Host processor (e200) development support features
  - — Data trace via data write messaging (DWM) and data read messaging (DRM). This allows the development tool to trace reads or writes, or both, to selected internal memory resources.
  - — Ownership trace via ownership trace messaging (OTM). OTM facilitates ownership trace by providing visibility of which process ID or operating system task is activated. An ownership trace message is transmitted when a new process/task is activated, allowing development tools to trace ownership flow.
  - — Program trace via branch trace messaging (BTM). Branch trace messaging displays program flow discontinuities (direct branches, indirect branches, exceptions, etc.), allowing the development tool to interpolate what transpires between the discontinuities. Thus, static code may be traced.
  - — Watchpoint messaging (WPM) via the auxiliary port
  - — Watchpoint trigger enable of program and/or data trace messaging
  - — Data tracing of instruction fetches via private opcodes

3 Developer Support

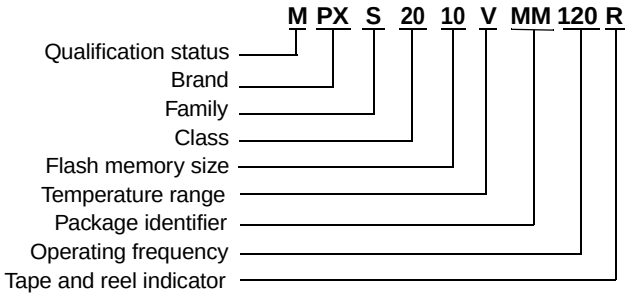
This family of MCUs is suppported by Freescale's Tower Development System as well as a broad set of advanced debug and runtime software:

- CodeWarrior
- FreeMaster
- MQX
- RAppID Init
- RAppID Toolbox

1. 4 MDO pins on 144 LQFP package, 12 MDO pins on 257 MAPBGA package.

- Green Hills

4 Orderable Parts



Qualification status
P = Pre-qualification (engineering samples)
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

Family
D = Display Graphics
N = Connectivity/Network
R = Performance/Real Tiime Control
S = Safety

Flash Memory Size
05 = 512 KB
10 = 1 MB

Temperature range
V = –40 °C to 105 °C (ambient)

Package identifier
LQ = 144 LQFP
MM = 257 MAPBGA

Operating frequency
80 = 80 MHz
120 = 120 MHz

Tape and reel status
R = Tape and reel
(blank) = Trays

Note: Not all options are available on all devices. See Table 3 for more information.

Table 3. Orderable part number summary

Part number	Flash/SRAM	Package	Speed (MHz)
MPXS2005VLQ80	512 KB / 128 KB	144 LQFP (20 mm x 20 mm)	80
MPXS2010VLQ80	1 MB / 128 KB	144 LQFP (20 mm x 20 mm)	80
MPXS2010VMM80	1 MB / 128 KB	257 MAPBGA (14 mm x 14 mm)	80
MPXS2010VLQ120	1 MB / 128 KB	144 LQFP (20 mm x 20 mm)	120
MPXS2010VMM120	1 MB / 128 KB	257 MAPBGA (14 mm x 14 mm)	120

5 Revision History

Table 4 summarizes revisions to this document.

Table 4. Revision History

Revision (Date)	Description
Rev. 1 (June 2011)	Initial release.

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