

# NP0J1A3

## Silicon PNP epitaxial planar type

For digital circuits

### ■ Features

- SSS-Mini type 6-pin package, reduction of the mounting area and assembly cost by half
- Maximum package height (0.4 mm) contributes to develop thinner equipments

### ■ Basic Part Number

- UNR11A3 × 2

### ■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

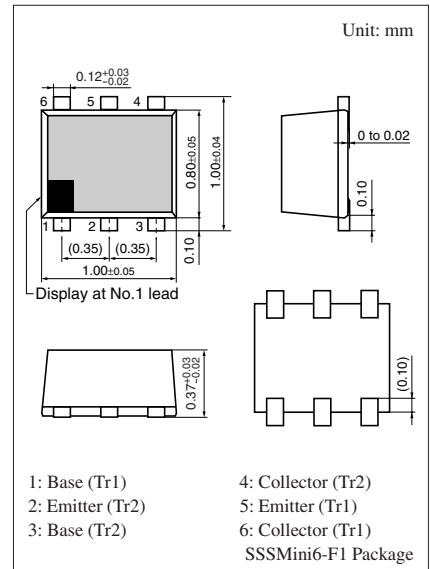
Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	$V_{CBO}$	-50	V
Collector-emitter voltage (Base open)	$V_{CEO}$	-50	V
Collector current	$I_C$	-80	mA
Total power dissipation *	$P_T$	125	mW
Junction temperature	$T_j$	125	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +125	$^\circ\text{C}$

Note) \*: Measuring on substrate at 17 mm × 10 mm × 1 mm

### ■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

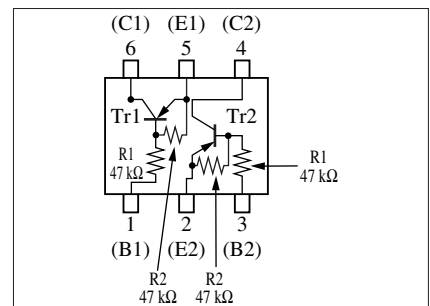
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	$V_{CBO}$	$I_C = -10 \mu\text{A}, I_E = 0$	-50			V
Collector-emitter voltage (Base open)	$V_{CEO}$	$I_C = -2 \text{ mA}, I_B = 0$	-50			V
Collector-base cutoff current (Emitter open)	$I_{CBO}$	$V_{CB} = -50 \text{ V}, I_E = 0$			-0.1	$\mu\text{A}$
Collector-emitter cutoff current (Base open)	$I_{CEO}$	$V_{CE} = -50 \text{ V}, I_B = 0$			-0.5	$\mu\text{A}$
Emitter-base cutoff current (Collector open)	$I_{EBO}$	$V_{EB} = -6 \text{ V}, I_C = 0$			-0.1	mA
Forward current transfer ratio	$h_{FE}$	$V_{CE} = -10 \text{ V}, I_C = -5 \text{ mA}$	80			—
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = -10 \text{ mA}, I_B = -0.3 \text{ mA}$			-0.25	V
Output voltage high level	$V_{OH}$	$V_{CC} = -5 \text{ V}, V_B = -0.5 \text{ V}, R_L = 1 \text{ k}\Omega$	-4.9			V
Output voltage low level	$V_{OL}$	$V_{CC} = -5 \text{ V}, V_B = -3.5 \text{ V}, R_L = 1 \text{ k}\Omega$			-0.2	V
Input resistance	$R_1$		-30%	47	+30%	$\text{k}\Omega$
Resistance ratio	$R_1 / R_2$		0.8	1.0	1.2	—
Transition frequency	$f_T$	$V_{CB} = -10 \text{ V}, I_E = 1 \text{ mA}, f = 200 \text{ MHz}$		80		MHz

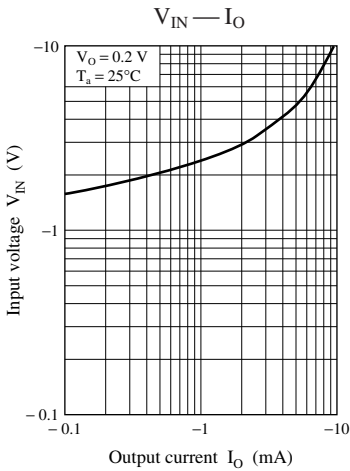
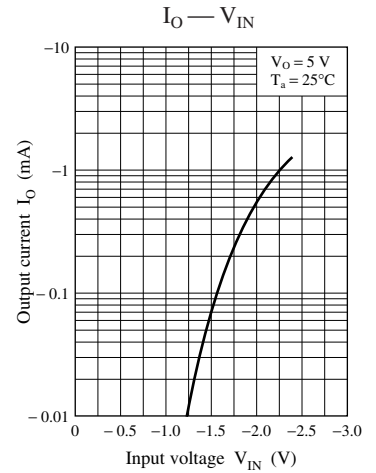
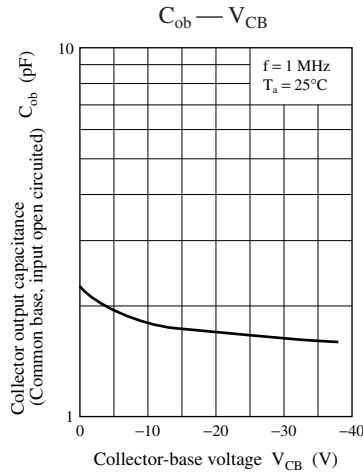
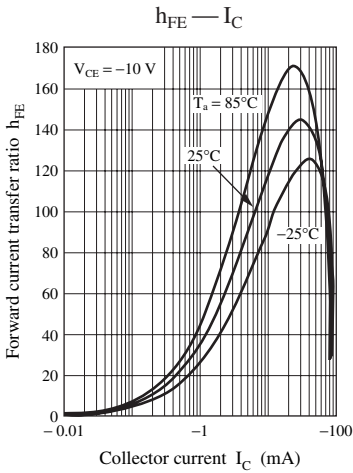
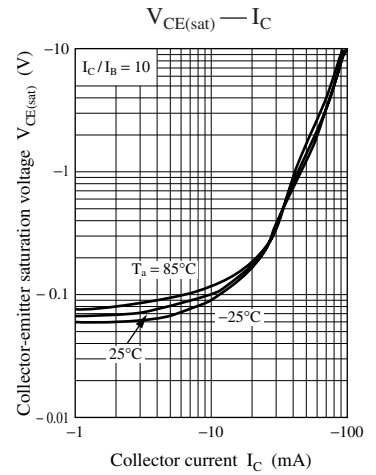
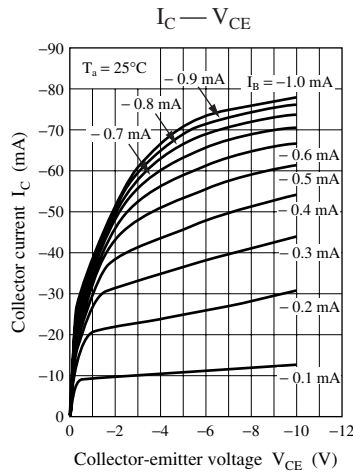
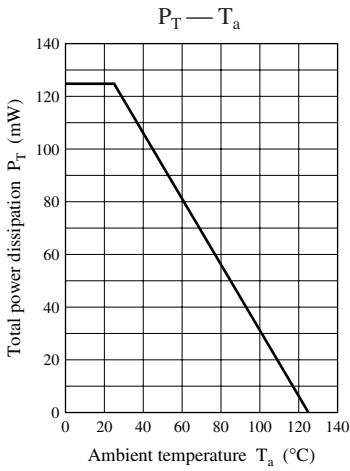
Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.



Marking Symbol: 1L

Internal Connection





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