

NIKO-SEM**P-Channel Logic Level Enhancement**

Mode Field Effect Transistor

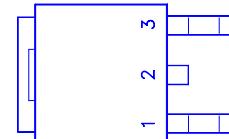
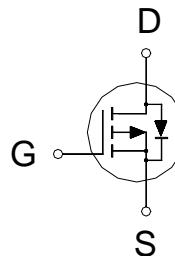
P8006EDG

TO-252

Lead-Free

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-55V	80m	-8A



1. GATE
2. DRAIN
3. SOURCE

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-55	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^\circ\text{C}$	I_D	-7	A
	$T_C = 70^\circ\text{C}$		-6	
Pulsed Drain Current ¹		I_{DM}	-30	
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	28	W
	$T_C = 70^\circ\text{C}$		18	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	$^\circ\text{C}$
Lead Temperature ($1/16$ " from case for 10 sec.)		T_L	275	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		3	$^\circ\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		75	$^\circ\text{C} / \text{W}$

¹Pulse width limited by maximum junction temperature.²Duty cycle $\leq 1\%$ **ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$	-55			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-1	-1.5	-2.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$			± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -44\text{V}, V_{GS} = 0\text{V}$			1	μA
		$V_{DS} = -36\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$			10	
On-State Drain Current ¹	$I_{D(\text{ON})}$	$V_{DS} = -5\text{V}, V_{GS} = -10\text{V}$	-32			A

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Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -4.5V, I_D = -6A$		90	150	m
		$V_{GS} = -10V, I_D = -7A$		60	80	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -10V, I_D = -7A$		9		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -30V, f = 1MHz$		760		pF
Output Capacitance	C_{oss}			90		
Reverse Transfer Capacitance	C_{rss}	$V_{DS} = 0.5V_{(BR)DSS}, V_{GS} = -10V,$ $I_D = -7A$		40		nC
Total Gate Charge ²	Q_g			15		
Gate-Source Charge ²	Q_{gs}	$V_{DS} = -20V, R_L = 1$		2.5		nS
Gate-Drain Charge ²	Q_{gd}			3.0		
Turn-On Delay Time ²	$t_{d(on)}$	$I_D \geq -1A, V_{GS} = -10V, R_{GS} = 6$		7	14	nS
Rise Time ²	t_r			10	20	
Turn-Off Delay Time ²	$t_{d(off)}$			19	34	
Fall Time ²	t_f			12	22	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25^\circ C$)						
Continuous Current	I_S				-1.3	A
Pulsed Current ³	I_{SM}				-2.6	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			-1	V
Reverse Recovery Time	t_{rr}	$I_F = -7 A, dI_F/dt = 100A / \mu S$		15.5		nS
Reverse Recovery Charge	Q_{rr}			7.9		nC

¹Pulse test : Pulse Width $\leq 300 \mu sec$, Duty Cycle $\leq 2\%$.²Independent of operating temperature.³Pulse width limited by maximum junction temperature.**REMARK: THE PRODUCT MARKED WITH “P8006EDG”, DATE CODE or LOT #**

Orders for parts with Lead-Free plating can be placed using the PXXXXXXG parts name.

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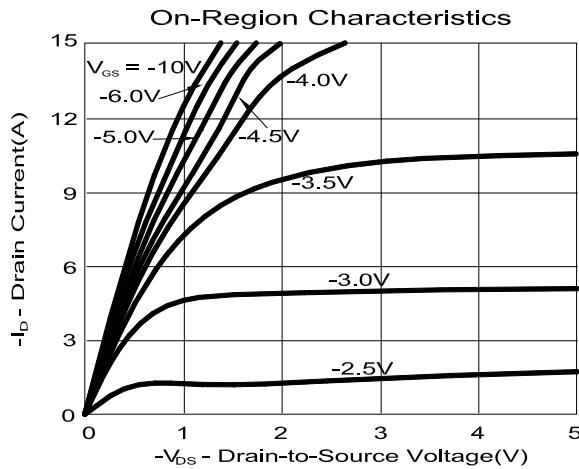
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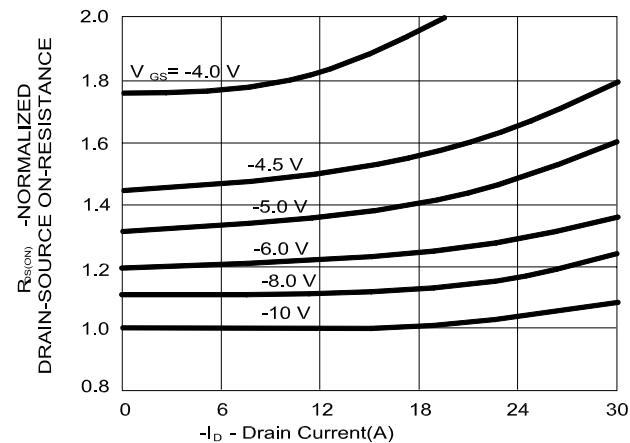
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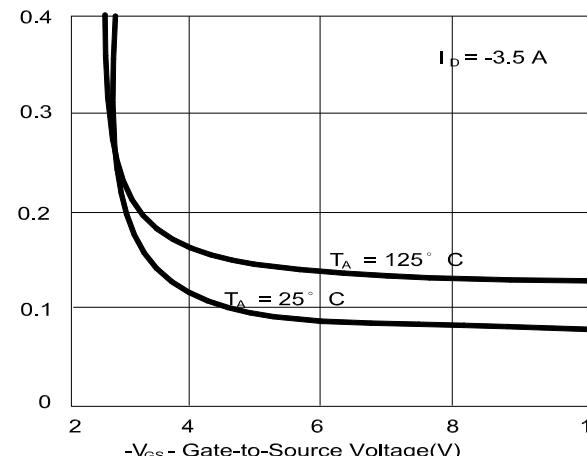
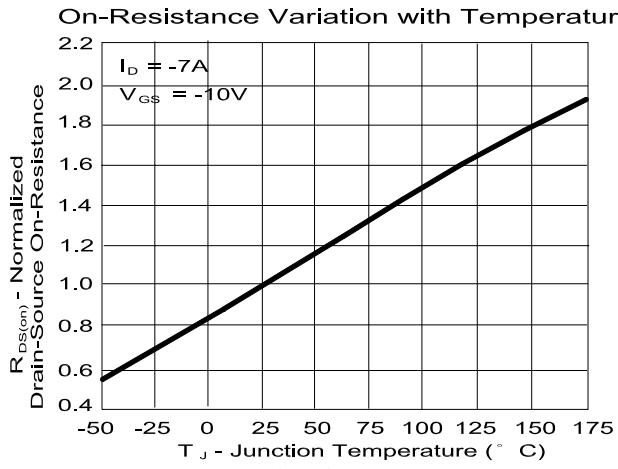
TYPICAL PERFORMANCE CHARACTERISTICS



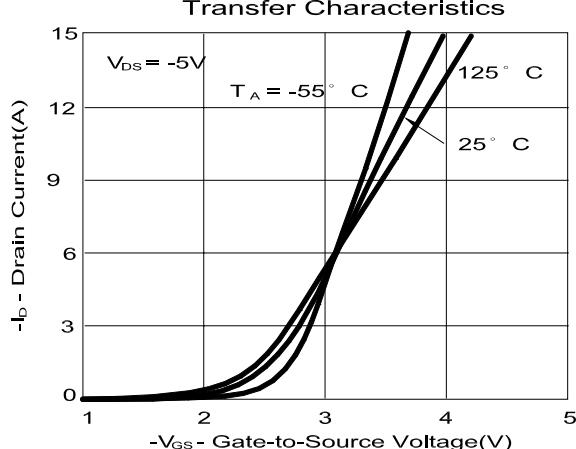
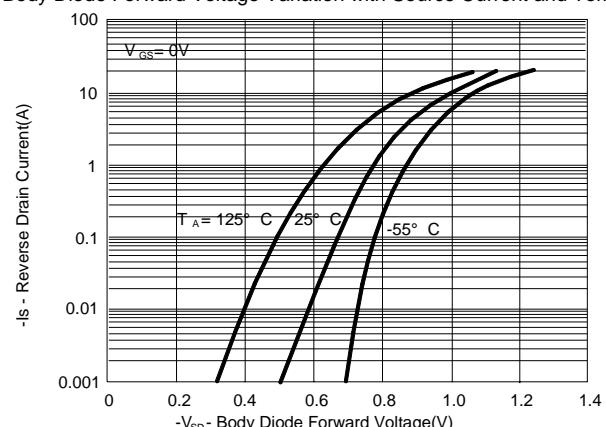
On-Resistance Variation with Drain Current and Gate Voltage



On-Resistance Variation with Temperature



Body Diode Forward Voltage Variation with Source Current and Temperature



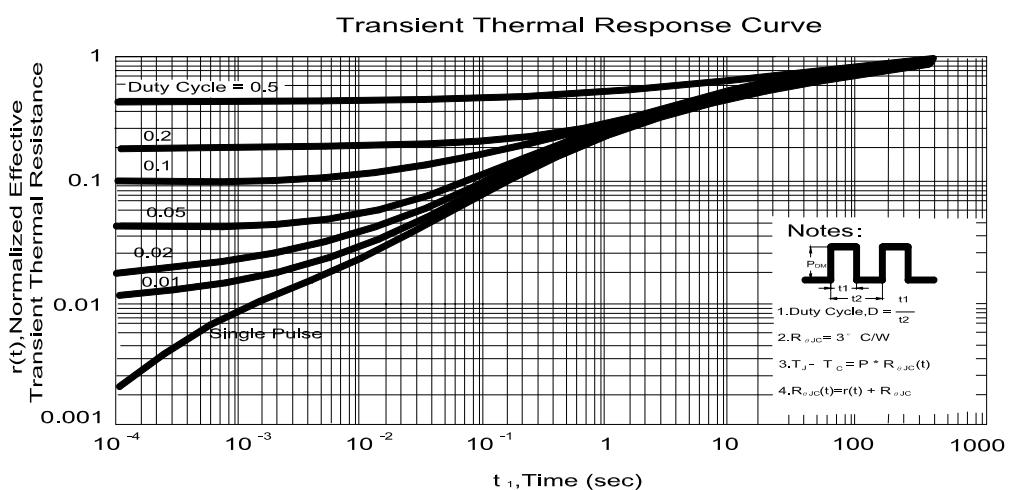
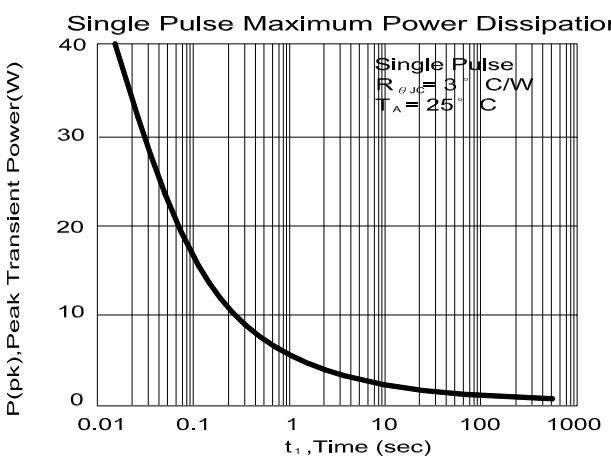
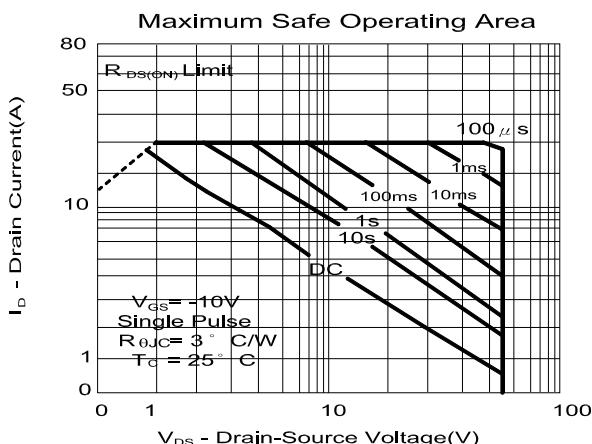
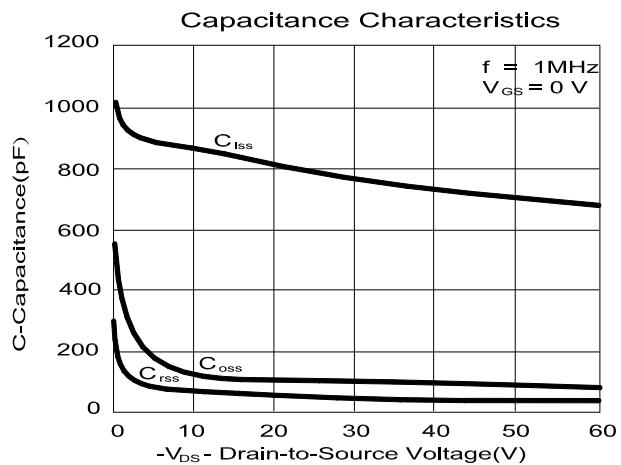
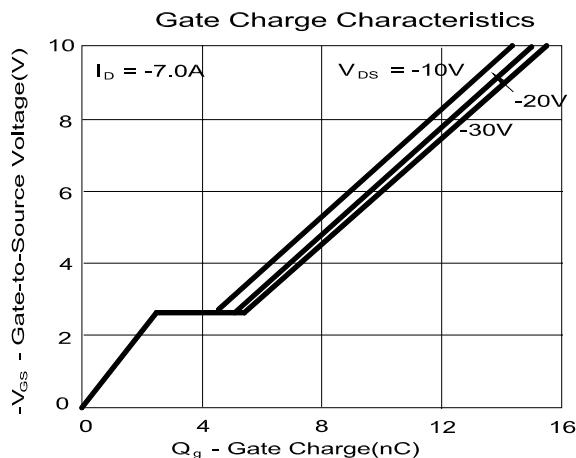
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TO-252 (DPAK) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	9.35		10.4	H	0.89		2.03
B	2.2		2.4	I	6.35		6.80
C	0.45		0.6	J	5.2		5.5
D	0.89		1.5	K	0.6		1
E	0.45		0.69	L	0.5		0.9
F	0.03		0.23	M	3.96	4.57	5.18
G	5.2		6.2	N			

