FUJITSU SEMICONDUCTOR
DATA SHEET

DS501-00003-0v01-E

Memory FRAM

CMOS

1 M Bit (128 K × 8)

MB85R1001A

■ DESCRIPTIONS

The MB85R1001A is an FRAM (Ferroelectric Random Access Memory) chip consisting of 131,072 words × 8 bits of nonvolatile memory cells created using ferroelectric process and silicon gate CMOS process technologies.

The MB85R1001A is able to retain data without using a back-up battery, as is needed for SRAM.

The memory cells used in the MB85R1001A can be used for 10^{10} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E^2PROM.

The MB85R1001A uses a pseudo-SRAM interface that is compatible with conventional asynchronous SRAM.

■ FEATURES

- Bit configuration : 131,072 words × 8 bits
- Read/write endurance : 10^{10} times
- Operating power supply voltage : 3.0 V to 3.6 V
- Operating temperature range : − 40 °C to + 85 °C
- Data retention : 10 years (+ 55 °C)
- Package : 48-pin plastic TSOP (1)

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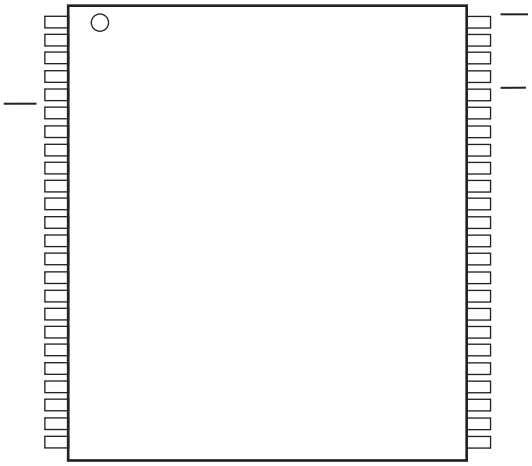
■ PIN ASSIGNMENTS

(TOP VIEW)

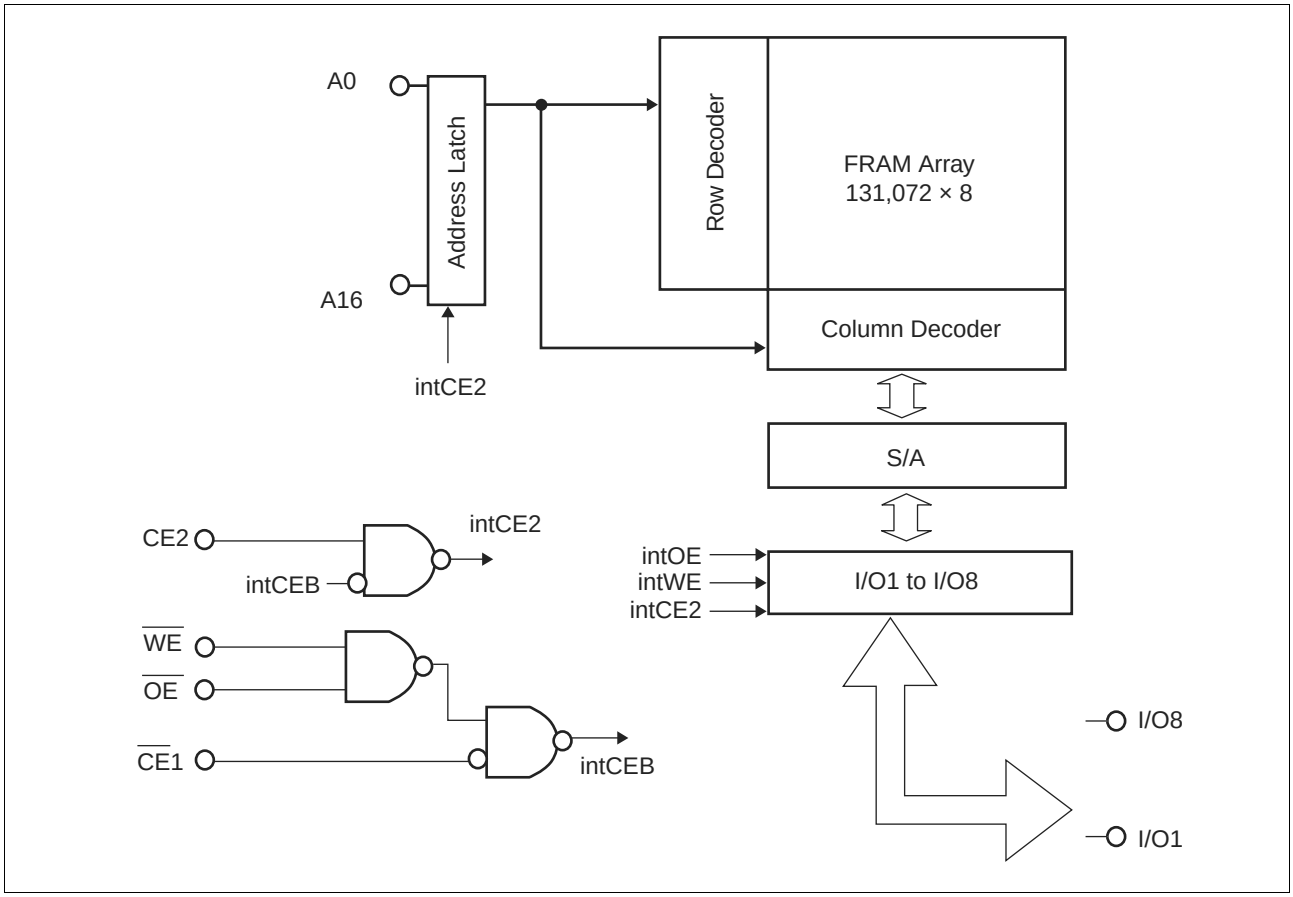


(FPT-48P-M48)

■ PIN DESCRIPTIONS

Pin Number	Pin Name	Functional Description
1, 2, 4, 5, 8, 18 to 26, 28, 29, 45	A0 to A16	Address Input pins
33 to 35, 38 to 42	I/O1 to I/O8	Data Input/Output pins
44	$\overline{CE}$1	Chip Enable 1 Input pin
7	CE2	Chip Enable 2 Input pin
6	$\overline{WE}$	Write Enable Input pin
48	$\overline{OE}$	Output Enable Input pin
10, 16, 37	VDD	Supply Voltage pins
13, 27, 46	VSS	Ground pins
3, 9, 11, 12, 14, 15, 17, 30 to 32, 36, 43, 47	NC	No Connect pins

■ BLOCK DIAGRAM



■ FUNCTIONAL TRUTH TABLE

Operation Mode	$\overline{CE}1$	CE2	$\overline{WE}$	$\overline{OE}$	I/O_1 to I/O_8	Supply Current
Standby Precharge	H	X	X	X	Hi-Z	Standby (I_{SB})
	X	L	X	X		
	X	X	H	H		
Read	↓ L	H ↑	H	L	Data Output	Operation (I_{CC})
Read (Pseudo-SRAM, $\overline{OE}$ control*1)	L	H	H	↓		
Write	↓ L	H ↑	L	H	Data Input	
Write (Pseudo-SRAM, $\overline{WE}$ control*2)	L	H	↓	H		

Note: L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, Hi-Z = High Impedance

↓ : Latch address and latch data at falling edge, ↑ : Latch address and latch data at rising edge

*1 : $\overline{OE}$ control of the Pseudo-SRAM means the valid address at the falling edge of $\overline{OE}$ to read.

*2 : $\overline{WE}$ control of the Pseudo-SRAM means the valid address and data at the falling edge of $\overline{WE}$ to write.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power Supply Voltage*	V_{CC}	– 0.5	+ 4.0	V
Input Pin Voltage*	V_{IN}	– 0.5	V_{CC} + 0.5 (≤ 4.0)	V
Output Pin Voltage*	V_{OUT}	– 0.5	V_{CC} + 0.5 (≤ 4.0)	V
Operating Temperature	T_A	– 40	+ 85	°C
Storage Temperature	Tstg	– 40	+ 125	°C

* : All voltages are referenced to VSS (ground 0 V).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage*	V_{CC}	3.0	3.3	3.6	V
High Level Input Voltage*	V_{IH}	$V_{CC} \times 0.8$	—	V_{CC} + 0.5(≤ 4.0)	V
Low Level Input Voltage*	V_{IL}	– 0.5	—	+ 0.6	V
Operating Temperature	T_A	– 40	—	+ 85	°C

* : All voltages are referenced to VSS (ground 0 V).

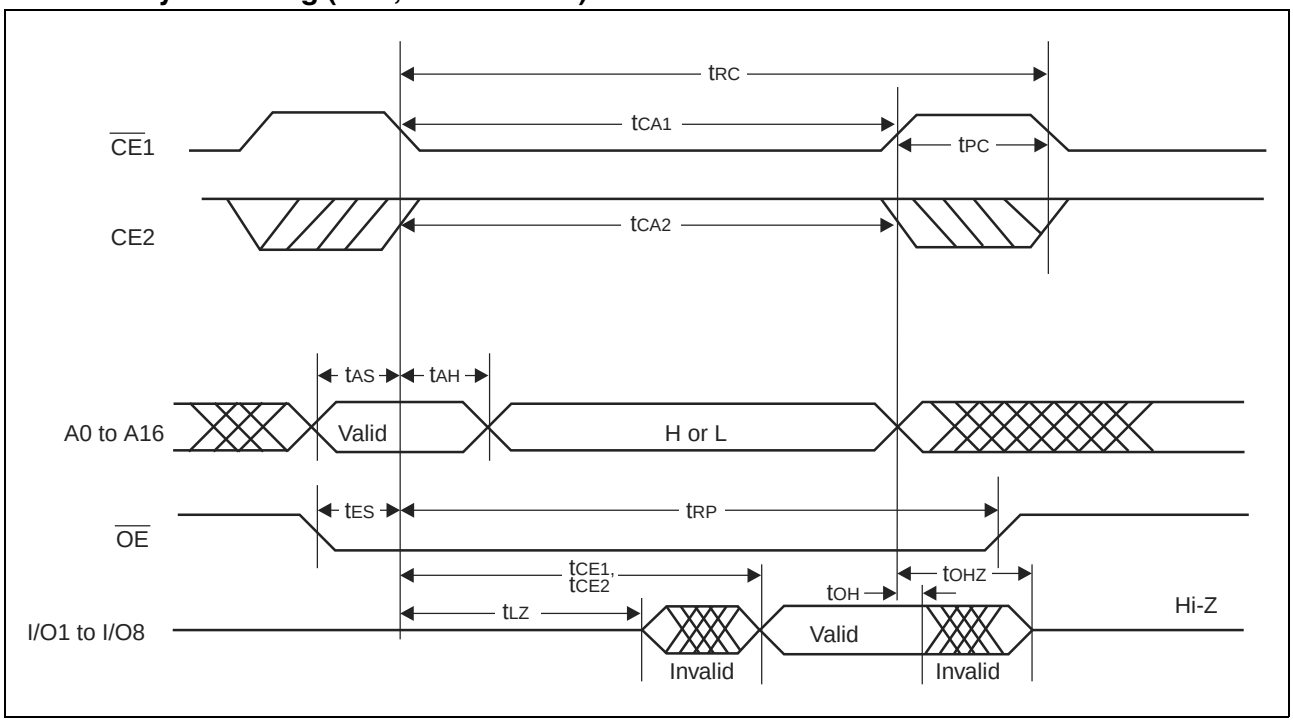
WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

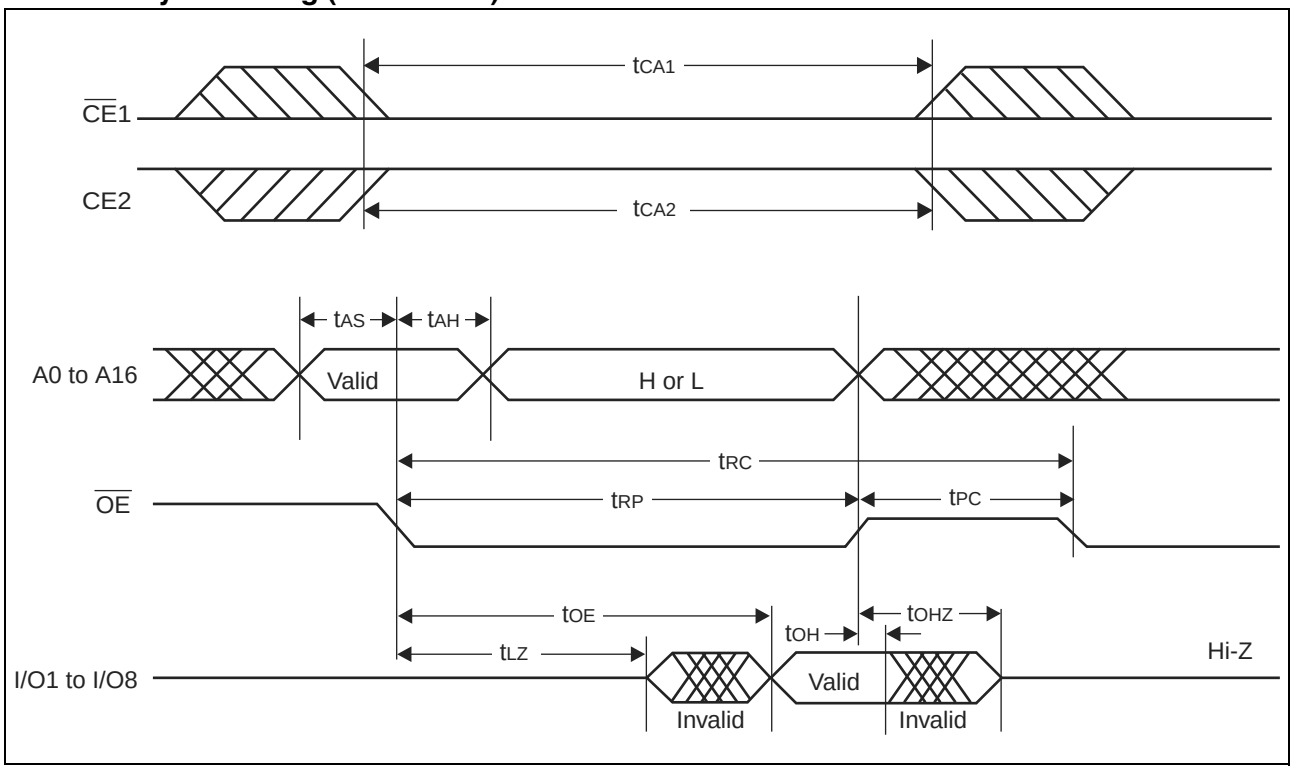
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ TIMING DIAGRAMS

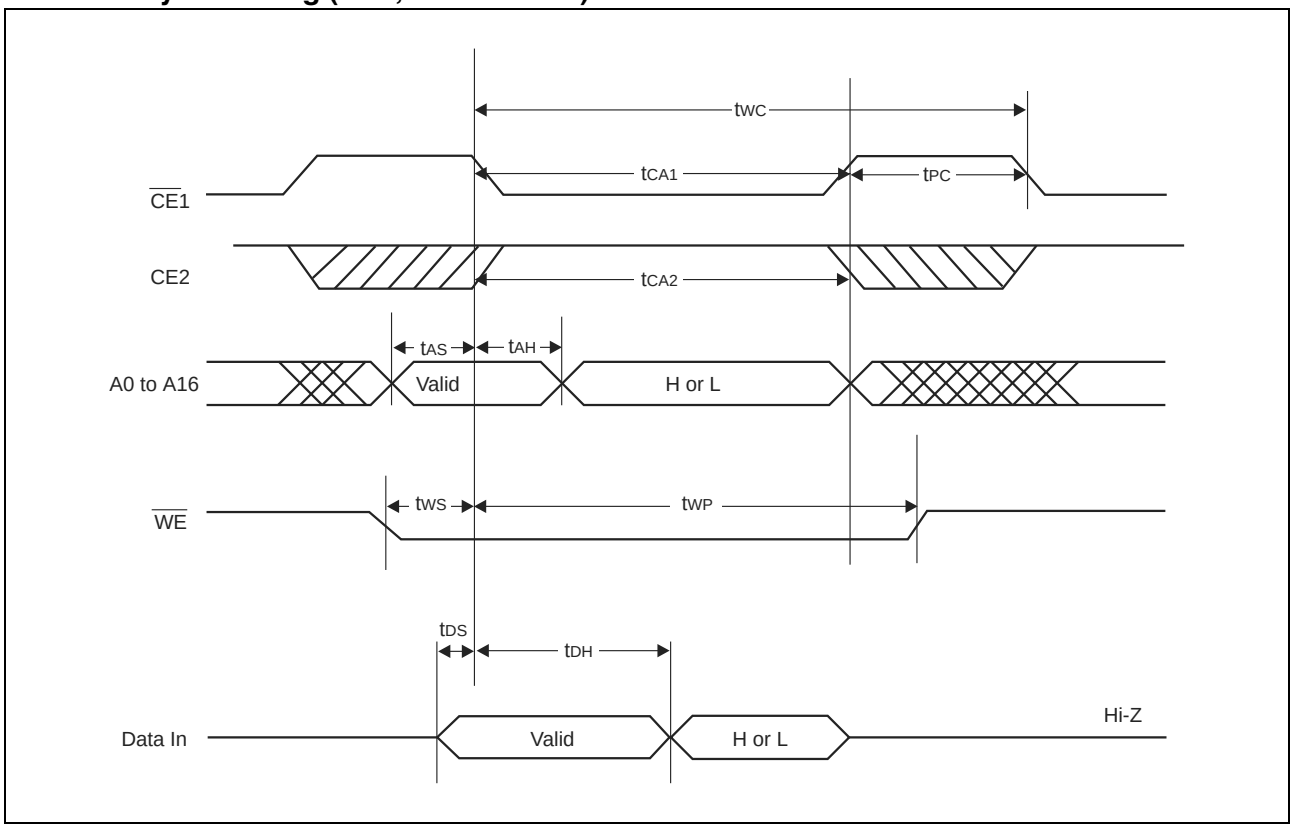
1. Read Cycle Timing ($\overline{CE}$1, CE2 Control)



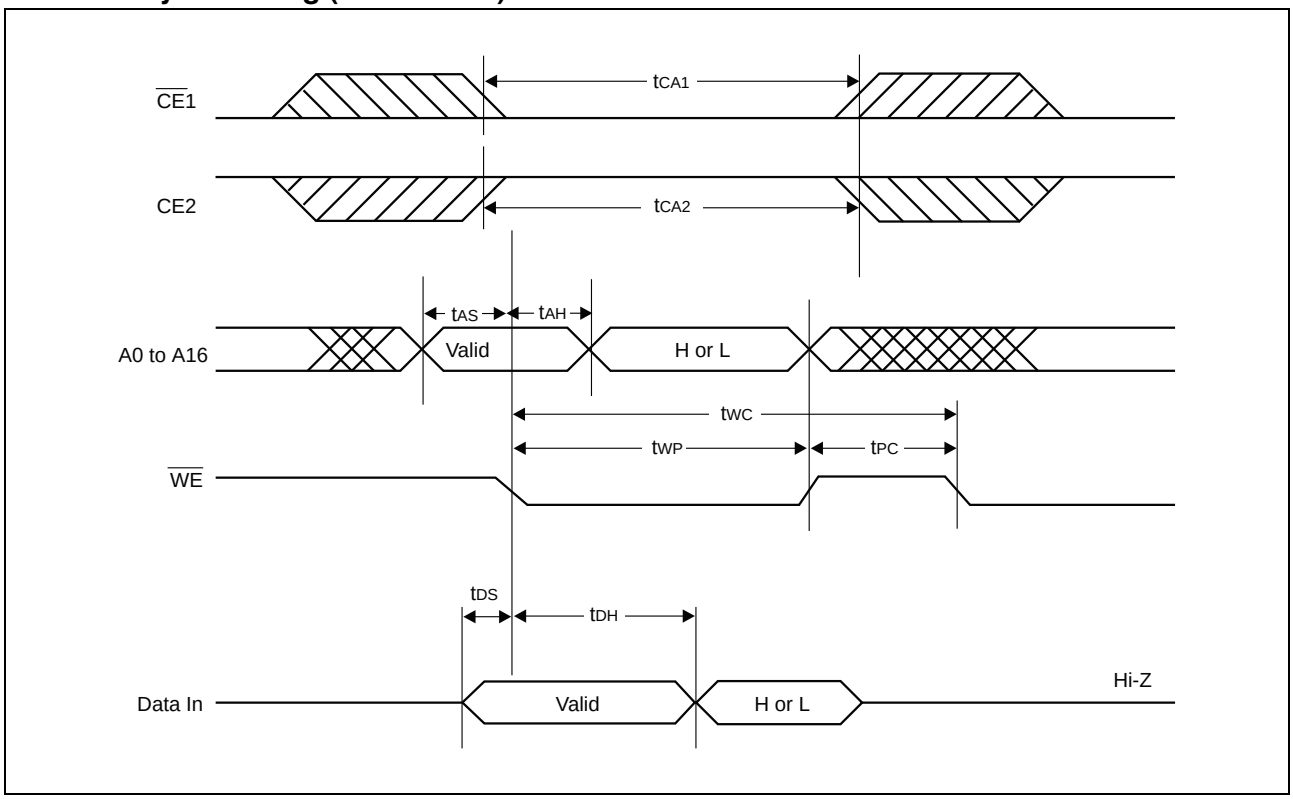
2. Read Cycle Timing ($\overline{OE}$ Control)



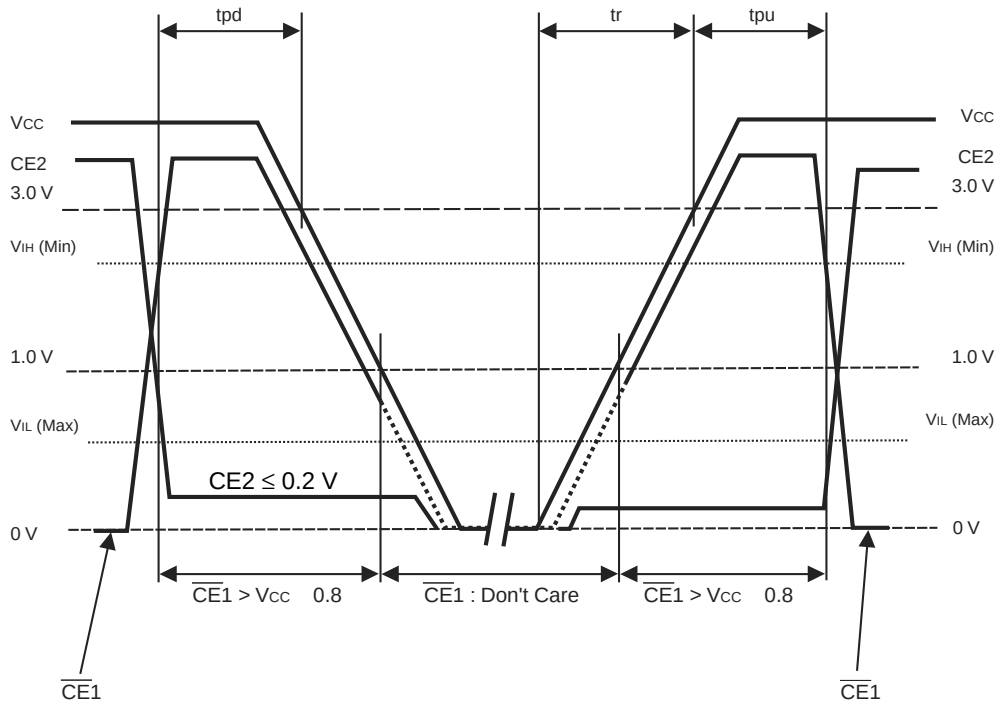
3. Write Cycle Timing ($\overline{CE}$1, CE2 Control)



4. Write Cycle Timing ($\overline{WE}$ Control)



■ POWER ON/OFF SEQUENCE



* : $\overline{CE1}$ (Max) < V_{CC} + 0.5 V

Notes: • Use either of $\overline{CE1}$ or CE2, or both for disable control of the device.

- Because turning the power-on from an intermediate level cause malfunction, when the power is turned on, V_{CC} is required to be started from 0 V.
- If the device does not operate within the specified conditions of read cycle, write cycle, power on/off sequence, memory data can not be guaranteed.
- When turning the power on or off, it is recommended that CE2 is connected to ground to prevent unexpected writing.

(within recommended operating conditions)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
$\overline{CE1}$ level hold time for Power OFF	t_{pd}	85	—	—	ns
$\overline{CE1}$ level hold time for Power ON	t_{pu}	85	—	—	ns
Power supply rising time	t_r	0.05	—	200	ms

■ NOTES ON USE

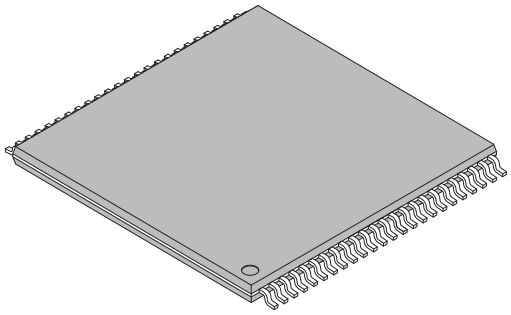
After the IR reflow completed, it is not guaranteed to save the data written prior to the IR reflow.

■ ORDERING INFOMATION

Part Number	Package
TBD	48-pin plastic TSOP(1) (FPT-48P-M48)

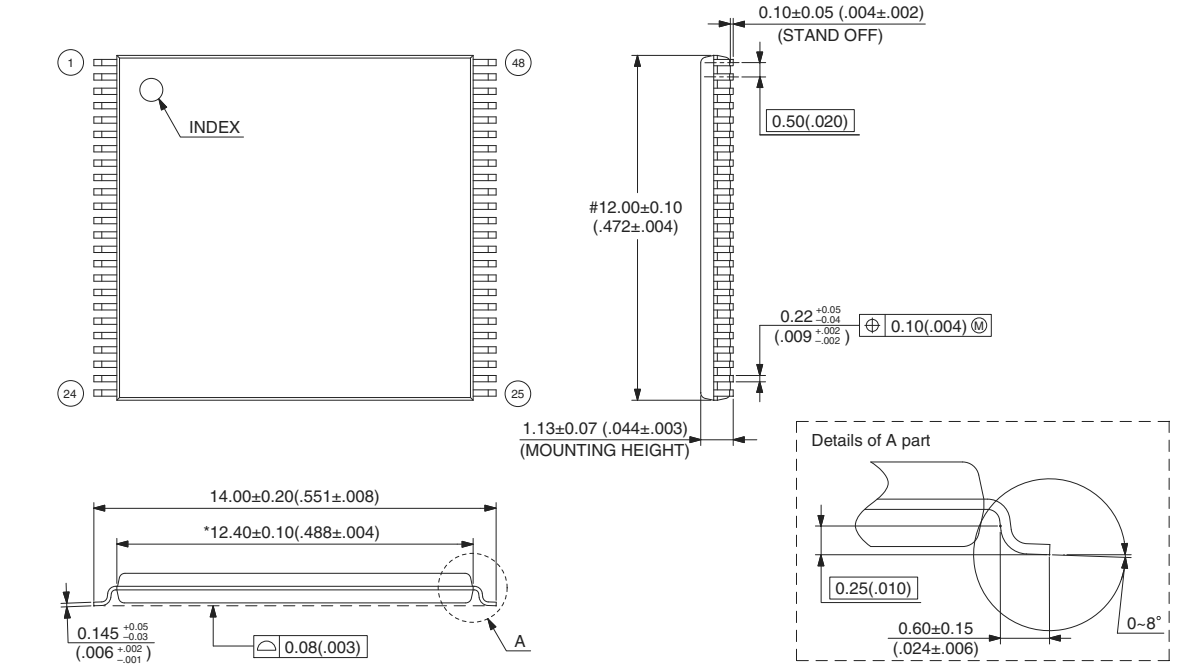
Note: Please confirm the ordering information with the sales representatives.

■ PACKAGE DIMENSIONS

48-pin plastic TSOP		
	Lead pitch	0.50 mm
	Package width × package length	12.00 mm × 12.40 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX
	Weight	0.36 g
(FPT-48P-M48)		

48-pin plastic TSOP
(FPT-48P-M48)

Note 1) # : Resin protrusion. (Each side : +0.15 (.006) Max).
Note 2) * : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

MEMO

MEMO

MEMO

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