PROCESS CP741V

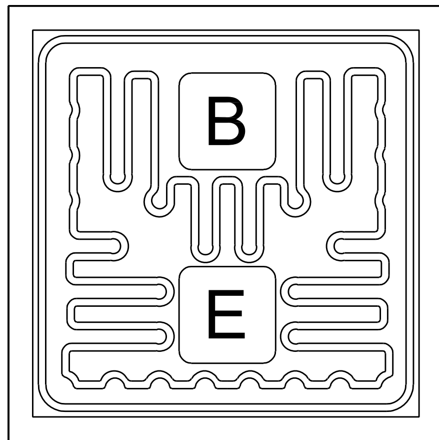
Small Signal Transistors

PNP - Low VCE(SAT) Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	17.7 x 17.7 MILS
Die Thickness	7.1 MILS
Base Bonding Pad Area	3.8 x 3.8 MILS
Emitter Bonding Pad Area	3.8 x 3.8 MILS
Top Side Metalization	Al-Si - 30,000Å
Back Side Metalization	Au - 12,000Å

GEOMETRY



BACKSIDE COLLECTOR R0

GROSS DIE PER 5 INCH WAFER

54,330

PRINCIPAL DEVICE TYPES

CMLT7410
CMPT7410
CMST7410
CMUT7410

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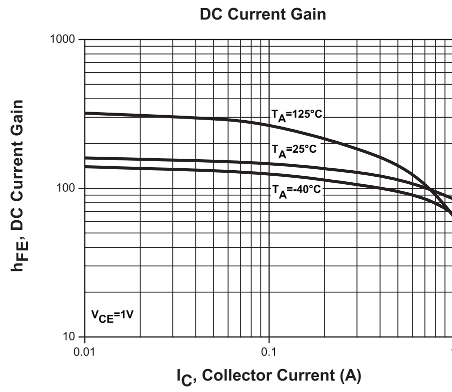
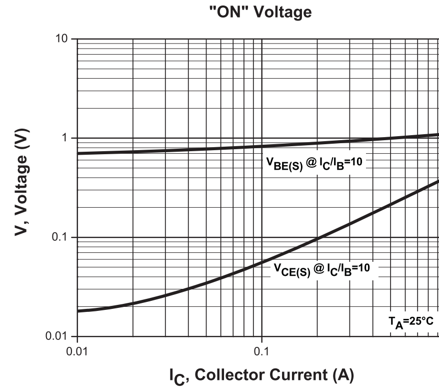
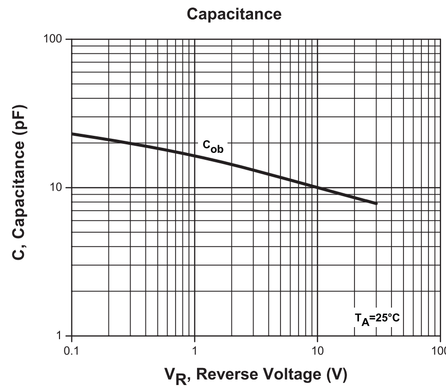
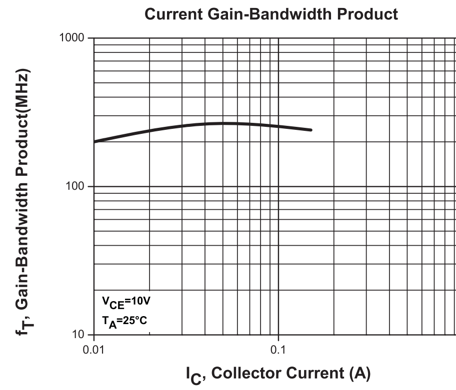
PROCESS CP741V

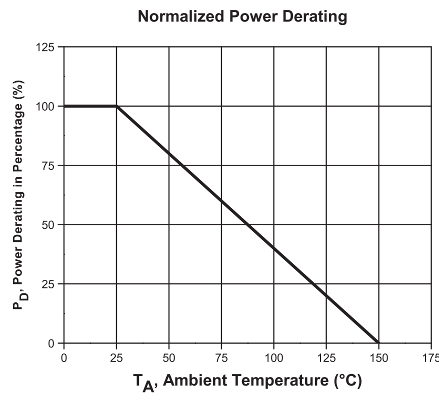
Typical Electrical Characteristics











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