PROCESS CP710

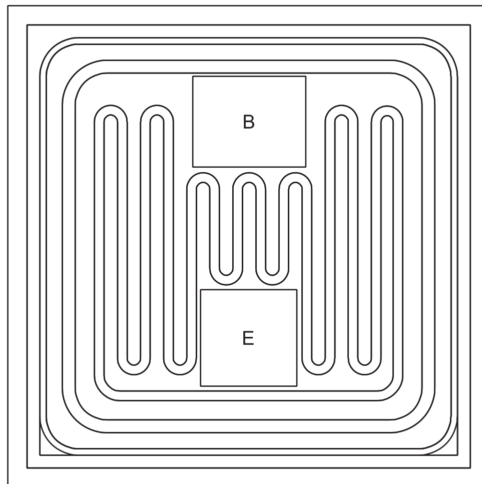
Small Signal Transistor

PNP - High Voltage Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	26 x 26 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	6.1 x 4.9 MILS
Emitter Bonding Pad Area	5.2 x 5.2 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



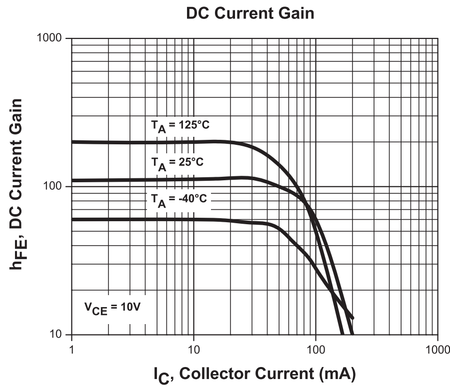
BACKSIDE COLLECTOR R2

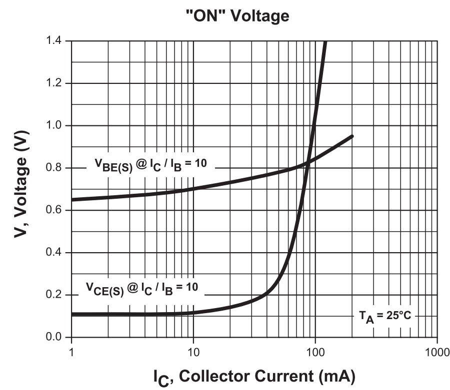
GROSS DIE PER 4 INCH WAFER
17,130

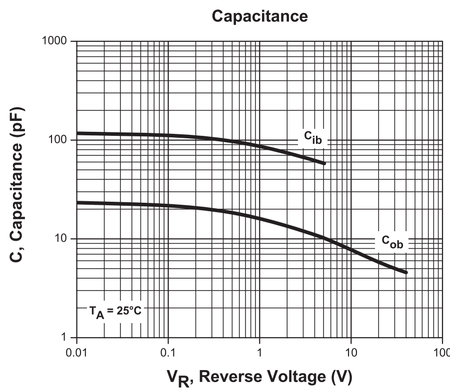
PRINCIPAL DEVICE TYPES
CMPTA94
CXTA94
CZTA94
MPSA94

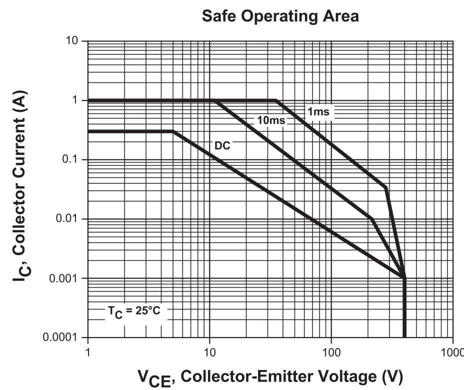
PROCESS CP710

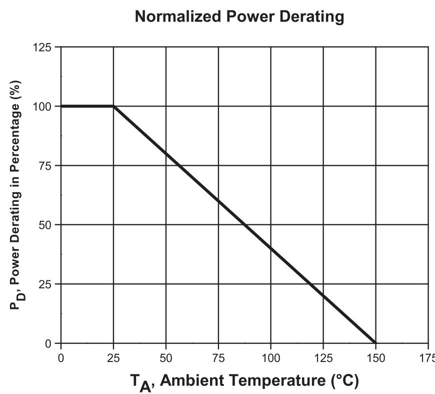
Typical Electrical Characteristics

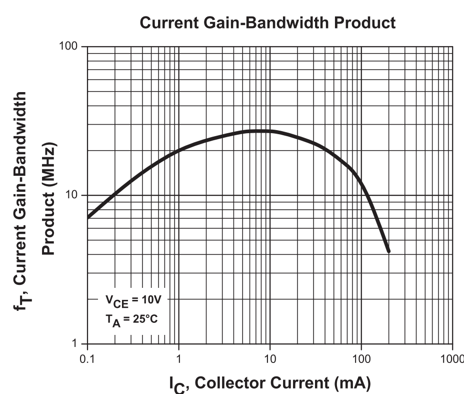












R5 (22-March 2010)