

1.5V Drive Pch+Pch MOSFET

TT8J1

●Structure

Silicon P-channel MOSFET

●Features

- 1) Low On-resistance.
- 2) High Power Package.
- 3) Low voltage drive. (1.5V)

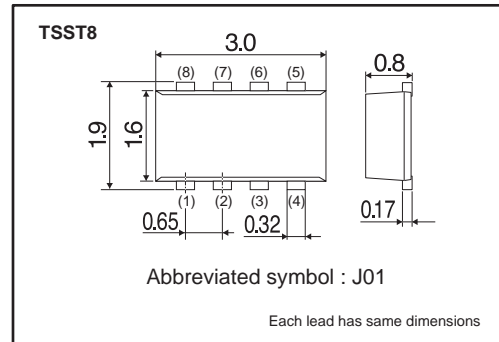
●Applications

Switching

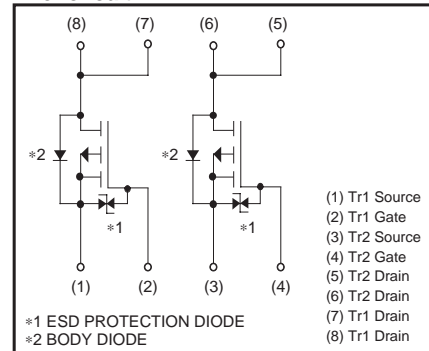
●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
TT8J1		○

●Dimensions (Unit : mm)



●Inner circuit



●Absolute maximum ratings (Ta=25°C)

<It is the same ratings for the Tr1 and Tr2.>

Parameter	Symbol	Limits	Unit
Drain-source voltage	V_{DS}	-12	V
Gate-source voltage	V_{GS}	± 10	V
Drain current	Continuous	I_D	± 2.5 A
	Pulsed	I_{DP} *1	± 10 A
Source current (Body diode)	Continuous	I_S	-0.8 A
	Pulsed	I_{SP} *1	-10 A
Total power dissipation	P_D *2	1.25	W / TOTAL
		1.0	W / ELEMENT
Channel temperature	T_{ch}	150	°C
Range of Storage temperature	T_{stg}	-55 to +150	°C

*1 $P_{ws} \leq 10 \mu s$, Duty cycles $\leq 1\%$

*2 Mounted on a ceramic board

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th(ch-a)}$ *	100	°C / W / TOTAL
		125	°C / W / ELEMENT

* Mounted on a ceramic board

●Electrical characteristics (Ta=25°C)

<It is the same characteristics for the Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	-	-	±10	μA	V _{GS} =±10V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR) DSS}	-12	-	-	V	I _D = -1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	-	-	-1	μA	V _{DS} = -12V, V _{GS} =0V
Gate threshold voltage	V _{GS(th)}	-0.3	-	-1.0	V	V _{DS} = -6V, I _D = -1mA
Static drain-source on-state resistance	R _{DS(on)} *	-	44	61	mΩ	I _D = -2.5A, V _{GS} = -4.5V
		-	60	84	mΩ	I _D = -1.2A, V _{GS} = -2.5V
		-	81	121	mΩ	I _D = -1.2A, V _{GS} = -1.8V
		-	110	220	mΩ	I _D = -0.5A, V _{GS} = -1.5V
Forward transfer admittance	Y _{fs} *	3.5	-	-	S	V _{DS} = -6V, I _D = -2.5A
Input capacitance	C _{iss}	-	1350	-	pF	V _{DS} = -6V
Output capacitance	C _{oss}	-	130	-	pF	V _{GS} =0V
Reverse transfer capacitance	C _{rss}	-	125	-	pF	f=1MHz
Turn-on delay time	t _{d(on)} *	-	9	-	ns	V _{DD} ≒ -6V
Rise time	t _r *	-	35	-	ns	V _{GS} = -4.5V
Turn-off delay time	t _{d(off)} *	-	130	-	ns	I _D = -1.2A
Fall time	t _f *	-	85	-	ns	R _L ≒ 5Ω
Total gate charge	Q _g *	-	13	-	nC	R _G =10Ω
Gate-source charge	Q _{gs} *	-	2.5	-	nC	V _{DD} ≒ -6V
Gate-drain charge	Q _{gd} *	-	2.0	-	nC	V _{GS} = -4.5V
						I _D = -2.5A
						R _L ≒ 2.4Ω / R _G =10Ω

* Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V _{SD} *	-	-	-1.2	V	I _S = -2.5A, V _{GS} =0V

* Pulsed

●Electrical characteristic curves

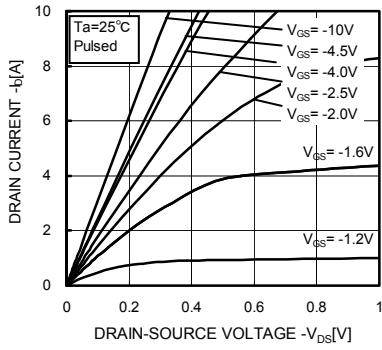


Fig.1 Typical Output Characteristics(I)

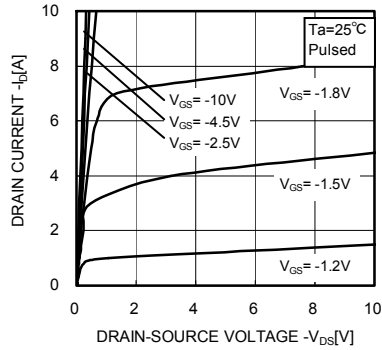


Fig.2 Typical Output Characteristics(II)

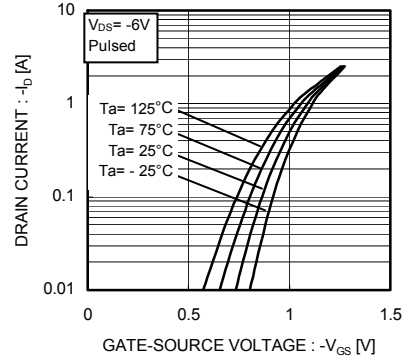


Fig.3 Typical Transfer Characteristics

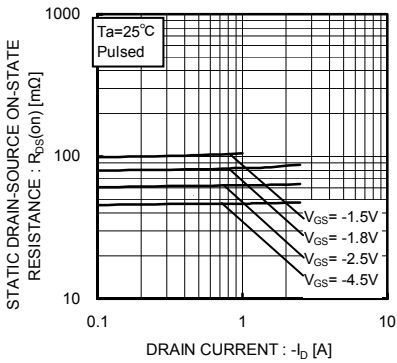


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

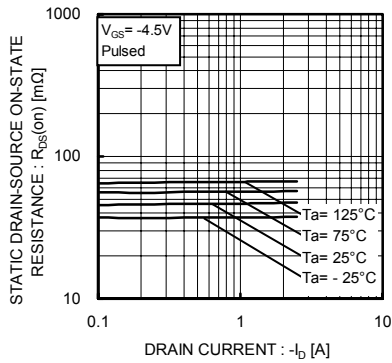


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

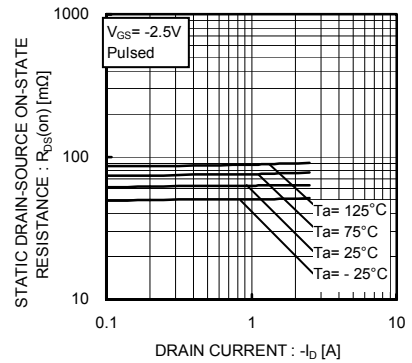


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

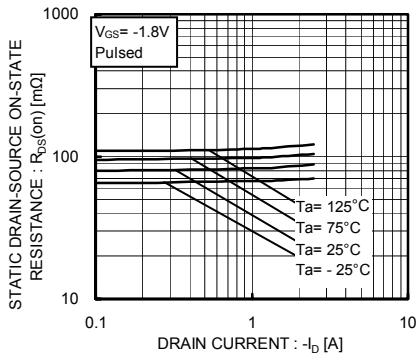


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

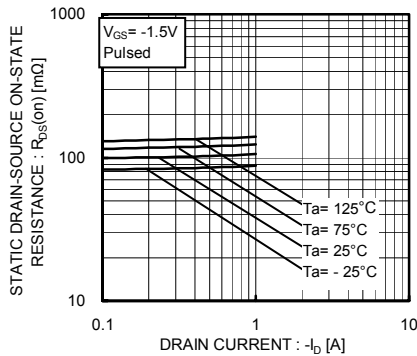


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(V)

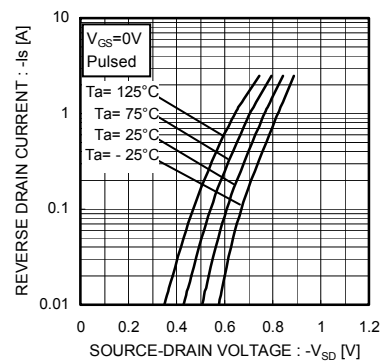


Fig.9 Reverse Drain Current vs. Source-Drain Voltage

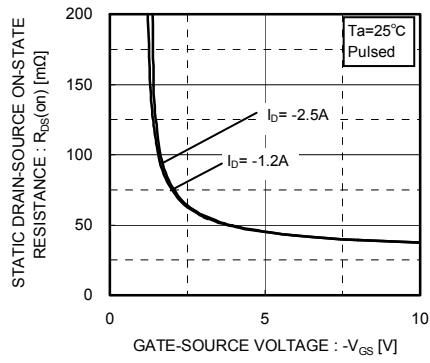


Fig.10 Static Drain-Source On-State Resistance vs. Gate Source Voltage

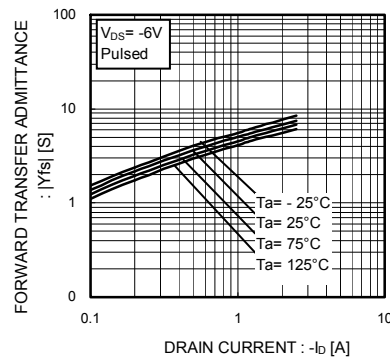


Fig.11 Forward Transfer Admittance vs. Drain Current

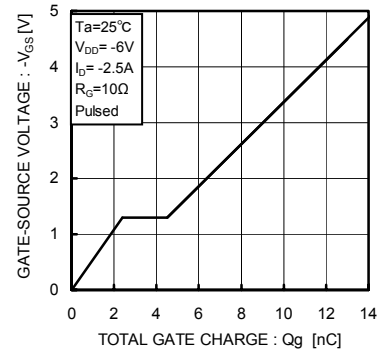


Fig.12 Dynamic Input Characteristics

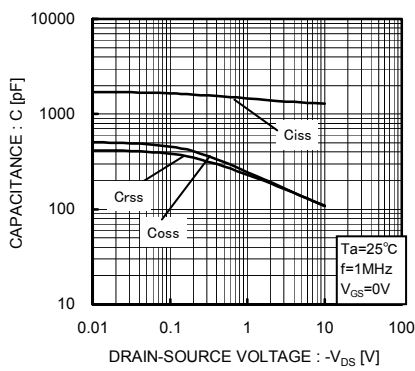


Fig.13 Typical Capacitance vs. Drain-Source Voltage

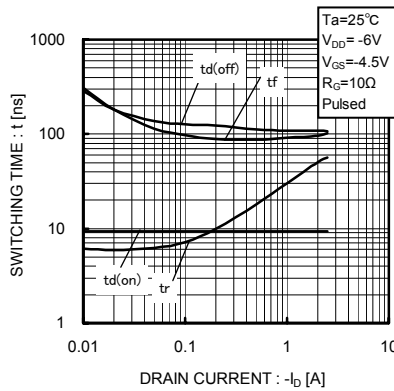


Fig.14 Switching Characteristics

●Measurement circuits

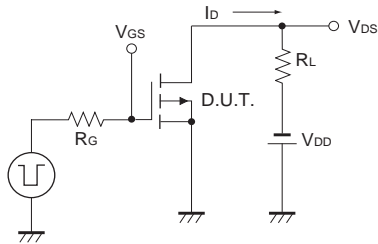


Fig.1-1 Switching Time Measurement Circuit

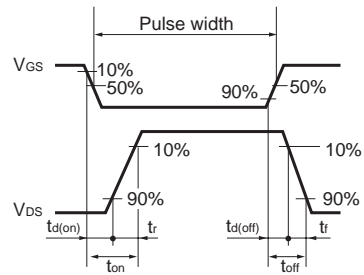


Fig.1-2 Switching Waveforms

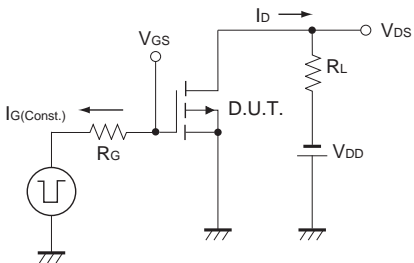


Fig.2-1 Gate Charge Measurement Circuit

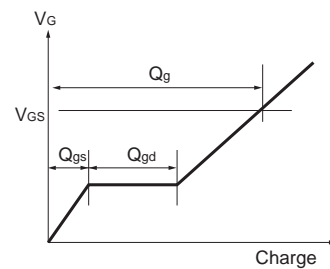


Fig.2-2 Gate Charge Waveform

●Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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