

44-V, 5.5-A, quad power half-bridge

Features

- Minimum input/output pulse width distortion
- 150 mΩ R_{dsON} complementary DMOS output stage
- CMOS compatible logic inputs
- Thermal protection
- Thermal warning output
- Undervoltage protection
- No power-on, power-off sequence required

Description

The STA510F is a monolithic, quad, half-bridge stage in multipower BCD technology. The device can be used as dual-bridge or reconfigured, by connecting the CONFIG pin to the V_{dd} pin, as single-bridge with double current capability, and as half-bridge (binary mode) with half current capability.



The device is particularly designed to make the output stage of a stereo all-digital high-efficiency (FFX) amplifier capable of delivering 100 W + 100 W output power into 8-Ω loads with THD = 10% and V_{CC} = 39 V. In single BTL configuration the device can deliver 200 W into a 4-Ω load with THD = 10% and V_{CC} = 39 V.

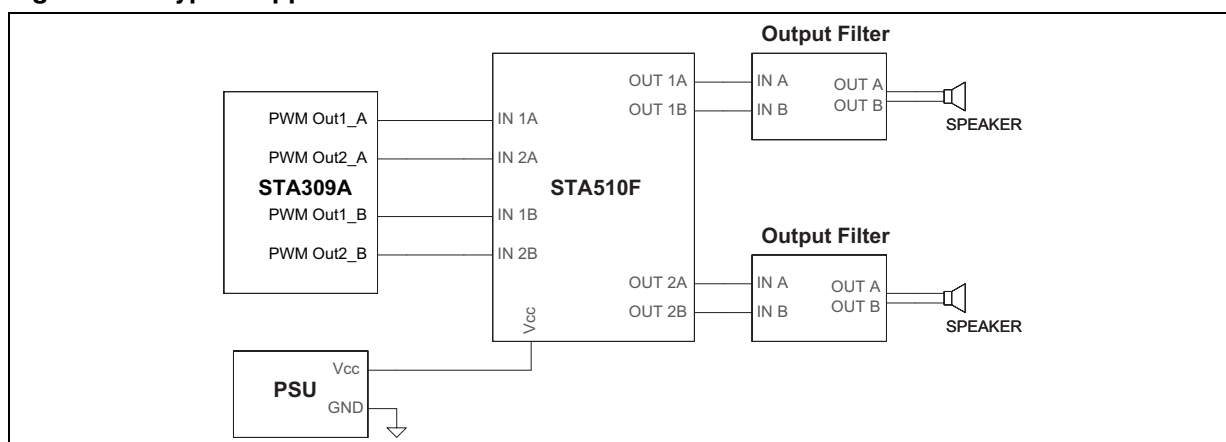
The device is fully compatible with the DDX[®] driver device.

The input pins have a threshold proportional to V_L pin voltage.

Table 1. Device summary

Order code	Operating temp. range	Package	Packing
STA510F	0° to 70° C	PowerSSO36 (slug up)	Tube
STA510FTR	0° to 70° C	PowerSSO36 (slug up)	Tape & Reel

Figure 1. Typical application



1 Pin description

Figure 2. Pin connections (top view)

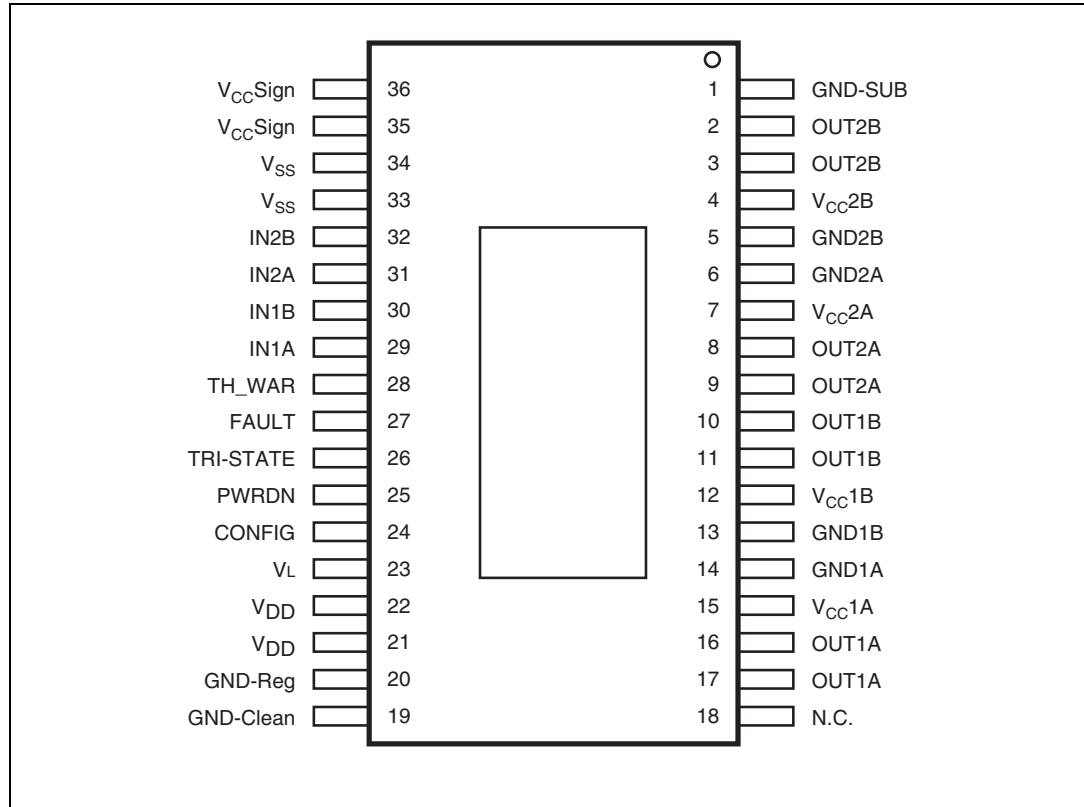


Table 2. Pin list

Pin	Name	Description
1	GND-SUB	Substrate ground
2, 3	OUT2B	Output half-bridge 2B
4	Vcc2B	Positive supply
5	GND2B	Negative supply
6	GND2A	Negative supply
7	Vcc2A	Positive supply
8, 9	OUT2A	Output half-bridge 2A
10, 11	OUT1B	Output half-bridge 1B
12	Vcc1B	Positive supply
13	GND1B	Negative supply
14	GND1A	Negative supply
15	Vcc1A	Positive supply
16, 17	OUT1A	Output half-bridge 1A

Table 2. Pin list (continued)

Pin	Name	Description
18	NC	Not connected
19	GND-clean	Logical ground
20	GND-Reg	Ground for regulator Vdd
21, 22	Vdd	5-V regulator referred to ground
23	V _L	High logical state setting voltage
24	CONFIG	Configuration
25	PWRDN	Standby
26	TRI-STATE	Hi-Z
27	FAULT	Fault pin advisor
28	TH-WAR	Thermal warning advisor
29	IN1A	Input of half-bridge 1A
30	IN1B	Input of half-bridge 1B
31	IN2A	Input of half-bridge 2A
32	IN2B	Input of half-bridge 2B
33, 34	Vss	5-V regulator referred to +Vcc
35, 36	VCCSIGN	Signal positive supply

Table 3. Pin values

Pin	Logical value	Device status
FAULT ⁽¹⁾	0	Fault detected (short-circuit, or thermal)
	1	Normal operation
TRI-STATE	0	All power stages in Hi-Z state
	1	Normal operation
PWRDN	0	Low-power mode
	1	Normal operation
THWAR ⁽¹⁾	0	Temperature of the IC = 130° C
	1	Normal operation
CONFIG ⁽²⁾	0	Normal operation
	1	OUT1A = OUT1B, OUT2A = OUT2B (IF IN1A = IN1B and IN2A = IN2B)

1. The pin is open collector. To have the high logic value, it needs a pull-up resistor.
2. CONFIG = 1 means connect pin 24 (CONFIG) to pins 21, 22 (Vdd).

2 Electrical specifications

2.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CC}	DC supply voltage (pin 4, 7, 12, 15)	44	V
V _{max}	Maximum voltage on pins 23 to 32	5.5	V
ESD	Max ESD on pins (HBM)	±1000	V
T _{op}	Operating temperature range	0 to 70	°C
T _{stg} , T _j	Storage and junction temperature	-40 to 150	°C

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
T _{j-case}	Thermal resistance junction to case (thermal pad)		1	2.5	°C/W
T _{jSD}	Thermal shut-down junction temperature		150		°C
T _{warn}	Thermal warning temperature		130		°C
t _{hSD}	Thermal shutdown hysteresis		25		°C

2.3 Electrical specifications

The results in [Table 6](#) below are given for the conditions: V_L = 3.3 V, V_{cc} = 37 V and T = 25° C unless otherwise specified.

Table 6. Electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R _{dsON}	Power Pchannel/Nchannel MOSFET RdsON	I _d = 1 A		150	200	mΩ
I _{dss}	Power Pchannel/Nchannel leakage current				100	μA
g _N	Power Pchannel RdsON matching	I _d = 1 A	95			%
g _P	Power Nchannel RdsON matching	I _d = 1 A	95			%
Dt _s	Low current deadtime (static)	see test circuit Figure 3		10	20	ns
Dt _d	High current deadtime (dynamic)	L = 22 μH, C = 470 nF, R _L = 8 Ω, I _d = 4.5 A, see test circuit Figure 4			50	ns
t _{d ON}	Turn-on delay time	Resistive load			100	ns

Table 6. Electrical specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{d\ OFF}$	Turn-off delay time	Resistive load			100	ns
t_r	Rise time	Resistive load, as Figure 4			25	ns
t_f	Fall time	Resistive load, as Figure 4			25	ns
V_{CC}	Supply voltage operating voltage		10		40	V
$V_{IN-High}$	High level input voltage		$V_L/2 + 300mV$			V
V_{IN-Low}	Low level input voltage				$V_L/2 - 300mV$	V
I_{IN-H}	High level input current	Pin voltage = V_L		1		μA
I_{IN-L}	Low level input current	Pin voltage = 0.3 V		1		μA
$I_{PWRDN-H}$	High level PWRDN pin input current	$V_L = 3.3 V$		35		μA
V_{Low}	Low logical state voltage (pins PWRDN, TRISTATE) (see Table 7)	$V_L = 3.3 V$			0.8	V
V_{High}	High logical state voltage (pins PWRDN, TRISTATE) (see Table 7)	$V_L = 3.3 V$	1.7			V
$I_{VCC-PWRDN}$	Supply current from Vcc in power down	PWRDN = 0			3	mA
I_{FAULT}	Output current pins FAULT -TH-WARN when FAULT CONDITIONS	Vpin = 3.3 V		1		mA
$I_{VCC-hiz}$	Supply current from Vcc in tri-state	Pin TRI-STATE = 0		22		mA
I_{VCC}	Supply current from Vcc in operation both channel switching)	Input pulse width duty cycle = 50%, switching frequency = 384 kHz, no LC filters;		70		mA
I_{OUT-SH}	Overcurrent protection threshold I _{sc} (short-circuit current limit)		5.5	7	9	A
V_{UV}	Undervoltage protection threshold			7		V
t_{pw_min}	Output minimum pulse width	No load	25		40	ns

Table 7. V_{Low} , V_{High} threshold variation with V_L

V_L	$V_{Low\ max}$	$V_{High\ min}$	Unit
2.7	0.7	1.5	V
3.3	0.8	1.7	V
5	0.85	1.85	V

Table 8. Logic truth table

TRI-STATE	INxA	INxB	Q1	Q2	Q3	Q4	Output mode
0	x	x	OFF	OFF	OFF	OFF	Hi-Z
1	0	0	OFF	OFF	ON	ON	DUMP
1	0	1	OFF	ON	ON	OFF	NEGATIVE
1	1	0	ON	OFF	OFF	ON	POSITIVE
1	1	1	ON	ON	OFF	OFF	Not used

Figure 3. Test circuit for low current deadtime

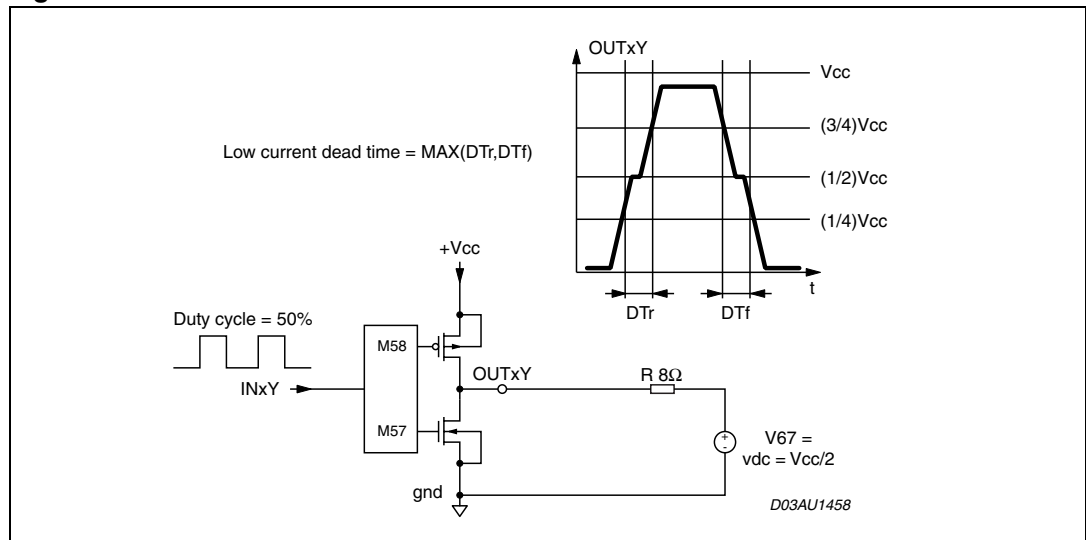


Figure 4. Test circuit for high current deadtime

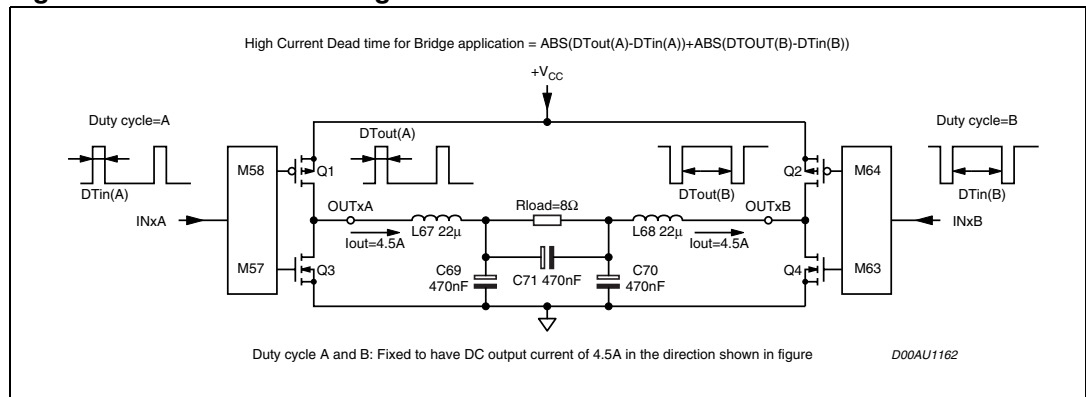


Figure 5. Typical quad half-bridge configuration giving 200 W per channel into 4 Ω speakers, 10% THD, V_{CC} = 39 V

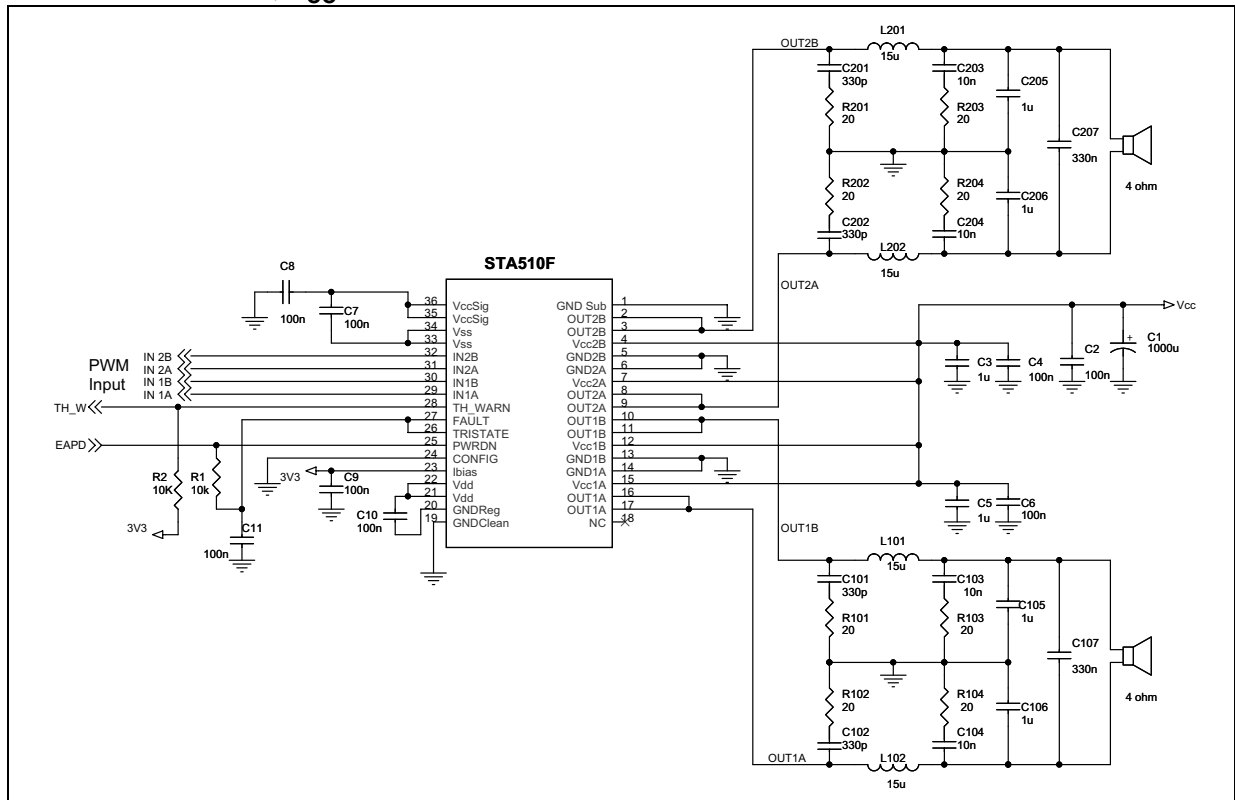
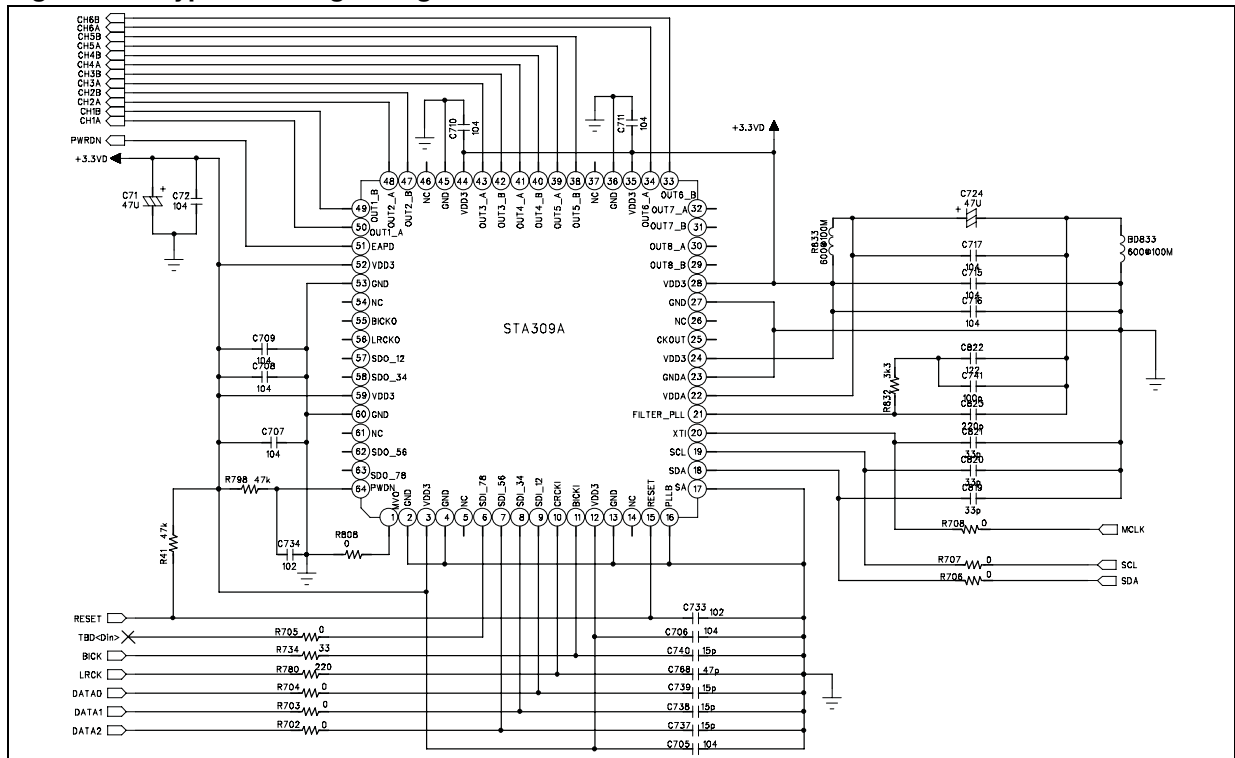


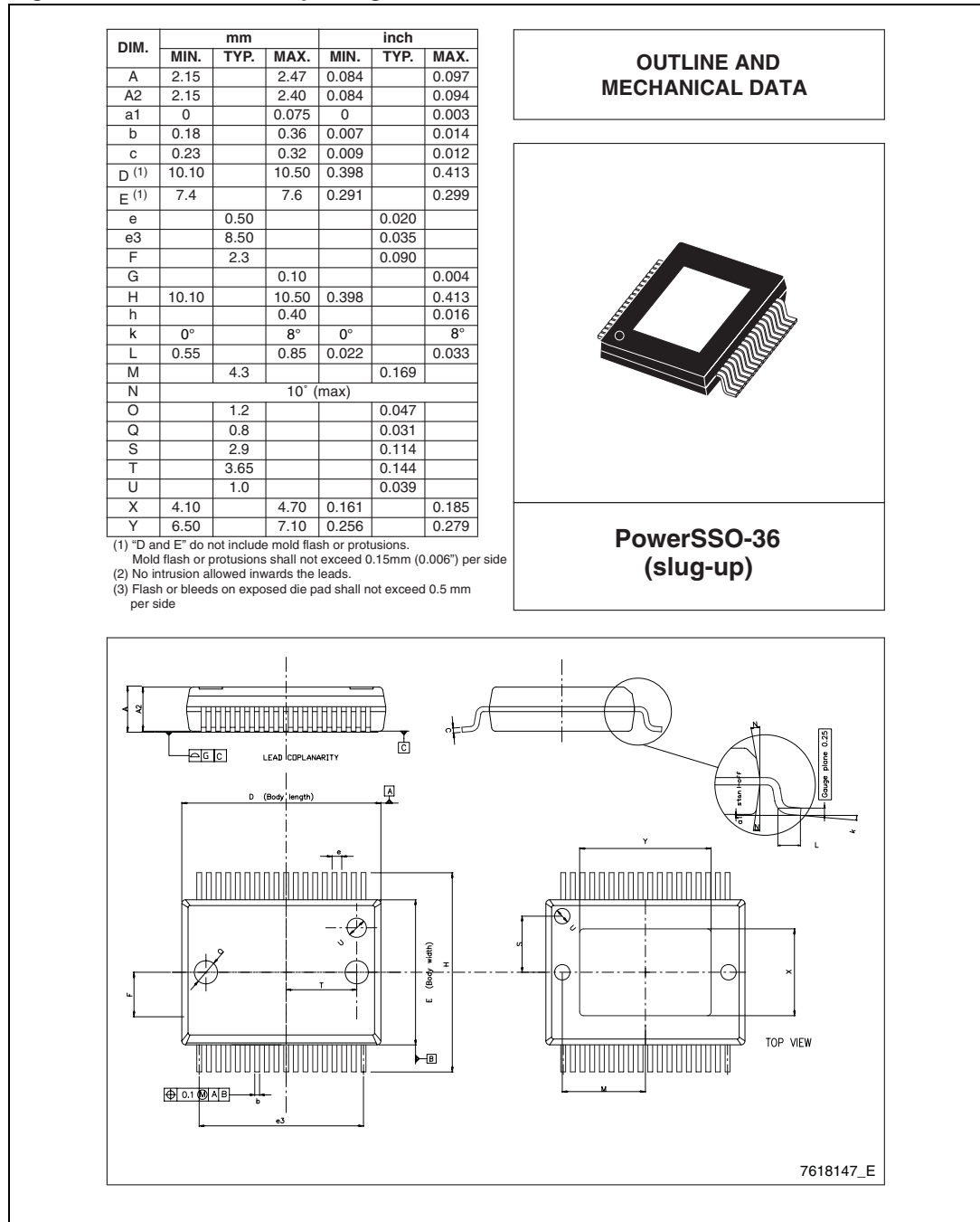
Figure 6. Typical driving configuration with STA309A



3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 7. PowerSSO36 package dimensions



4 Trademarks and other acknowledgements

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5 Revision history

Table 9. Document revision history

Date	Revision	Changes
13-Dec-2007	1	Initial release.
28-Jun-2011	2	Added part number STA510FTR to Table 1: Device summary Updated ECOPACK® text in Section 3: Package information Minor textual updates
02-Sep-2011	3	Updated package to PowerSSO36 throughout datasheet Corrected typographical error in Features Updated Figure 1: Typical application Updated Figure 2: Pin connections (top view) Updated Figure 6: Typical driving configuration with STA309A Updated Figure 7: PowerSSO36 package dimensions

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