

Version: 0.3

TECHNICAL SPECIFICATION

MODEL NO : PD035QU2

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Customer•s Confirmation

Customer

Date

FOR MORE INFORMATION:

Bу

PVI-s Confirmation

AZ DISPLAYS, INC. 75 COLUMBIA, ALISO VIEJO, CA 92656 Http://www.AZDISPLAYS.com

Confirmed By	Emmy Chang
Prepared By	曹耀霆



Revision History

Rev.	Issued Date	Revised Contents
0.1	Sep.15.2008	Preliminary
0.2	Sep.19.2008	Modify
		Page5: 4. Mechanical Drawing of TFT-LCD Module
0.3	Sep.30.2008	Modify
		Page 9
		7-2) Recommended Driving Condition for Back Light

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1. Application

This data sheet applies to a color TFT LCD module,PD035QU2.This module applies to OA product, which requires high quality flat panel display. If you must use in severe reliability environments, please don't extend over PVI's reliability test conditions.

2. Features

- . Amorphous silicon TFT LCD panel with LED back-light unit
- . Pixel in stripe configuration
- . Slim and compact, designed for O/A application

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	3.45 (diagonal)	inch
Display Format	320×(RGB)×240	dot
Active Area	70.08(H)×52.56(V)	mm
Pixel Pitch	0.073(H)×0.219(V)	mm
Pixel Configuration	Stripe	
Display Colors	16.7M	
Surface Treatment	Haze 20%	
Back-light	6-LEDs	
Outline Dimension	76.9(W)×63.9 (H)×2.8 (D)(typ.)	mm
Weight	(31)	g
Display mode	Normally white	
Grav scale inversion direction	6	o'clock
	(ref to Note 14-1)	UCIUCK

4. Mechanical Drawing of TFT-LCD Module



5. Input / Output Terminals

Pin No.	Symbol Function		Remark
1	VBL-	Backlight LED Ground	
2	VBL-	Backlight LED Ground	
3	VBL+	Backlight LED Power	
4	VBL+	Backlight LED Power	
5	Y1	Top electrode	
6	X1	Right electrode	
7	NC	Note Use	
8	/RESET	Hardware Reset	
9	SPENA	SPI Interface Data Enable Signal	Note 5-3
10	SPCLK	SPI Interface Data Clock	Note 5-3
11	SPDAT	SPI interface Data	Note 5-3
12	B0	Blue Data Bit 0	11010 0 0
13	B1	Blue Data Bit 1	
14	B2	Blue Data Bit 2	
15	B3	Blue Data Bit 2	
16	B4	Blue Data Bit 4	
17	B5	Blue Data Bit 5	
18	B6	Blue Data Bit 6	
10	B7	Blue Data Bit 7	
20	GO	Green Data Bit	
20	G0	Green Data Bito	
21		Green Data Bit 1	
22	62	Green Data Bit 2	
23	G3	Green Data Bit 3	
24	G4	Green Data Bit 4	
20	GS	Green Data Bit 6	
20	Go	Green Data Bit 6	
21		Green Data Bit 7	Noto 5.4
20		Red Data Bit 0 / DX 0	Note 5-4
29		Red Data Bit 1/ DX 1	Note 5-4
30	RZ	Red Data Bit 2/ DX 2	Note 5-4
31	R3	Red Data Bit 3/ DX 3	Note 5-4
32	R4	Red Data Bit 4/ DX 4	Note 5-4
33	RD DC	Red Data Bit 5/ DX 5	Note 5-4
34		Red Data Bit 6/ DX 6	Note 5-4
35		Red Data Bit // DX /	Note 5-4
30		Honzonial Sync Input	
37	VSTNC	Det Dete Cleak	
38		Dot Data Clock	
39		Not Use	
40		Not Use	
41	VCC	Digital Power	
42		Digital Power	
43	۲ <u>۲</u>	BOTTOM Electrode	
44	72 NO		
45		Internal test use	
46			
4/			
48	SEL2	Control The Input Data Format / Floating	Note 5-1
49	SEL1	Control The Input Data Format	Note 5-1,5
50	ISEL0	Control The Input Data Format	Note 5-1,5

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51	NC	Not Use	
52	DE	Data Enable Input	Note 5-2
53	GND	Ground	
54	GND	Ground	

Note 5-1:The mode control(SEL2) not use, it can't control CCIR601 interface, If not use CCIR601, it can floating.

Note 5-2:For digital RGB input data format, both SYNC mode and DE+SYNC mode are supported. If DE signal is fixed low, SYNC mode is used. Otherwise, DE+SYNC mode is used. Suggest used SYNC mode.

Note 5-3:Usually pull high.

- Note 5-4: IF select serial RGB or CCIR601/656 input mode is selected, only DX0-DX7 used, and the other short to GND, Only selected serial RGB \sim CCIR601/656 interface, DX BUS will enable, Digital input mode DX0 is LSB is MSB.
- Note 5-5:Control the input data format

SEL 2-0: Define the input interface mode.

SEL2	SEL1	SELO	Format	Operating Frequency
0	0	0	Parallel-RGB data format (only support stripe type color filter)	6.5MHz
0	0	1	Serial-RGB data format	19.5MHz
0	1	0	CCIR 656 data format (640RGB)	24.54MHz
0	1	1	CCIR 656 data format (720RGB)	27MHz
1	0	0	YUV mode A data format (Cr-Y-Cb-Y)	24.54MHz
1	0	1	YUV mode A data format (Cr-Y-Cb-Y)	27MHz
1	1	0	YUV mode B data format (Cb-Y-Cr-Y)	27MHz
1	1	1	YUV mode B data format (Cb-Y-Cr-Y)	24.54MHz

Input format	DOTCLK Freq (MHz)	Display Data	Active Area (DOTCLK)
YUV mode	24.54	640	1280
	27	720	1440

Mode	D[23:16]	D[15:8]	D[7:0]	IHS	IVS	DEN
ITU-R BT 656	D[23:16]	GND	GND	NC	NC	NC
ITU-R BT 601	D[23:16]	GND	GND	IHS	IVS	NC
8 bit RGB	D[23:16]	GND	GND	IHS	IVS	NC for HV Mode
0 011100	-[]	0.10				DEN for DEN Mode
24 bit PGP	PIZ-01	G[7:0]	BIZ:01	ILLS	IVS	NC for HV Mode
24 DIL RGB	12[7.0]	G[7.0]	B[7.0]	1115	105	DEN for DEN Mode

SPI timing Characteristics

PARAMETER	Symbol	Min.	Тур.	Max.	Unit
SPCK period	Tcx	60	1000		ns
SPCK high width	Тскн	30	1045		ns
SPCK low width	TCKL	30	The rest		ns
Data setup time	Tsun	12			ns
Data hold time	T _{HD1}	12	1 7648		ns
SPENA to SPCK setup time	T _{cs}	20	11 IS-1	5 +s =	ns
SPENA to SPDA hold time	TCE	20			ns
SPENA high pulse width	Tco	50	i kee		ns
SPDA output latency	T _{CR}	26 3 82	1/2	9 -s' 8	T _{CK}

Reference initial code:

Vgh,Vgl:(0x70,0x0003);//VGH=16.3V,VGL=-10.2V VcomAC: (0x72,0x6164); VcomDC: (0x70,0x0005); PWM: (0x72,0xB4D4);//PWM=19.7(B/L)

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6. Absolute Maximum Ratings:

					GND=0V,	Ta=25℃
Parameters	Symbol	Condition	Min.	MAX.	Unit	Remark
Power Voltage	DVDD,AVDD	GND=0	-0.3	5.0	V	
Input Signal Voltage	Vin	GND=0	-0.3	VDD+0.3	V	Note 6-1
Logic Output Voltage	Vout	GND=0	-0.3	VDD+0.3	V	Note 6-1



Note 6-1:Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

1.T≦60°C,90% RH Max

T>60°C, absolute humidity shall be less than 90% RH at 60°C



7. Electrical Characteristics

7-1) Recommended Operating Conditions:

				V33A		, 1 a−2 5 €
Item	Symbol	Min.	Тур.	Max.	Unit	Remark
Power Voltage	VCC	3.0	3.3	3.6	V	
Digital Operation Current	lcc	-	8.6	-	V	
Gate On Power	VGH	14	15	18	V	
Gate Off Power	VGL	-11	-10	-8	V	
Vcom High Voltage	VcomH	-	3.7	-	V	Note 7-1
Vcom Low Voltage	VcomL	-	-1.6	-	V	Note 7-1
Vcom Level max	VcomA	-	-	6	V	

Note 7-1: VcomH & VcomL : Adjust the color with gamma data. Vp-p should be higher then 4V .(Option 5V)

7-2) Recommended Driving Condition for Back Light

VSSA=GND=0V, Ta=25℃

Ta=25°℃

Parameter	Symbol	Min.	Тур.	Max.	Unit	Remark
LED current		-	20	-	mA	
Power Consumption		-	400	420	mW	
LED Voltage	VBL+	18.6	19.8	21	V	Note 7-2

Note 7-2 : There are 1 Groups LED



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8.DC Characteristics

Parameter	Symbol		Rating		Llpit	Remark	
Falailletei	Symbol	Min	Тур	Max	Onit		
Low Level input voltage	VIL	0	-	0.3*VCC	V		
High level input voltage	VIH	0.7*VCC	-	VCC	V		

9.AC Characteristics

Digital Parallel RGB interface

Signal	Item	Symbol	Min	Тур	Max	Unit
	Frequency	Tosc	-	156	-	ns
Dclk	High Time	Tch	-	78	-	Ns
	Low Time	Tcl	-	78	-	Ns
Data	Setup Time	Tsu	12	-	-	Ns
Dala	Hold Time	Thd	12	-	-	Ns
	Period	TH	-	408	-	Tosc
	Pulse Width	THS	5	30	-	Tosc
Uauma	Back-Porch	Thb	-	38	-	Tosc
nsync	Display Period	TEP	-	320	-	Tosc
	Hsync-den time	THE	36	68	88	Tosc
	Front-Porch	Thf	-	20	-	Tosc
	Period	Tv	-	262	-	TH
	Pulse Width	Tvs	1	3	5	TH
Vsync	Back-Porch	Tvb	-	15	-	TH
	Display Period	Tvd	-	240	-	TH
	Front-porch	Tvf	2	4	-	TH

Note: 1Thp + Thb=68,the user is make up by yourself

2.Tv=Tvs+Tvb+Tvd+Tvf, the user is make up by yourself 3.When SYNC mode is used,1st data start from 68th Dclk after Hsync falling

Digital Serial RGB interface

Signal	Item	Symbol	Min	Тур	Max	Unit
	Frequency	Tosc	-	52	-	ns
Dclk	High Time	Tch	-	78	-	Ns
	Low Time	Tcl	-	78	-	Ns
Data	Setup Time	Tsu	12	-	-	Ns
Data	Hold Time	Thd	12	-	-	Ns
	Period	TH	-	1224	-	Tosc
	Pulse Width	THS	5	90	-	Tosc
Heumo	Back-Porch	Thb	-	114	-	Tosc
Tisync	Display Period	TEP	-	960	-	Tosc
	Hsync-den time	THE	108	204	264	Tosc
	Front-Porch	Thf	-	60	-	Tosc
	Period	Tv	-	262	-	TH
	Pulse Width	Tvs	1	3	5	TH
Vsync	Back-Porch	Tvb	-	15	-	TH
	Display Period	Tvd	-	240	-	TH
	Front-porch	Tvf	2	4	-	TH

Note: 1Thp + Thb=204, the user is make up by yourself

2.Tv=Tvs+Tvb+Tvd+Tvf, the user is make up by yourself 3.When SYNC mode is used,1st data start from 204th Dclk after Hsync falling

CCIR601/656 interface

Signal	Item	Symbol	Min	Тур	Max	Unit
	Frequency	Tosc	-	37	-	ns
Dclk	High Time	Tch	-	78	-	ns
	Low Time	Tcl	-	78	-	ns
Data	Setup Time	Tsu	12	-	-	ns
Dala	Hold Time	Thd	12	-	-	ns

10. Pixel Arrangement



11. Display Color and Gray Scale Reference

										-	Inpi	ut C	colo	r D	ata										
Color					Re	ed							Gr	een	1						Bl	ue			
		R7	R6	R5	R4	R3	R2	R1	RO	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	В0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Basic	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Colors	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magent	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker																								
Red	\downarrow																								
	Brighte																								
	Red	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	Darker																								
Green	\downarrow																								
areen	Brighte																								
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Darker																								
Blue	\downarrow																								
Diuc	Brighte																								
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1



12. Waveform

Hear 150 Hear 173	12-1 SEL[2:0]	1)CCI	R601 Horizontal Timing	
HING HING	[]		Hgyab = 1560-	
001CLX	HSYNC			
RP(2) Inside Data Col V12 COS2 V1897 Deside Data SEL[20] = 101, MTSC How = 1280 RP(2) Inside Data Col V12 COSE V1787 COSE	DOTCLK			
SEL[20]= 101, NTSC Herror Lise - HEPBOY 4-5TH (10) Herror Lise -	RR[7:0]		Invalid Data Cr1 X Y1 X Cb1 X Y2 Cr320 X Y639 X Cb320 X Y640	Invalid Data
SEL[c0] = 101, MSC How SEL[c0] = 101, PRL How SEL[c0] = 100, PRL How SEL[c0			tese = HBP[6:0]*4+STH[1:0] → t	
HEYNC	SEL[2:0]]= 101, N	ПSC 	
DOTCLK RR[7:8] WeidEDats Cot V Y Cot V 2 Cot80 V 18 CL380 V 728 WeidEDats Cot V Y Cot V 2 Cot80 V 718 CL380 V 728 WeidEDats Cot V Y Cot V 2 Cot80 V 718 CL380 V 728 WeidEDats Cot V Y Cot V 2 Cot80 V 718 CL380 V 728 WeidEDats Cot V Y Cot V 2 Cot80 V 718 CL380 V 728 WeidEDats Cot V Y Cot V 2 Cot80 V 718 CL380 V 728 WeidEDats Cot V Y Cot V 2 Cot80 V 718 CL380 V 728 WeidEDats Cot V Y Cot V 2 Cot80 V 718 CL380 V 728 WeidEDats Cot V Y Cot V 2 WeidEDats Cot V Y Cot V 2 Cot80 V 718 CL380 V 728 WeidEDats Cot V Y Cot V 2 WeidEDats Cot V Y Cot V 2 Cot V Y Cot V 2 WeidEDats Cot V Y Cot V	HSYNC]	
BR(7:) Weild Data Ori Y1 Cold Y2 Cold Y12 Herride Data SEL[20] = 101, PAL Human 1728 Herride Data Ori Y1 Cold Y2 Cold Y19 Cold<	DOTCLK			
SEL[20] = 101, PAL Hga = 1725 HNNC Image: HBP(8074-8TH(10)) Hga = 1725 SEL[20] = 110, NTSO Hga = 1715 SEL[20] = 110, NTSO Hga = 1715 HSYNC Image: HBP(8074-8TH(10)) Hga = 1715 SEL[20] = 110, NTSO Hga = 1715 Hga = 1715 HSYNC Image: HBP(8074-8TH(10)) Hga = 1725 HSYNC Image: HBP(8074-8TH(10)) Hga = 1500 HSYNC Image: HBP(8074-8TH(10)) Hga = 1500	RR[7:0]		Invalid Data Cr1 X Y1 X Cb1 X Y2 Cr360 X Y7 19 X Cb360 X Y7 2	Invalid Data
SEL[2:0] = 101, PAL HSYNC HUME TO CONSTRUCT AND ADDR SEL[2:0] = 101, NTSC SEL[2:0] = 110, NTSC SEL[2:0] = 110, NTSC HUME TO CONSTRUCT ADDR SEL[2:0] = 110, PAL HUME TO CONSTRUCT ADDR HUME TO CONSTRUCT ADDR SEL[2:0] = 110, PAL HUME TO CONSTRUCT ADDR SEL[2:0] = 110, PAL HUME TO CONSTRUCT ADDR HUME TO CONSTRUCT A				
HSYNC HSYNC HSYNC HSYNC HSYNC HSURID Data HSYNC HSURID Data HSYNC HSURID Data HSYNC HSURID Data HSYNC HSURID Data HSYNC	SEL[2:0]	= 101, P	AL	
DOTOLIX PR(7-8) Preside Data Preside Data	HSYNC			
DOTOLIK RR[7:0] Hvelid Data Cot V1 Cot V2 Cot V1 Cot V2 Cot V2 Cot V1 Cot V2 Cot	nonto		<u> </u>	
RR(7-1) Invalid Data Cr1 Y1 Cb1 Y2 Cc380 Y719 Cb380 Y729 Invalid Data SEL[2:0] = 110, NTSC Hgra = 1716 Hgra = 1726 Hgra = 1500 <	DOTCLK			
Image: HBPB007 4:5TH 1:0] Image: 1716 SEL [2:0] = 110, NTSC HSYNC DOTOLK Image: HBPB007 4:5TH 1:0]	RR[7:0]		Invalid Data Y Cr1 Y1 Cb1 Y2 Cr360 Y719 Cb360 Y720	Invalid Data
SEL[2:0] = 110, NTSC HSYNC DOTCLK AR[7:0] Hwalid Data Col V1 Crl V2 Col V1 Crl V2 Crl V2 Crl V2 Crl V2 Crl V2 Crl V2 Crl V2 Crl			← t _{iBP} = HBP[6:0]*4+STH[1:0] → ← H _{DiSP} = 1440	
HSYNC DOTCLK J J J J J J J J J J J J J J J J J J J	SEL[2:0]	= 110, N	TSC	
DUTCLK RR[7:0] Ivvalid Data RR[7:0] Ivvalid Data Col Y1 Cr1 Y2 CD500 Y719 C080 Y720 Ivvalid Data Hose = 1440 SEL[2:0] = 110, PAL HSYNC CDTCLK RR[7:0] Ivvalid Data Col Y1 Cr1 Y2 CD500 Y719 C080 Y720 Ivvalid Data Col Y1 Cr1 Y2 CD500 Y719 C080 Y720 Ivvalid Data Hose = 1440 Kape = 140 Kape = 14	HSYNC			
RR[7:0] Invalid Data Cb1 Y1 Cr1 Y2 Cb380 Y719 C6800 Y720 Invalid Data SEL[2:0] = 110, PAL Hgra = 1720 DOTCLK Hgra = 1720 BR[7:0] Hvalid Data Cb1 Y1 Cr1 Y2 Cb380 Y719 Cd800 Y720 Invalid Data BR[7:0] Hvalid Data Cb1 Y1 Cr1 Y2 Cb380 Y719 Cd800 Y720 Invalid Data BR[7:0] Hvalid Data Cb1 Y1 Cr1 Y2 Cb380 Y719 Cd800 Y720 Invalid Data BR[7:0] Hvalid Data Cb1 Y1 Cr1 Y2 Cb380 Y719 Cd800 Y720 Invalid Data BR[7:0] Hvalid Data Cb1 Y1 Cr1 Y2 Cb320 Y839 Cd20 Y840 Invalid Data HBYNC Hgra = HBP[60]*4-STH[1:0] Hgra = 1580 Hgra = 1280 Hgra = 1280 Hgra = 1280	DOTCLK			
Image: HBP(80)*4+STH(1:0) House = 1440 SEL [2:0] = 110, PAL House = 1720 Image: HSP(80)*4+STH(1:0) House = 1440 Image: HSP(80)*4+STH(1:0) House = 1440 Image: HSP(80)*4+STH(1:0) House = 1580 Image: HSP(80)*4+STH(1:0) House = 1580 Image: HSP(80)*4+STH(1:0) House = 1280 Image: HSP(80)*4+STH(1:0) House = 1280	RR[7:0]		Invalid Data X Cb1 X Y1 X Cr1 X Y2 Cb360 X Y7 19 X Cr360 X Y720	Invalid Data
SEL [2:0] = 110, PAL HSYNC DOTCLK AR[7:0] Hvalid Data Hoge = HBP[6:0]' + STH[1:0] Hoge = 1560 Hoge = 1280 Hoge = 1				<u> </u>
HSYNC DOTCLK HSYNC H	SEL[2:0]	= 110, P	AL	
HSYNC DOTCLK RR[7:0] Invalid Data Cb1 Y1 Cr1 Y2 Cb360 Y719 Cr360 Y720 Invalid Data tupe = HBP[6:0]' 4+STH[1:0] Hyge = 1560 Hyge = 1560 Hyge = 1560 Hyge = 1560 Hyge = 1280 Hyge = 1280 Hyge = 1280 Hyge = 1280 Hyge = 1280			← H _{qrdc} = 1729 →	
DOTCLK RR[7:0] Invalid Data tuge = HBP[6:0] ² + STH[1:0] + Crit V2 Hore = 1560 DOTCLK RR[7:0] Invalid Data Cot V1 Crit V2 Cob360 V719 Cris60 V720 Invalid Data Hore = 1440 Hore = 1560 Hore = 1440 Hore = 1560 Hore = 1440 Hore = 160 Hore = 1280 Hore = 1280 Hore = 1280 Hore = 1280	HSYNC		ļ ļ	
RR[7:0] Invalid Data Cb1 Y1 Cr1 Y2 Cb360 Y719 Cr360 Y720 Invalid Data SEL[2:0] = 111, NTSC/PAL Horse = 1440 Horse = 1440 Horse = 1440 Horse = 1440 DOTCLK Hyra = 1560 Horse = 1560 Horse = 1280 Horse = 1280	DOTCLK			
SEL[2:0] = 111, NTSC/PAL Hose = 1600 HSYNC Hyde = 1500 DOTCLK Hose = 100 Image: HBP[6:0]*4+STH[1:0] Hose = 1280	RR[7:0]		Invalid Data Cb1 Y1 X Cr1 Y2 Cb360 Y7 19 X Cr360 Y720	Invalid Data
SEL[2:0] = 111, NTSC/PAL HSYNC DOTCLK RR[7:0] Invalid Data Cb1 X1 XC1 Y2 Cb320 Y639 Cr320 Y640 Invalid Data HSPE HBP[6:0]*4+STH[1:0] HSTRC HSPE 1280			م المعالي	
HSYNC DOTCLK RR[7:0] Invalid Data t _{HSP} = HBP[6:0]" 4+STH[1:0] HSYNC Hyde = 1580 (/	SEL[2:0]	= 111, N	TSC/PAL	
DOTCLK	HSYNC		≪H _{yde} = 1580≯	
DOTCLK				
RR[7:0] Invalid Data Cb1 Y1 Cr1 Y2 Cb320 Y639 Cr320 Y640 Invalid Data + <td< td=""><td>DOTCLK</td><td></td><td></td><td></td></td<>	DOTCLK			
t _{HBP} = HBP[6:0] [*] 4+STH[1:0] → + → + →	RR[7:0]		Invalid Data X Cb1 X Y1 X Cr1 X Y2 Cb320 X Y639 X Ci320 X Y640 X	Invalid Data
			4 ↓ _{HBP} = HBP[6:0] [*] 4+STH[1:0] → 4 ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓	



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12-2)CCIR601 Vertical Timing

SEL[2:0] = 100 ~ 111, NTSC



RR[7:0] DL293 DL294 DL295 DL296 DL297 DL299

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DL1 DL2 DL3 DL4 DL5 DL6 DL7

12-3) CCIR656 Horizontal Timing SEL[2:0] = 010, NTSC/PAL FF X 00 X 00 X EAV X FF X 00 X 00 X SAV Cb1 X Y1 X Cr1 X Y2 > Cb320 Y630 Cr320 Y640 FF X 00 X 00 X EAV X Invalid Data invalid Data t_{HEF =} HBP[6:0]"4+STH[1:0]-SEL[2:0] = 011, NTSC FF X 00 X 00 X EAV X invalid Data FF X 00 X 00 X SAV X Cb1 X Y1 X Cr1 X Y2 -- Cb360 Y7 19 Cr360 Y720 FF 00 00 EAV ivalid Data BR[7:0] t_{HEP} = HBP[6:0]"4+STH[1:0]-SEL[2:0] = 011, PAL BR[7:0] FF 00 00 EAV invalid Data FF 00 00 SAV Cb1 Y1 Cr1 Y2 Cb360 Y7 19 Cr360 Y720 FF 00 00 EAV Iwalid Data - 1728 12-4)CCIR656 Vertical Timing SEL[2:0] = 010, 011, NTSC (F=0 → ODD field, F=1 → EVEN field) н 523 524 525 1 2 3 4 5 19 20 21 22 23 24 25 26 V F -tvBP = VBP[6:0]-RR[7:0] DL238 DL239 DL240 DL1 DL2 DL3 DL4 н 261 262 263 264 265 266 267 268 282 283 284 285 286 287 288 289 V F -tvep = VBP[6:0]-RR[7:0] DL239DL240 DL1 DL2 DL3 DL4 SEL [2:0] = 010, 011, PAL, PALM=0 (F=0 → ODD field, F=1 → EVEN field) н 618 619 620 621 622 623 624 625 1 2 3 21 22 23 24 25 26 27 28 29 30 v F RR[7:0] DL276 DL280 -t_{VBP} = VBP[6:0]-DL1 DL2 DL3 DL4 н 305 306 307 308 309 310 311 312 313 314 315 333 334 335 336 337 338 339 340 341 342 F RR[7:0] DL279 DL280 -tver = VBP[6:0] + 1-DL1 DL2 DL3 SEL [2:0] = 010, 011, PAL, PALM=1 (F=0 → ODD field, F=1 → EVEN field) н 618 619 620 621 622 623 624 625 1 2 3 21 22 23 24 25 26 27 28 29 30 ν -t_{VBP} = VBP[6:0]-RR[7:0] DL283 DL284 DL285 DL286 DL287 DL288 DL1 DL2 DL3 DL4 DL5 DL6 DL7 DL8 н 305 306 307 308 309 310 311 312 313 314 315 333 334 335 336 337 338 339 340 341 342 ν F -t_{rep} = VBP[6:0] + 1--

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12-5)Digital RGB NTSC mode Vertical Data Format for $262 T_{\text{H}}$



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12-10)Standby ON/OFF Control

When STB pin is pulled L, blank data is outputted for 5-frames first, form the falling edge of the following VSYNC signal. The blank data would be gray level 255 for normally white LC.



12-11)Clock and Sync waveforms



RESET



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т

T>1ms



14. Optical Characteristics

14-1)	Specification:
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Ta = 25℃

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks	
	Horizontal	θ 21, θ 22		50	60	-	deg		
Viewing Angle	Vortical	heta 12	CR≧10	40	50	-	deg	Note 14-1	
	vertical	heta 11		45	55		deg		
Contrast F	Ratio	CR	At optimized Viewing angle	300	400			Note 14-2	
Luminar	nce	L	<i>θ</i> =0°	180	250		cd/m²		
White Chron	naticity	х	<i>θ</i> =0°	0.26	0.31	0.36			
white Child	nationy	У	<i>θ</i> =0°	0.28	0.33	0.38			
Response time	Rise	Tr	$\theta = 0^{\circ}$	-	10	-	ms	Note 1/1-3	
Response time	Fall	Tf	0-0	-	15	-	ms	14-5	
LE	D Life Time		+25 ℃	-	50000	-	hrs	Note 14-4	

Note 14-1 : The definitions of viewing angles



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Note 14-2 : CR = Luminance when Testing point is White Luminance when Testing point is Black

Contrast Ratio is measured in optimum common electrode voltage.

Note 14-3 : The definition of response time :



Note 14-4 : The "LED Life time " is defined as the module brightness decrease to 50% original Brightness that the ambient temperature is 25° C and $I_{LED} = 20$ mA

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15. Handling Cautions

- 15-1) Mounting of module
 - A)Please power off the module when you connect the input/output connector.
 - B)Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
 - C)Protective film (Laminator) is applied on surface to protect it against scratches and dirt.
- 15-2) Precautions in mounting
 - A) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
 - B) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
 - C) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
 - D) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.
- 15-3) Adjusting module
 - A) Adjusting volumes on the rear face of the module have been set optimally before shipment.
 - B) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.
- 15-4) Others
 - A) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
 - B) Store the module at a room temperature place.
 - C) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
 - D) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
 - E) Observe all other precautionary requirements in handling general electronic components.
 - F) Please adjust the voltage of common electrode as material of attachment by 1 module.
- 15-5) Polarizer mark

The polarizer mark is to describe the direction of view angle film how to mach up with the rubbing direction.

16. Reliability Test

No	Test Item	Test Condition					
1	High Temperature Storage Test	Ta = +80℃, 240 hrs					
2	Low Temperature Storage Test	Ta = -30 $^\circ$ C , 240 hrs					
3	High Temperature Operation Test	Ta = +70℃, 240 hrs					
4	Low Temperature Operation Test	Ta = -20 $^\circ$ C , 240 hrs					
5	High Temperature & High Humidity Operation Test	Ta = +60℃, 90%RH, 240 hrs					
6	Thermal Shock Test	$-20^{\circ}\text{C} \rightarrow +70^{\circ}\text{C}$, 100 Cycles,					
0	(non-operating)	30 min 30 min					
		Frequency:10~550Hz					
7	Vibration Test	Vibration Test Amplitude: 1.3mm					
'	(non-operating)	Sweep:1.5G,33.3~400Hz					
		Vibration: Sinusoidal Wave,1Hrs for X,Y,Z direction					
		100G, 6ms					
0	Shock Test	Direction : $\pm X$, $\pm Y$, $\pm Z$					
0	(non-operating)	Cycle : 3 times					
		Half sinusoidal wave					
0	Electrostatic Discharge Test	150pF, 330Ω					
9	(non-operating)	Air : ±8KV ; Contact : ±6KV					

Ta: ambient temperature

Note : The protective film must be removed before temperature test.

[Criteria]

- 1. The test samples have recovery time for 2 hours at room temperature before the function check. In the standard conditions, there is no display function NG issue occurred.
- 2. All the cosmetic specifications are judged before the reliability stress.



17. Block Diagram TBD



18. Packing TBD