

Package Style: Bare Die

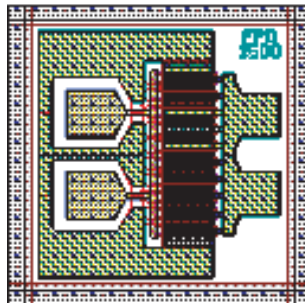


Product Description

The FPD1500 is an AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT), featuring a 0.25 μm x1500 μm Schottky barrier gate, defined by high-resolution stepper-based photolithography. The recessed gate structure minimizes parasitics to optimize performance. The epitaxial structure and processing have been optimized for reliable high-power applications. The FPD1500 is also available in the low-cost plastic SOT89 and DFN packages.

Optimum Technology Matching® Applied

- GaAs HBT
- GaAs MESFET
- InGaP HBT
- SiGe BiCMOS
- Si BiCMOS
- SiGe HBT
- GaAs pHEMT
- Si CMOS
- Si BJT
- GaN HEMT
- InP HBT
- RF MEMS
- LDMOS



Features

- 29dBm Linear Output Power at 12GHz
- 9dB Power Gain at 12GHz
- 12.5dB Max Stable Gain at 12GHz
- 41dBm O_{IP3}
- 35% Power-Added Efficiency

Applications

- Narrowband and Broadband High-Performance Amplifiers
- SATCOM Uplink Transmitters
- PCS/Cellular Low-Voltage High-Efficiency Output Amplifiers
- Medium-Haul Digital Radio Transmitters

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power at P_{1dB} Gain Compression	28.5	30.0		dBm	$V_{DS}=8V, I_{DS}=50\% I_{DSS}$
Maximum Stable Gain (S21/S12)	11.5	12.5		dB	$V_{DS}=8V, I_{DS}=50\% I_{DSS}$
Power Gain at P_{1dB}	8.0	9.0		dB	$V_{DS}=8V, I_{DS}=50\% I_{DSS}$
PAE		45		%	$V_{DS}=8V, I_{DS}=50\% I_{DSS}, P_{OUT}=P_{1dB}$
OIP_3 from 15dB to 5dB below P_{1dB}		41		dBm	$V_{DS}=8V, I_{DS}=50\% I_{DSS}$
		43		dBm	Matched for optimal power, tuned for best IP_3
Saturated Drain-Source Current (I_{DSS})	375	465	550	mA	$V_{DS}=1.3V, V_{GS}=0V$
Maximum Drain-Source Current (I_{MAX})		750		mA	$V_{DS}=1.3V, V_{GS}\approx +1V$
Transconductance		400		ms	$V_{DS}=1.3V, V_{GS}=0V$
Gate-Source Leakage Current (I_{GSO})		1	15	μA	$V_{GS}=-5V$
Pinch-Off Voltage (V_P)	0.7	1.0	1.3	V	$V_{DS}=1.3V, I_{DS}=1.5\text{mA}$
Gate-Source Breakdown Voltage (V_{BDGS})	12.0	14.0		V	$I_{GS}=1.5\text{mA}$
Gate-Drain Breakdown Voltage (V_{BDGD})	14.5	16.0		V	$I_{GD}=1.5\text{mA}$
Thermal Resistivity (θ_{JC}) *		42		$^{\circ}\text{C}/\text{W}$	$V_{DS}>6V$

Note: $T_{AMBIENT}=22^{\circ}\text{C}$, RF specifications measured at $f=12\text{GHz}$ using CW signal.

Absolute Maximum Ratings¹

Parameter	Rating	Unit
Drain-Source Voltage (V_{DS}) ($-3V < V_{GS} < -0.5V$) ²	10	V
Gate-Source Voltage (V_{GS}) ($0V < V_{DS} < +8V$)	-3	V
Drain-Source Current (I_{DS}) (For $V_{DS} < 2V$)	I_{DSS}	
Gate Current (Forward or reverse current)	15	mA
RF Input Power (P_{IN}) (Under any acceptable bias state)	25	dBm
Channel Operating Temperature (T_{CH}) (Under any acceptable bias state)	175	°C
Storage Temperature (T_{STG}) (Non-Operating Storage)	-65 to 150	°C
Total Power Dissipation (P_{TOT}) ^{3, 4, 5}	3.6	W
Simultaneous Combination of Limits ⁶ (2 or more max. limits)	80	%

Notes:

¹ $T_{AMBIENT} = 22$ °C unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device.

²Operating at absolute maximum V_D continuously is not recommended. If operation at 10V is considered then I_{DS} must be reduced in order to keep the part within its thermal power dissipation limits. Therefore V_{GS} is restricted to $< -0.5V$.

³Total Power Dissipation to be de-rated as follows above 22 °C: $P_{TOT} = 3.6 - (0.024W/°C) \times T_{HS}$, where T_{HS} = heatsink or ambient temperature above 22 °C. Example: For a 85 °C carrier temperature: $P_{TOT} = 3.6 - (0.024 \times (85 - 22)) = 2.09W$

⁴Total Power Dissipation (P_{TOT}) defined as $(P_{DC} + P_{IN}) - P_{OUT}$, where P_{DC} : DC Bias Power, P_{IN} : RF Input Power, P_{OUT} : RF Output Power.

⁵Users should avoid exceeding 80% of 2 or more Limits simultaneously.

⁶Thermal Resistivity specification assumes a Au/Sn eutectic die attach onto an Au-plated copper heatsink or rib.



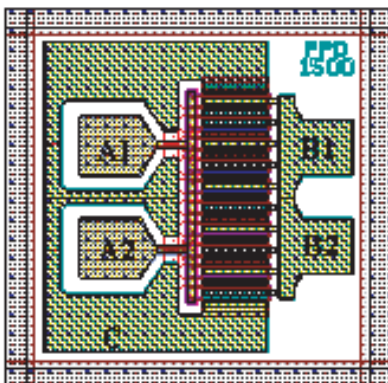
Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

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Pad Layout



Pad	Description	Pin Coordinates (μm)
A1	Gate Pad	130, 330
A2	Gate Pad	130, 190
B1	Drain Pad	390, 330
B2	Drain Pad	390, 190
C	Source Pad	

Note: Coordinates are referenced from the bottom left hand corner of the die to the center of the bond pad opening.

Die Size (μm)	Die Thickness (μm)	Min. Bond Pad Opening ($\mu m \times \mu m$)
470x530	75	64x77

Preferred Assembly Instructions

GaAs devices are fragile and should be handled with great care. Specially designed collets should be used where possible.

The back of the die is metallized and the recommended mounting method is by the use of conductive epoxy. Epoxy should be applied to the attachment surface uniformly and sparingly to avoid encroachment of epoxy onto the top face of the die. Ideally it should not exceed half the chip height. For automated dispense Ablestick LMISR4 is recommended and for manual dispense Ablestick 84-1 LMI or 84-1 LMIT are recommended. These should be cured at a temperature of 150 °C for one hour in an oven especially set aside for epoxy curing only. If possible the curing oven should be flushed with dry nitrogen. The gold-tin (80% Au 20% Sn) eutectic die attach has a melting point of approximately 280 °C but the absolute temperature being used depends on the leadframe material used and the particular application. The maximum time at used should be kept to a minimum.

This part has gold (Au) bond pads requiring the use of gold (99.99% pure) bondwire. It is recommended that 25.4mm diameter gold wire be used. Recommended lead bond technique is thermocompression wedge bonding with 0.001” (25µm) diameter wire. Bond force, time stage temperature and ultrasonics are all critical parameters and the settings are dependent on the setup being used and application. Ultrasonic or thermosonic bonding is not recommended.

Bonds should be made from the die first and then to the mounting substrate or package. The physical length of the bondwires should be minimized especially when making RF or ground connections.

Handling Precautions



To avoid damage to the devices, care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing.

ESD/MSL Rating

These devices should be treated as Class 0 (0V to 250V) using the human body model as defined in JEDEC Standard No. 22-A114. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263. This is an unpackaged part and therefore no MSL rating applies.

Application Notes and Design Data

Application Notes and design data including S-parameters, noise paramters, and device model are available on request from www.rfmd.com.

Reliability

An MTTF of 4.2 million hours at a channel temperature of 150 °C is achieved for the process used to manufacture this device.

Disclaimers

This product is not designed for use in any space-based or life-sustaining/supporting equipment.

Ordering Information

Delivery Quantity	Ordering Code
Full Pack (100)	FPD1500-000
Small Quantity (25)	FPD1500-000SQ
Sample Quantity (3)	FPD1500-000S3

FPD1500

