Headphone Amplifiers

Digital Input Class-D Headphone Amplifier

BU7839GVW

No.10102EAT03

●Description

Most suitable for long duration reproduction of digital audio because digital audio data is taken as its input and low power consumption is realized.BU7839GVW has Stereo Audio DAC and HP amp functions for digital audio playback.
Pop sound in ramp-up period is reduced due to built-in start-up sound reduction circuit or transistor for mute.
Also, Built-in digital volume which can control L-ch & R-ch separately.

●Features

1) With Stereo Audio DAC and HP amp functions
2) Most suitable for long duration reproduction of digital audio because digital audio data is taken as its input and low power consumption is realized
3) Pop sound in ramp-up period is reduced due to built-in start-up sound reduction circuit or transistor for mute
4) Built-in digital volume which can control L-ch & R-ch separately
   Immediate switching and zero cross switching for reduction of clicking sound at the time of gain change
   Gain change methods of soft switching can be selected with registers
5) Sampling frequency compatible with 8kHz-48kHz
6) Compatible with master slave with built-in PLL
7) Built-in soft mute function
8) Compatible with full front and full back formats
9) Compatible with 16, 18 & 24bit formats
10) Compatible with fs=32kHz,44.1kHz,48kHz with de-emphasis function
11) 2wire CPU I/F (2 addresses selectable 33h, 36h)

●Functions

Stereo Audio DAC + HPamp

- 2wire CPU I/F
- Serial audio I//F
- Interpolator
- ΔΣModulator
- Level Shifter
- PLL

●Absolute maximum rating

Parameter	Symbol	Ratings	Unit
Analog power supply voltage	AVDD	-0.3 ～ 4.5	V
Digital power supply voltage	DVDD	-0.3 ～ 2.1	V
Digital IO power supply voltage	DVDDIO	-0.3 ～ 4.5	V
Terminal applied voltage 1	VIN1	DVSS-0.3 ～ DVDDIO+0.3	V
Terminal applied voltage 2 *1	VIN2	DVSS-0.3 ～ 4.5	V
Allowance loss	Pd	520 *2	mW
Storage temperature range	Tstg	-50 ～ 125	℃
Operation temperature range	Topr	-30 ～ 85	℃

* 1 SDA,SCL terminal
* 2 When you use at above Ta = 25 degree, 52mW are reduced concerning 1degree
When you mount 114.6mm x 76.2mm x 1.6mm

Note:When you use under the conditions which exceed this value, there are times when the device is destroyed. In addition usual operation is not guaranteed.

●Recommended operating range

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
Analog power supply voltage	AVDD	2.5	2.8	3.0	V
Digital IO power supply voltage	DVDDIO	DVDD	-	3.0	V
Digital power supply voltage	DVDD	1.35	1.50	1.65	V

●**External size figure**

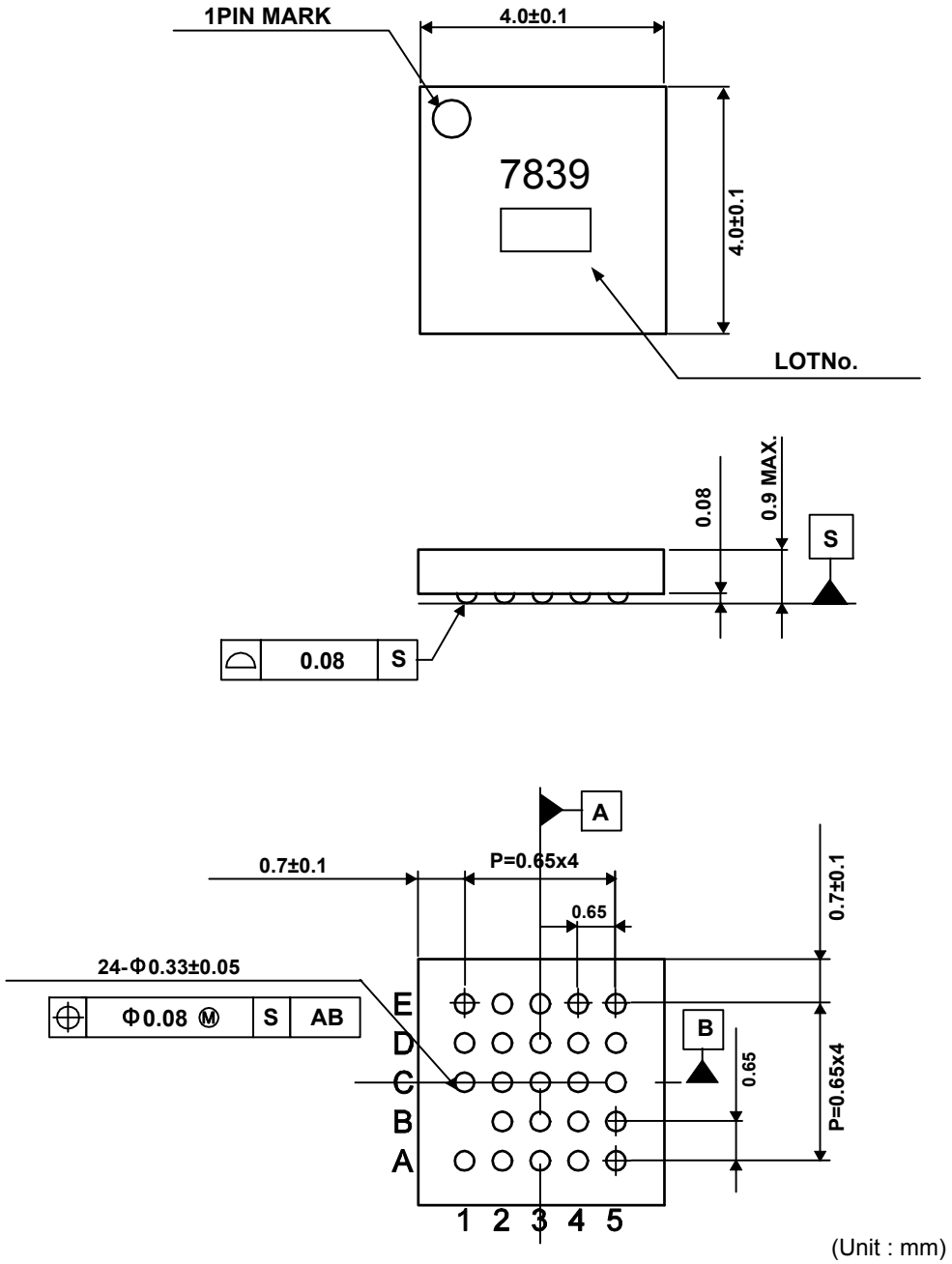


Fig.1 External size figure

●Block diagram

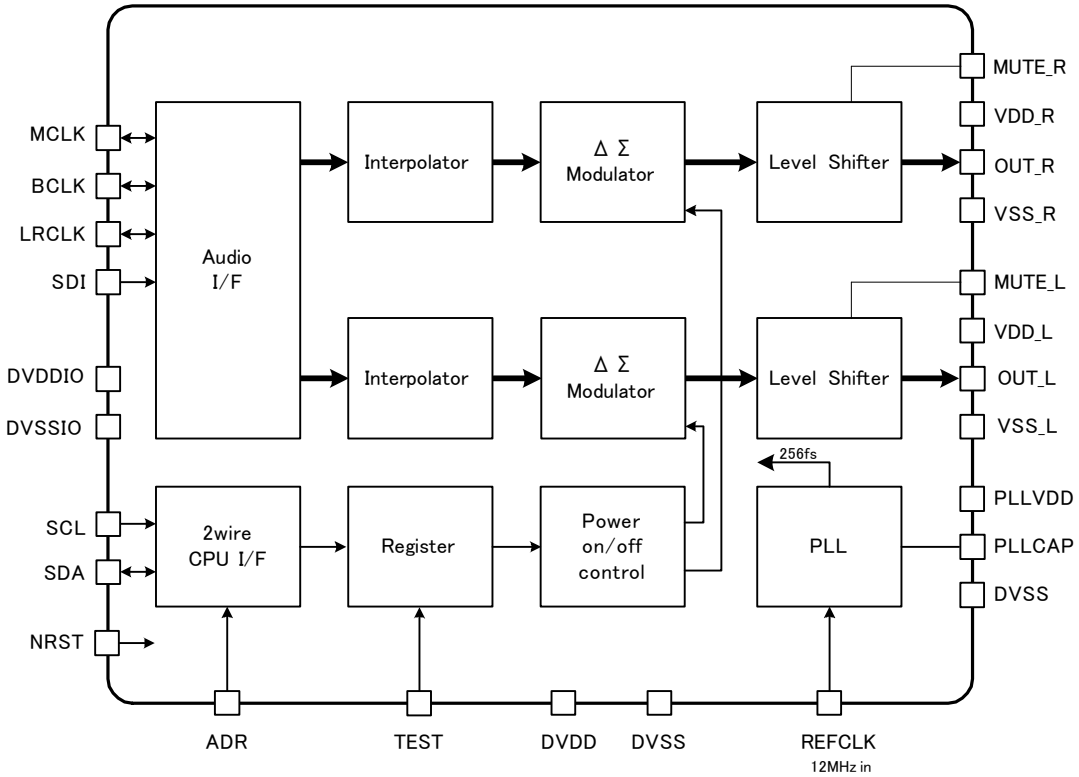


Fig. 2 Block diagram

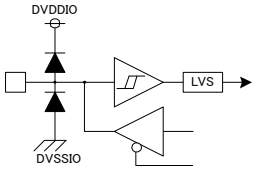
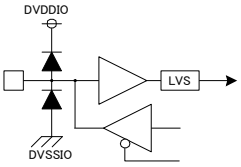
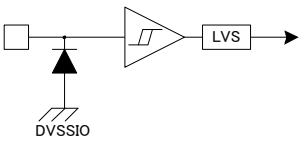
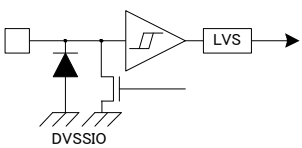
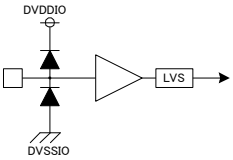
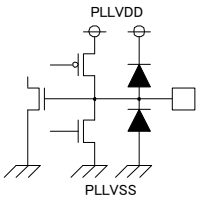
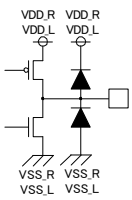
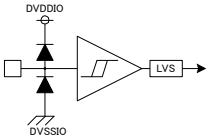
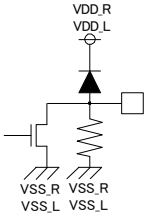
●Description of each block

●2wire CPU I/F
Interface with CPU, 2-wire control
Write/read possible
Device address is 2-address selectable (33h,36h) with ADR terminal
●Register
This LSI is controlled all by register
Write/read by 2wire CPU I/F
●Audio I/F
Compatible with three modes of full front, full back and IIS
Sampling frequency compatible with 8kHz～48kHz
●Interpolator,ΔΣModulator
Variable over sampling, Order-variable ΔΣ modulator
Optimum value is selected internally and automatically
●Level Shifter
Level conversion in 3V series of analogue output
Built-in mute transistor for start-up sound reduction
●PLL
REFCLK terminal is taken as reference clock and 256fs is created
It becomes the default setting when 12MHz is inputted to REFCLK
Please change each setting if any frequency other than 12MHz is inputted to REFCLK

●**Terminal table**

No	Terminal name	Function	Classification	Digital/ Analog	In/Out	Rest middle/ rear Initial value	Note
A1	MCLK	Audio I/F Master clock	A	D	In/Out	in	256fs
B3	BCLK	Audio I/F Bit clock	B	D	In/Out	in	64fs
A2	LRCLK	Audio I/F LR clock	B	D	In/Out	in	fs
C2	SDI	Audio I/F Serial data	E	D	In	-	
C1	DVDDIO	Digital IO VDD	-	D	-	-	I/O power supply
B4	SCL	2wire CPU I/F serial clock	C	D	In	-	
A5	SDA	2wire CPU I/F serial data	D	D	In/Out	in	
B2	NRST	Reset	E	D	In	-	L: reset
A3	ADR	Device address select	E	D	In	-	L:33h or H:36h
C3	TEST	test pin	E	D	In	-	Please connect to the ground
D1	DVDD	Digital core VDD	-	D	-	-	Digital power supply
A4	DVSS	Digital core VSS	-	D	-	-	Digital ground ※
B5	REFCLK	reference clock	H	D	In		Input 10M～20MHz
D5	PLLVDD	PLL VDD	-	A	-	-	PLL power supply
C5	PLLCAP	PLL capacitor	F	A	Out	Hiz	
C4	DVSS	PLL, Digital VSS	-	D	-	-	PLL, Digital ground ※
D4	VDD_R	Analog VDD	-	A	-	-	Rch power supply
E4	OUT_R	Rch output	G	A	Out	Hiz	
E5	MUTE_R	Rch mute	I	A	Out	Hiz	For starting sound decrease
D3	VSS_R	Analog VSS	-	A	-	-	Rch ground
E1	VDD_L	Analog VDD	-	A	-	-	Lch power supply
E2	OUT_L	Lch output	G	A	Out	Hiz	
D2	MUTE_L	Lch mute	I	A	Out	Hiz	For starting sound decrease
E3	VSS_L	Analog VSS	-	A	-	-	Lch ground

●**Terminal equivalent circuit figure**

A		B		C	
D		E		F	
G		H		I	

●Application circuit chart

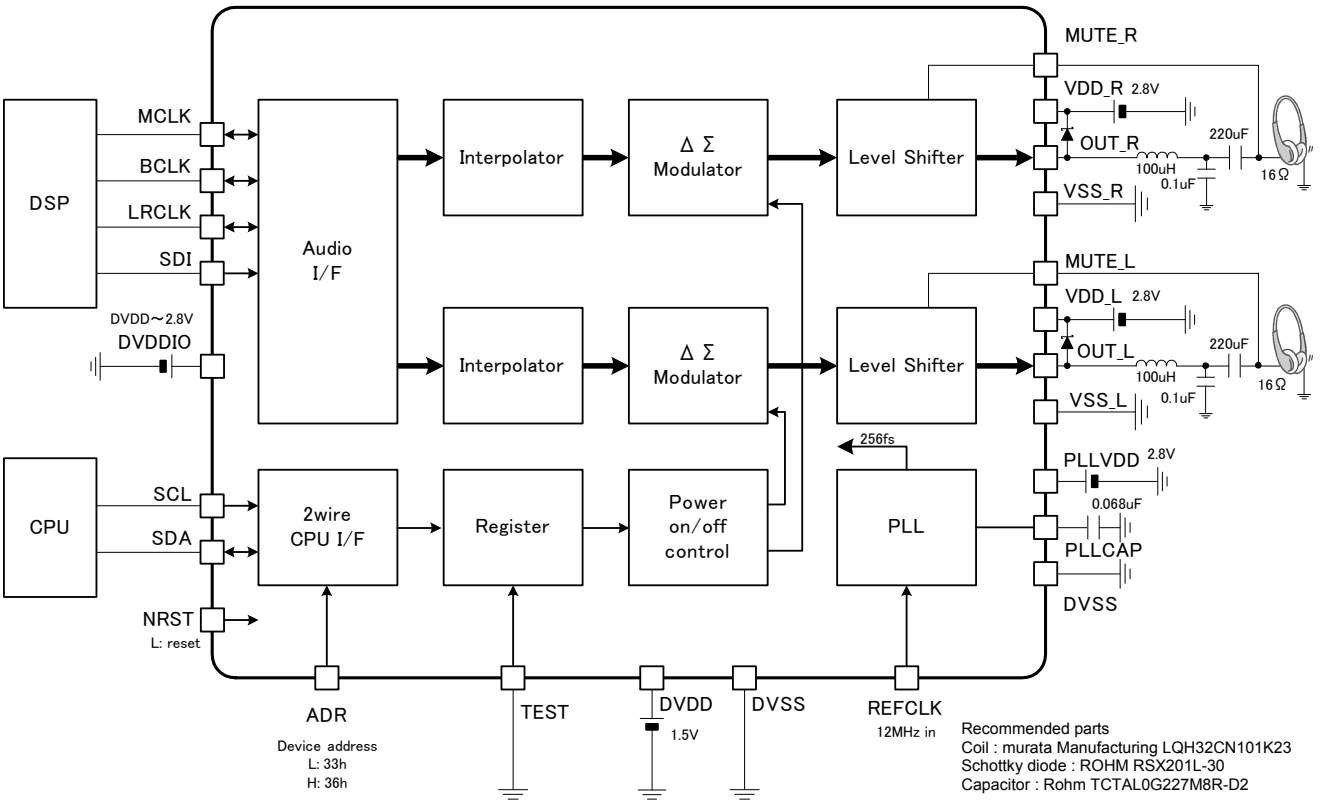


Fig.3 Application circuit chart

●Measurement circuit chart

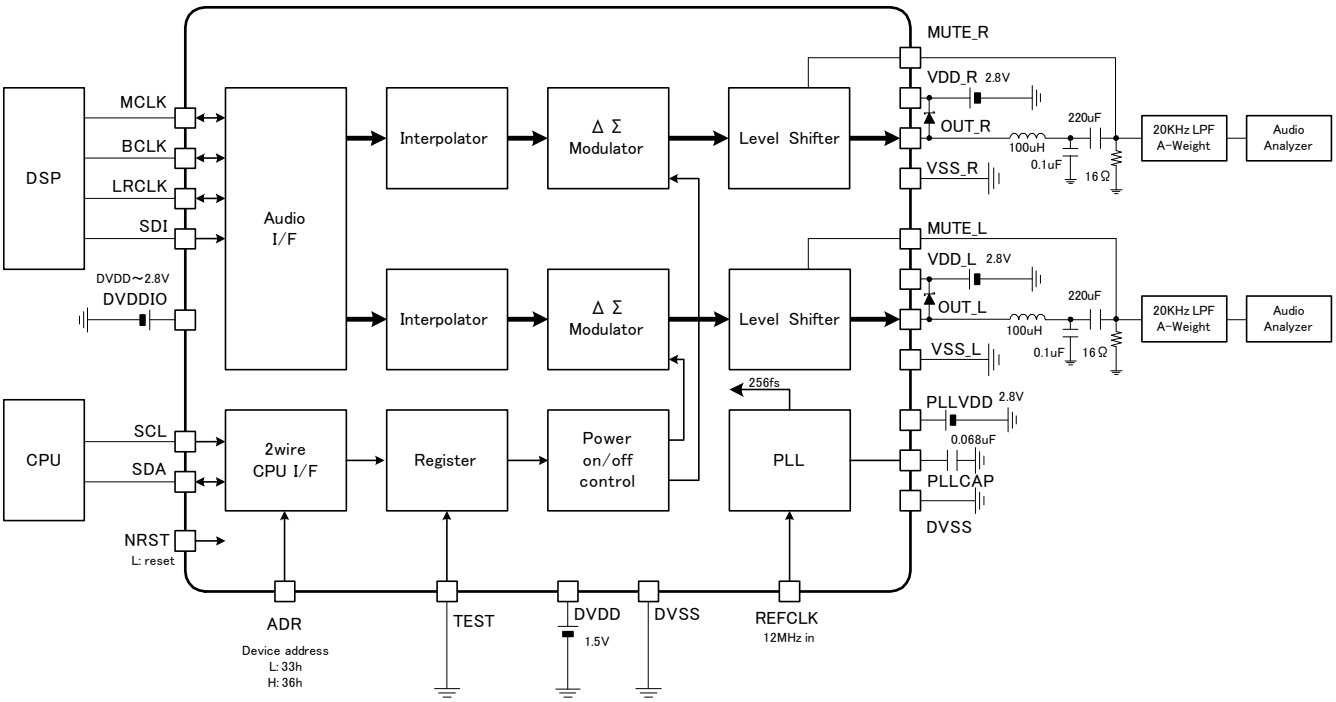


Fig.4 Measurement circuit chart

●**Electrical Characteristic**

Ta=25degree,DVDD=DVDDIO=1.5V,VDD_R=VDD_L=PLLVDD=2.8V,REFCLK=12MHz,fs=44.1kHz,f=1kHz,Load=16Ω, A-weight,20kHzLPF,Slave mode

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
Static consumption current DVDD	IDDst	-	-	10	μA	At the time of standby
Static consumption current VDD_R+VDD_L	ICCst	-	-	10	μA	At the time of standby
Static consumption current PLLVDD	IPLLst	-	-	10	μA	At the time of standby
Consumption current DVDD	IDD	-	0.6	2.0	mA	At the time of 0.1mW output (in slave mode)
Consumption current VDD_R+VDD_L	ICC	-	2.0	6.0	mA	At the time of 0.1mW output
Consumption current PLL	IPLL	-	0.8	2.5	mA	
Output amplitude error	Vout	-2	-	2	dB	Errors with reference to standard values at the time of 0dBFS output are as follows
Channel-to-channel gain error	Gerr	-1	-	1	dB	Lch-Rch
S/N	SN	60	80	-	dB	0dBFS, A-Weight
THD+N	THD	-40	-60	-	dB	-3dBFS, A-Weight
Channel-to-channel isolation	Iso	65	80	-	dB	0dBFS, 1kHz BPF
PSRR	Psrr	-	0	-	dB	

<S/N measuring method>

Measure the level ratio of the respective integral values of the signals and noise within the band of 20kHzLPF +A-Weight.

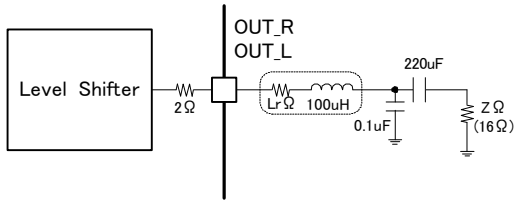
<THD+N measuring method>

Measure the level ratio of the total harmonic component + (plus) noise and the basic wave frequency component within the band of 20kHzLPF +A-Weight.

●Output amplitude error

Output amplitude is determined by the equivalent series resistance of external coil. Let Lr, VDD and Z respectively stand for the equivalent series resistance, the power supply voltage value of VDD_R,VDD_L and the load impedance, the standard value of output amplitude becomes the following equation:

Standard value of output amplitude [Vpp] = VDD x 0.5 x Z / (Lr + Z + 2)



Shown in the following table is the standard values of output amplitude if VDD=2.8V, Load impedance Z=16Ω, and Equivalent series resistance is 0.7Ω, 4Ω or 7Ω.

Equivalent series resistance [Ω]	Standard value of output amplitude [Vpp]	Standard value of output amplitude [dBv]	Output power [mW]
0.0	1.24	-7.13	12.10
0.7	1.20	-7.46	11.21
4.0	1.02	-8.87	8.10
7.0	0.90	-9.98	6.27

●DC characteristic

Ta=25degree,DVDD=DVDDIO=1.5V, VDD_R=VDD_L=PLLVDD=2.8V

Item	Symbol	Standardized values			Unit	Note
		MIN	TYP	MAX		
Input 'H' Level	VIH	0.7x DVDDIO	-	-	V	
Input 'L' Level	VIL	-	-	0.3x DVDDIO	V	
Output 'H' Level	VOH	0.8x DVDDIO	-	-	V	Io=-1mA
Output 'L' Level 1	VOL1	-	-	0.2x DVDDIO	V	Io=1mA
Output 'L' Level 2 (SDA terminal)	VOL2	-	-	0.2x DVDDIO	V	Io=3mA

Table 10 DC characteristic

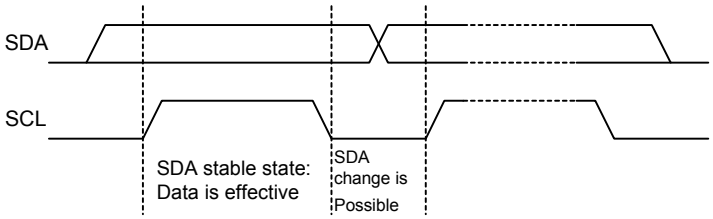
●2wire CPU I/F Part

Device address is "0110011"(33h) or "0110110"(36h), i.e. 33h when ADR terminal is L or 36h when ADR terminal is H.
Please don't switch the ADR terminal while 2wire CPU I/F is operating.
The transmission rate is compatible with a maximum of 400kbps

ADR	2wire CPU I/F device address							W/R
	A7	A6	A5	A4	A3	A2	A1	
0	0	1	1	0	0	1	1	0/1
1	0	1	1	0	1	1	0	0/1

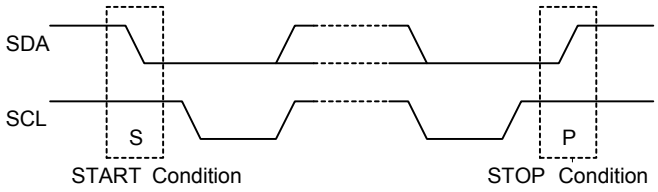
・Bit transmission

The data of 1bit is transmitted while SCL is H. In case of bit transmission, the signal transition of SDA can not be implemented while SCL is H.
If SDA changes while SCL is H, START condition or STOP condition is generated, it is interpreted as control signal.



・START condition/STOP condition

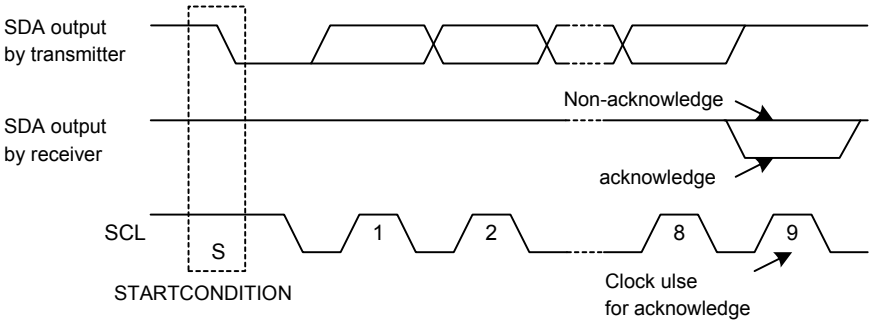
Data transmission on bus is not implemented while SDA and SCL are H. At this time, if SCL remains to be H and SDA is transited from H to L, then the START condition (S) is attained and so the access is started, and if SCL remains to be H and SDA is transited from L to H, then the STOP condition (P) is attained and so the access is terminated, which is shown below.



This device accepts the continuous START condition and the continuous STOP condition.

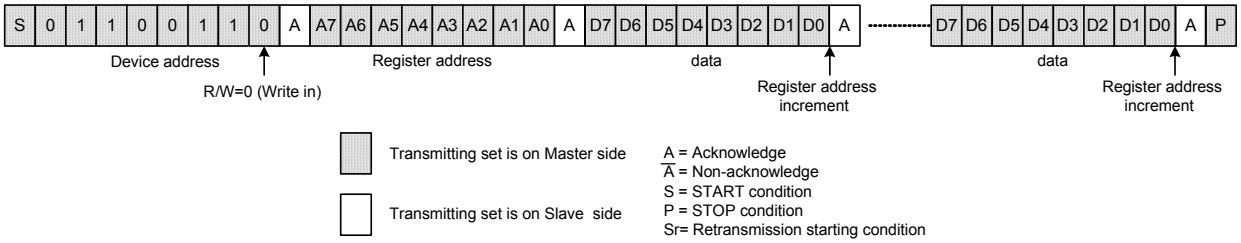
・Acknowledge

After START condition is generated, data is transmitted at 8 bits once. After 8 bit transmission, the transmitter opens SDA, and the receiver returns the acknowledge signal with SDA taken as L.



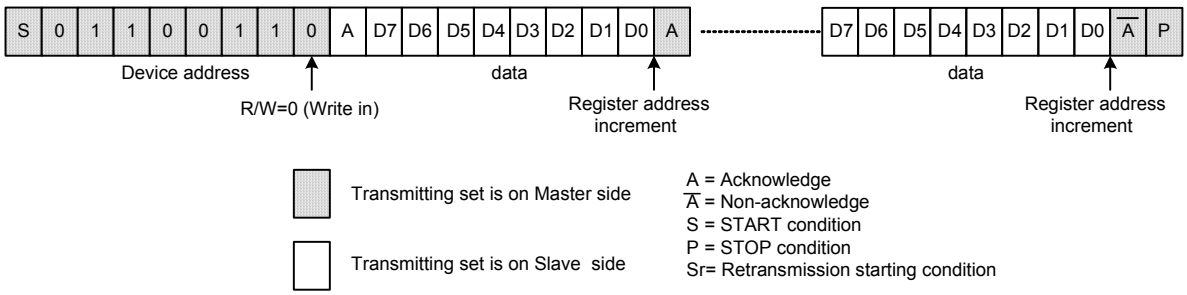
・Write protocol

Write protocol is shown below. Register address is transmitted by 1 byte after device address and write command have been transmitted. Third byte writes the data, which is written in by second byte, into internal register, and for fourth byte and subsequent bytes, the register address is incremented automatically. But, the register address becomes 00h by the transmission of 1 byte after the register address has become the final address (6Ch). The address is incremented after the transmission is over.



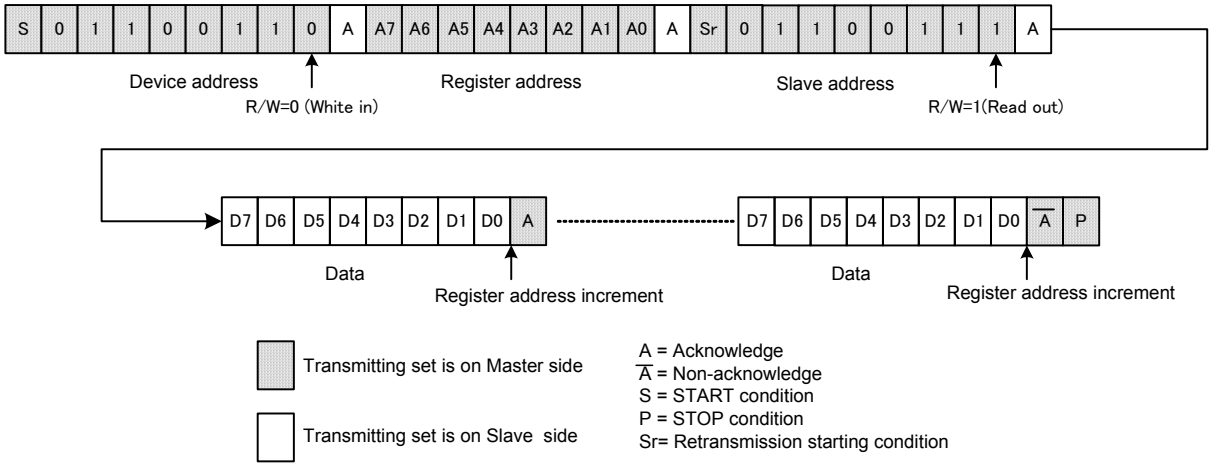
・Readout protocol

Readout starts from 1 byte after device address and R/W bit have been written in. For the address after the readout register is finally accessed and the subsequent addresses, the data of the addresses that have been incremented is read out. As the readout of 1 byte after the address has become the final address, 00h is read out. The address is incremented after the transmission is over.

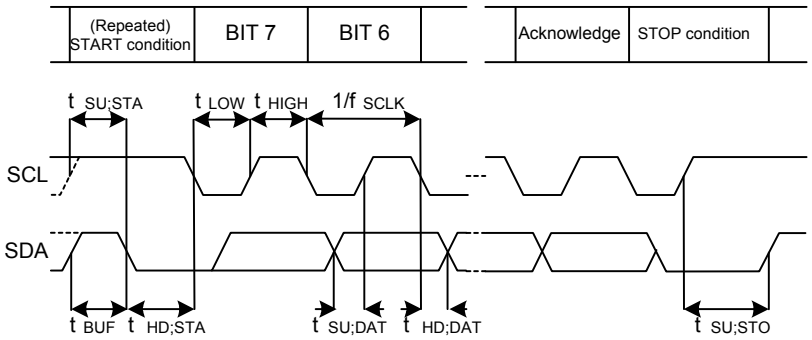


・Compound readout protocol

After internal address is specified, create the retransmission starting condition, change the data transmitting direction and implement the readout. Subsequently, the data of the address that has been incremented is read out. As the readout of 1 byte after the address has become the final address, 00h is read out. The address is incremented after the transmission is over. After retransmission starting condition, compound write is possible with R/W=0 (write in).



・Timing diagram



Ta=25 degree,DVDD=DVDDIO=1.8V, VDD_R=VDD_L=PLLVDD=3.0V

Item	Symbol	Standard mode		High-speed mode		Unit
		min	max	min	max	
SCL clock frequency	f_{SCLK}	0	100	0	400	kHz
Hold time of START condition	$t_{HD;STA}$	4.0	-	0.6	-	μs
" L " Level time of SCL	t_{LOW}	4.7	-	1.3	-	μs
"H" Level time of SCL	t_{HIGH}	4.0	-	0.6	-	μs
Setup time of repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	μs
Data hold time ※1	$t_{HD;DAT}$	0.1	3.45	0.1	0.9	μs
Data setup time	$t_{SU;DAT}$	250	-	100	-	ns
Setup time of STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	μs
Bus opening time between STOP condition and START condition	t_{BUF}	4.7	-	1.3	-	μs

*1 The maximum $t_{HD;DAT}$ is not allowed to exceed the “L” level time （t_{LOW}） of SCL signal

●Audio I/F part

■At slave mode.
Ta=25degree ,DVDD=DVDDIO=1.5V, VDD_R=VDD_L=PLLVDD=2.8 V

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
MCLK frequency *1	Fmclk	2.048	-	18.432	MHz	Fmclk = 256fs or 384fs
MCLK Duty Cycle	Dmclk	40	-	60	%	
BCLK frequency	Fbclk	0.512	-	3.072	MHz	Fbclk = 64fs
BCLK Duty Cycle	Dbclk	40	-	60	%	
LRCLK frequency	Flrclk	8	-	48	kHz	Flrclk = 1fs
LRCLK Hold Time	Thdlr	80	-	-	ns	
SDI Setup Time	Tsusdi	80	-	-	ns	
SDI Hold Time	Thdsdi	80	-	-	ns	

*1 It is not necessary to adjust the phase of MCLK and BCLK and LRCLK, but it is necessary to be something related to synchronization

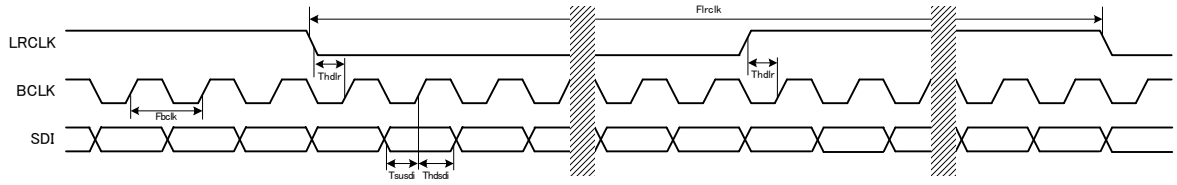


Fig.5 Audio I/F AC timing(at slave mode)

■At master mode
Ta=25degree,DVDD=DVDDIO=1.5V, VDD_R=VDD_L=PLLVDD=2.8V

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
BCLK frequency	Fbclk	0.512	-	3.072	MHz	Fbclk = 64fs
LRCLK frequency	Flrclk	8	-	48	kHz	Flrclk = 1fs
SDI Setup Time	Tsusdi	80	-	-	ns	
SDI Hold Time	Thdsdi	80	-	-	ns	

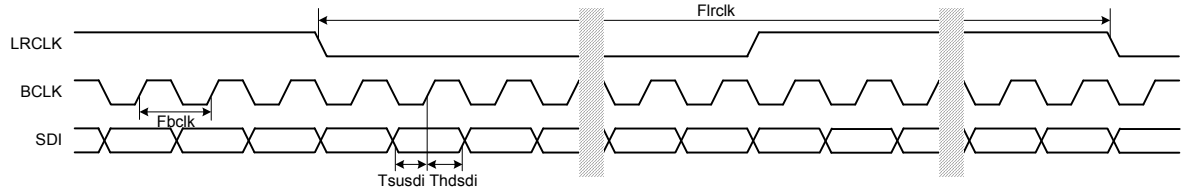
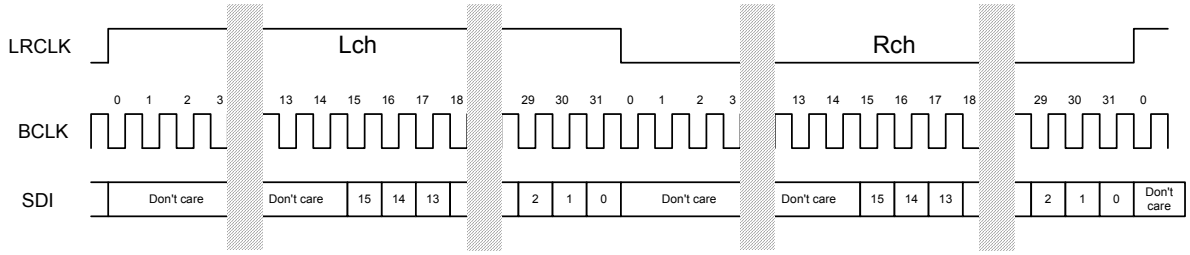


Fig.6 Audio I/F AC timing(at master mode)

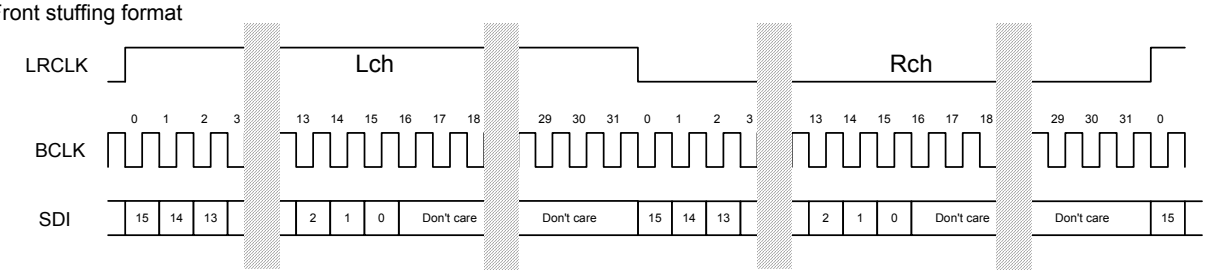
●Audio I/F format

・At bit[1:0]=”00” (16bit length)

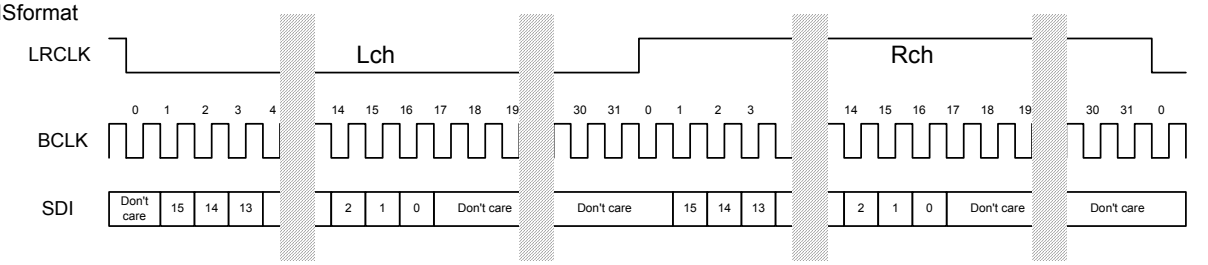
■Rear stuffing format



■Front stuffing format

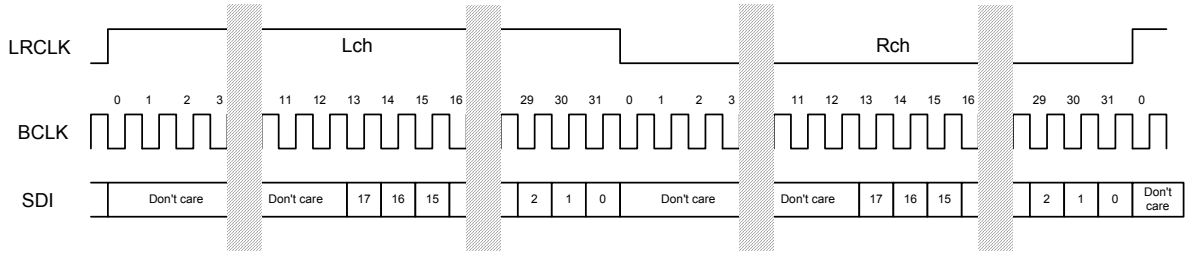


■IISformat

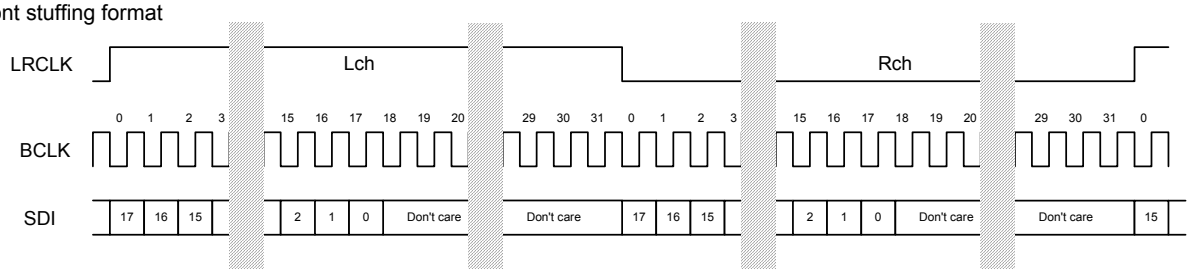


・At bit[1:0]=”01” (18bit length)

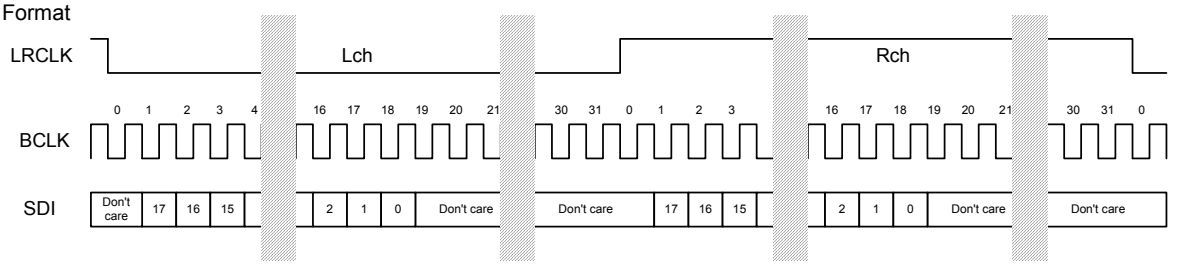
■Rear stuffing Format



■Front stuffing format

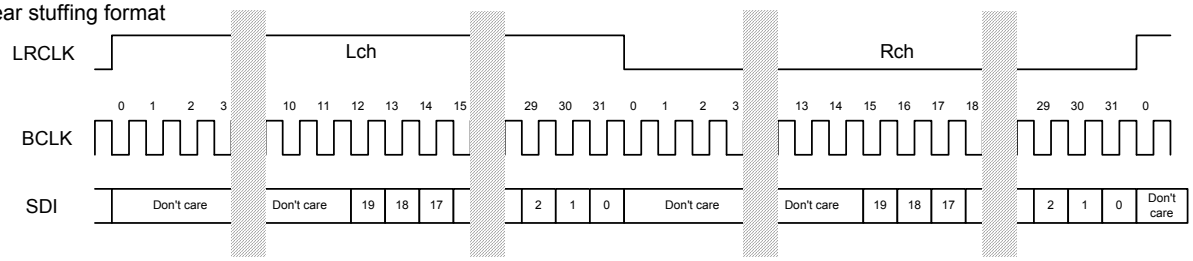


■IIS Format

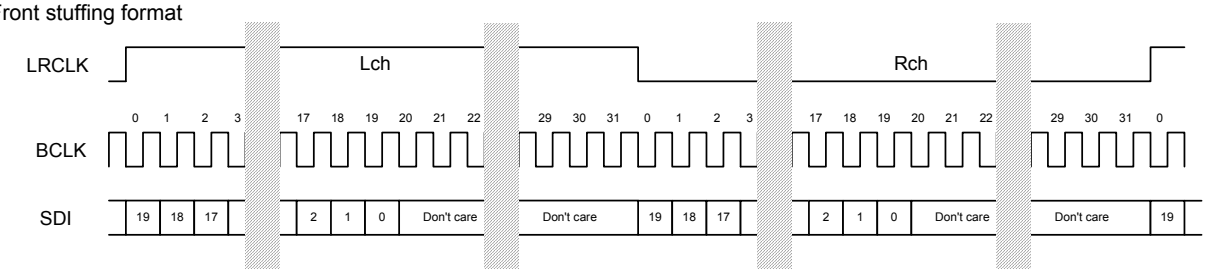


・At bit[1:0]=”10” (20bit length)

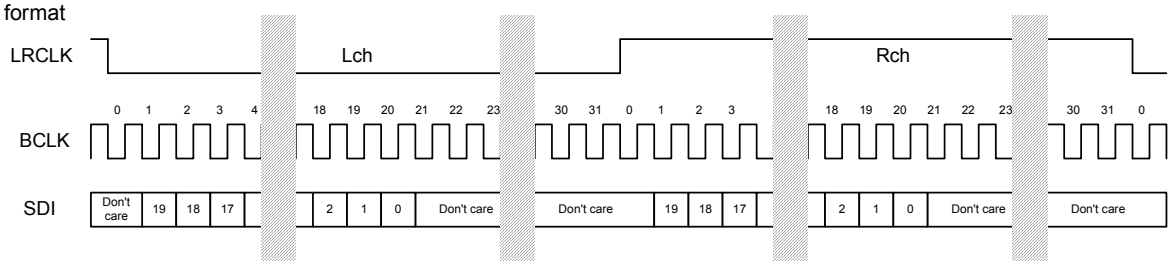
■Rear stuffing format



■Front stuffing format

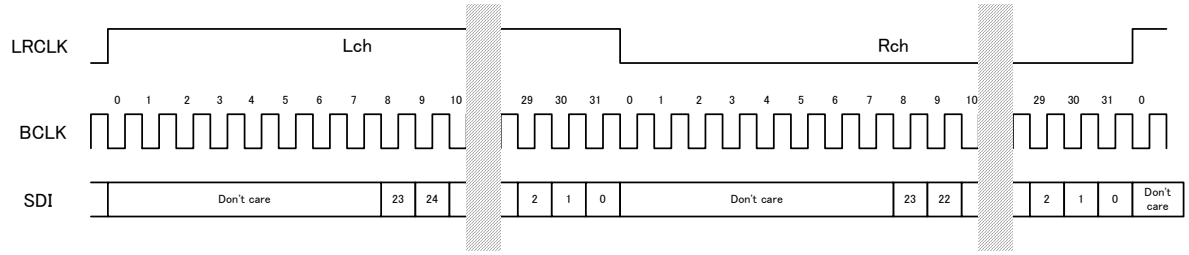


■IIS format

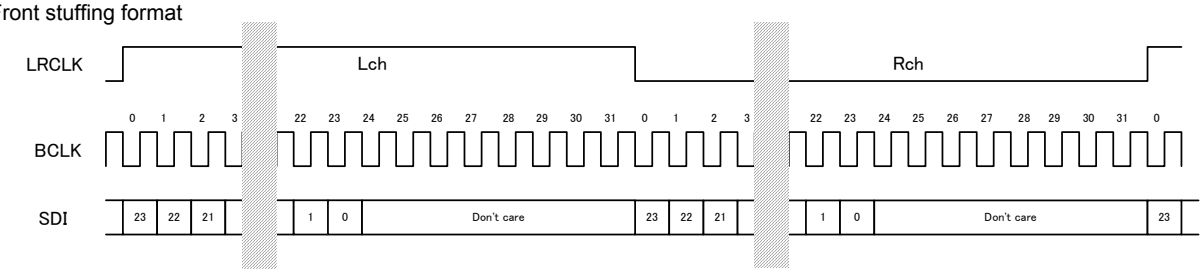


・At bit[1:0]=”11” (24bit length)

■Rear stuffing format



■Front stuffing format



■IIS format

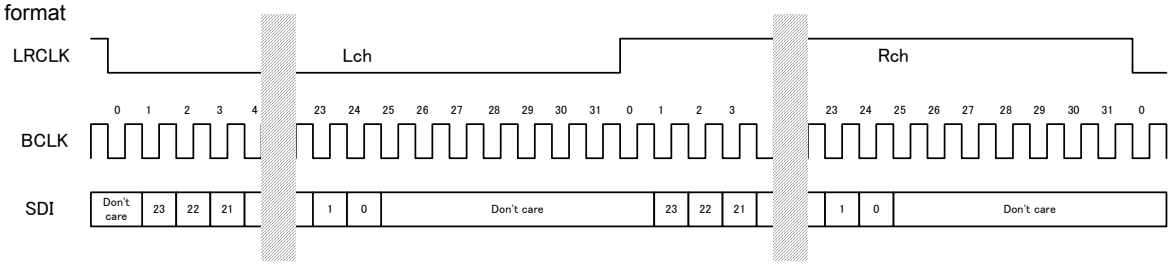


Fig.7 Audio I/F Format

●PLL Part

Ta=25degree,DVDD=DVDDIO=1.5V, VDD_R=VDD_L=PLLVDD=2.8V, REFCLK=12MHz, fs=44.1kHz

Item	Symbol	specification			Unit	Condition
		MIN	TYP	MAX		
Lock up time	Tlock	-	-	15	msec	
BCLK Duty Cycle	Dbclk	40	-	60	%	

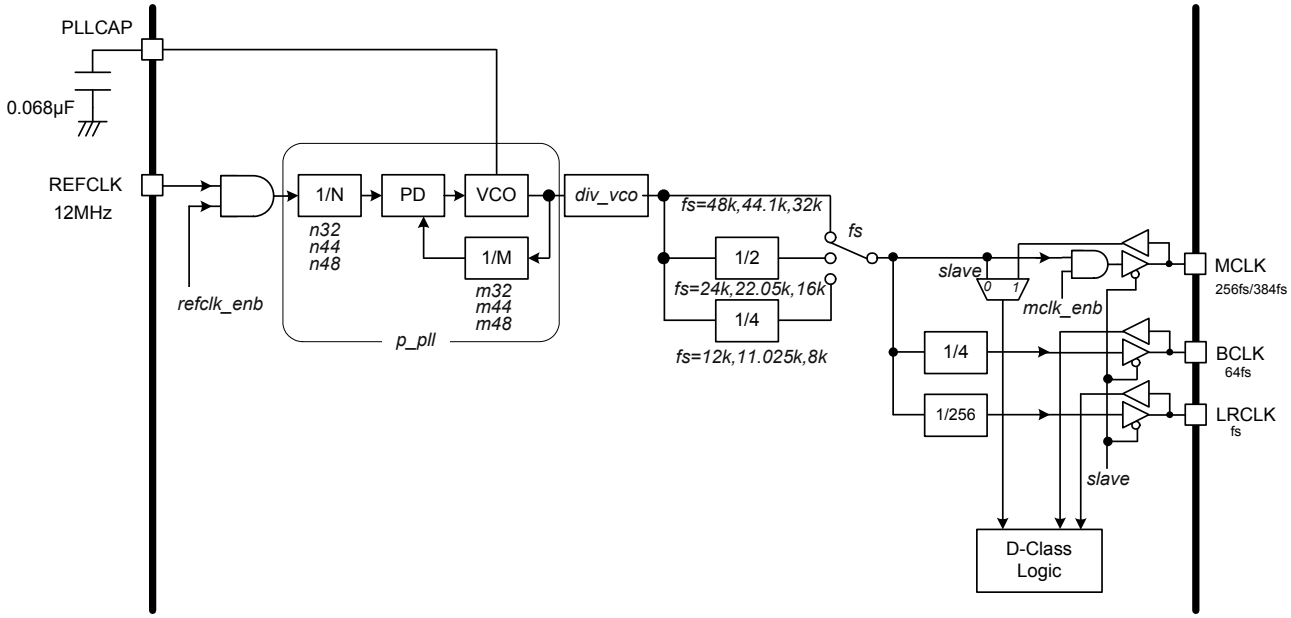


Fig.8 Block diagram of PLL part

●Ordering part number

B	U	7	8	3	9	G	V	W	-	E	2

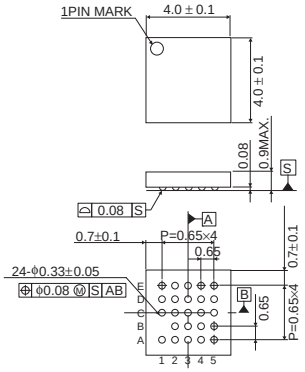
Part No. (BU)

Part No. (7839)

Package
GVW:SBGA024W040

Packaging and forming specification
E2: Embossed tape and reel

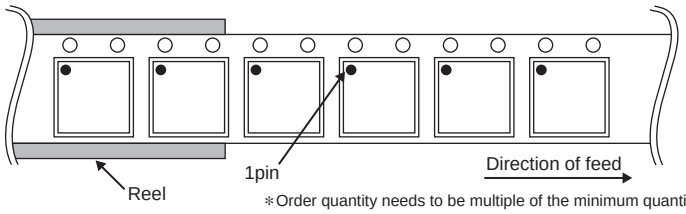
SBGA024W040



(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

No copying or reproduction of this document, in part or in whole, is permitted without the consent of ROHM Co.,Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing ROHM's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from ROHM upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, ROHM shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. ROHM does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by ROHM and other parties. ROHM shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While ROHM always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. ROHM shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). ROHM shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.

ROHM SEMICONDUCTOR

Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact us.

ROHM Customer Support System

http://www.rohm.com/contact/