BLF8G20LS-260A

Power LDMOS transistor

Rev. 1 — 13 September 2012 Objective data sheet

1. Product profile

1.1 General description

260 W LDMOS packaged asymmetrical Doherty power transistor for base station applications at frequencies from 1805 MHz to 1880 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in an asymetric Doherty production test circuit.

Test signal	f (MHz)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR (dBc)
2-carrier W-CDMA[2]	1805 to 1880	28	50	15.5	43	−23[1]

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 7.5 dB at 0.01% probability on CCDF per carrier, carrier spacing 5 MHz.

[2] I_{Dq} = 750 mA (main); $V_{GS(amp)peak}$ = 0.80 V.

1.2 Features and benefits

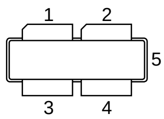
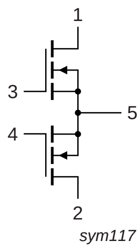
- Excellent ruggedness
- High-efficiency
- Low R_{th} providing excellent thermal stability
- Designed for broadband operation (1805 MHz to 1880 MHz)
- Asymmetrical design to achieve optimum efficiency across the band
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for W-CDMA base stations and GSM multi carrier applications in the 1805 MHz to 1880 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1 (main)		
2	drain2 (peak)		
3	gate1 (main)		
4	gate2 (peak)		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF8G20LS-260A	-	earless flanged balanced ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		−0.5	+13	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		−0.5	+13	V
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	V_{DS} = 28 V; I_{Dq} = 750 mA (main); $V_{GS(amp)peak}$ = 0.80 V; T_{case} = 80 °C		
		P_L = 50 W	0.36	K/W
		P_L = 200 W	0.29	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.44 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 144 mA	1.50	1.88	2.30	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	27	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 7.20 A	-	10.8	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 5.04 A	-	0.102	-	Ω
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.2 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 220 mA	1.50	1.80	2.30	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	40	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 11.0 A	-	15.9	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 7.7 A	-	0.067	-	Ω

Table 7. RF characteristics

Test signal: 2-carrier W-CDMA; PAR = 7.5 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 - 64 DPCH; f_1 = 1807.5 MHz; f_2 = 1812.5 MHz; f_3 = 1872.5 MHz; f_4 = 1877.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 750 mA (main); $V_{GS(amp)peak}$ = 0.80 V; T_{case} = 25 °C; unless otherwise specified; in an asymetric Doherty production test circuit in 1805 MHz to 1880 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 50 W	<tbd>	15.5	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 50 W	-	−10	<tbd>	dB
η_D	drain efficiency	$P_{L(AV)}$ = 50 W	<tbd>	43	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 50 W	-	−23	<tbd>	dBc

7. Test information

7.1 Ruggedness in class-AB operation

The BLF8G20LS-260A is capable of withstanding a load mismatch corresponding to a VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 750 mA (main); $V_{GS(amp)peak}$ = 0.80 V; P_L = 200 W (CW); f = 1805 MHz to 1880 MHz.

7.2 Impedance information

Table 8. Typical impedance of main device

Measured load-pull data of main device; I_{Dq} = 750 mA (main); V_{DS} = 28 V.

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)	$P_{L(3dB)}$ (W)	η_D [2] (%)	G_p [2] (dB)
Peak power load					
1810	0.9 – j3.3	1.4 – j3.9	191	59	15.5
1840	0.8 – j3.4	1.4 – j3.9	182	58	15.7
1880	0.8 – j3.7	1.4 – j3.9	182	58	15.6
Peak drain efficiency load					
1810	0.9 – j3.3	2.3 – j2.7	138	70	17.9
1840	0.8 – j3.4	2.5 – j2.5	123	69	18.5
1880	0.8 – j3.7	2.1 – j2.5	127	68	18.0

[1] Z_S and Z_L defined in Figure 1.

[2] at 3 dB gain compression.

Table 9. Typical impedance of peak device

Measured load-pull data of peak device; I_{Dq} = 1200 mA (peak); V_{DS} = 28 V.

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)	$P_{L(3dB)}$ (W)	η_D [2] (%)	G_p [2] (dB)
Peak power load					
1810	0.8 – j3.5	1.7 – j4.0	257	61	16.0
1840	0.8 – j3.8	1.9 – j4.3	257	59	15.8
1880	0.8 – j3.9	1.9 – j4.3	251	59	16.2
Peak drain efficiency load					
1810	0.8 – j3.5	2.5 – j2.5	178	70.0	18.6
1840	0.8 – j3.8	2.5 – j2.5	180	70.0	18.5
1880	0.8 – j3.9	2.3 – j2.7	182	68.0	18.8

[1] Z_S and Z_L defined in Figure 1.

[2] at 3 dB gain compression.

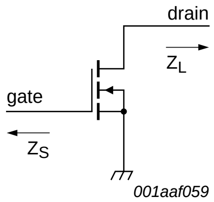
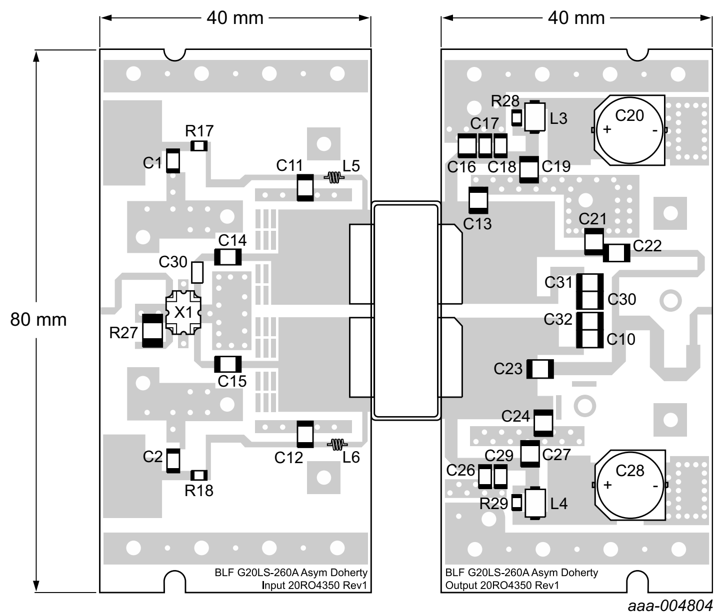


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350; thickness = 0.508 mm.

See Table 10 for list of components.

Fig 2. Component layout for test circuit

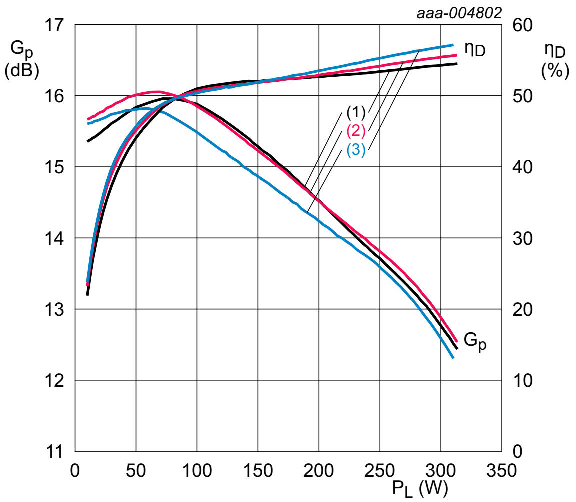
Table 10. List of components

For test circuit, see Figure 2.

Component	Description	Value	Remarks
C11, C12, C14, C15, C16, C22, C23, C25, C31	multilayer ceramic chip capacitor	30 pF	ATC100B
C13	multilayer ceramic chip capacitor	0.5 pF	ATC800B
C17, C26	multilayer ceramic chip capacitor	100 nF	Murata
C18, C29	multilayer ceramic chip capacitor	1 μF	Murata
C19, C27, C30, C32	multilayer ceramic chip capacitor	10 μF	Murata
C20, C28	electrolytic capacitor	2200 μF	Panasonic
C21	multilayer ceramic chip capacitor	0.3 pF	ATC800B
C24	multilayer ceramic chip capacitor	1.2 pF	ATC800B
R27	resistor	50 Ω	EMC
R28, R29	resistor	9.1 Ω	Vishay Dale
R30	resistor	9.1 Ω	1206
L3, L4	ferrite bead	-	Fair Rite 2743019447
L5, L6	inductor	12 nH	Coilcraft
X1	hybrid coupler	-	Anaren X3C19P1-03S

7.4 Graphical data

7.4.1 CW pulsed



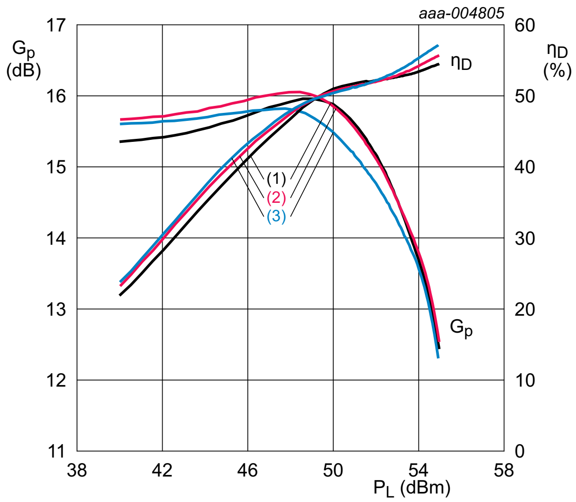
V_{DS} = 28 V; $V_{GS(amp)main}$ = 2.208 V; I_{Dq} = 746 mA; $V_{GS(amp)peak}$ = 0.80 V.

(1) f = 1805 MHz

(2) f = 1842.5 MHz

(3) f = 1880 MHz

Fig 3. Power gain and drain efficiency as function of load power; typical values



V_{DS} = 28 V; $V_{GS(amp)main}$ = 2.208 V; I_{Dq} = 746 mA; $V_{GS(amp)peak}$ = 0.80 V.

(1) f = 1805 MHz

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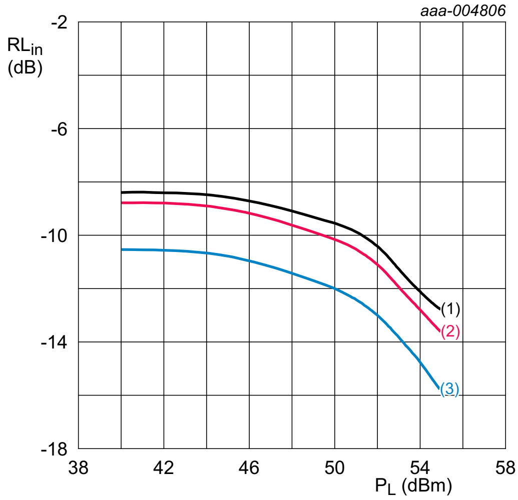
Fig 4. Power gain and drain efficiency as function of load power; typical values



V_{DS} = 28 V; $V_{GS(amp)main}$ = 2.208 V; I_{Dq} = 746 mA; $V_{GS(amp)peak}$ = 0.80 V.

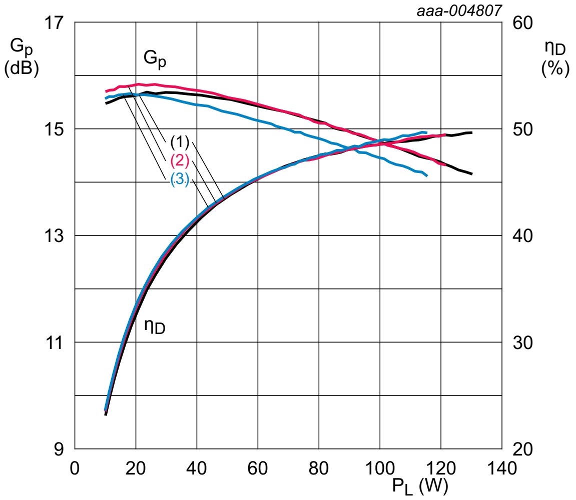
(1) f = 1805 MHz

(2) f = 1842.5 MHz

(3) f = 1880 MHz

Fig 5. Input return loss as a function of load power; typical values

7.4.2 2-Carrier W-CDMA



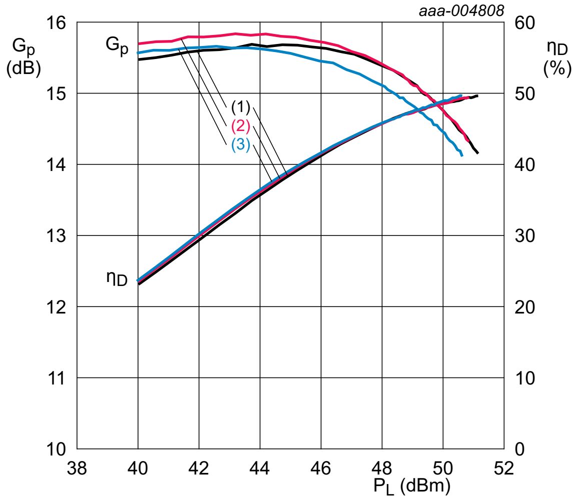
V_{DS} = 28 V; $V_{GS(amp)main}$ = 2.208 V; I_{Dq} = 746 mA; $V_{GS(amp)peak}$ = 0.80 V.

(1) f = 1807.5 MHz

(2) f = 1842.5 MHz

(3) f = 1877.5 MHz

Fig 6. Power gain and drain efficiency as function of load power; typical values



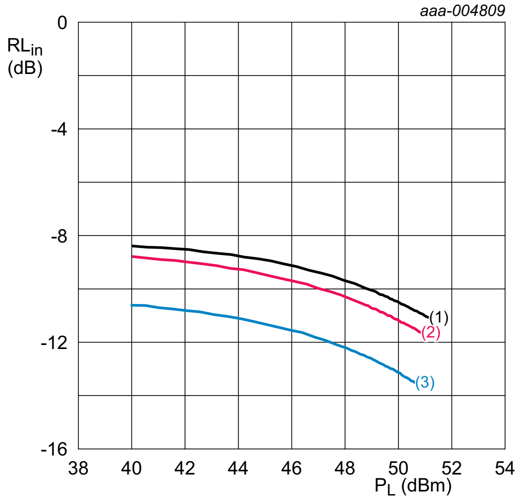
V_{DS} = 28 V; $V_{GS(amp)main}$ = 2.208 V; I_{Dq} = 746 mA; $V_{GS(amp)peak}$ = 0.80 V.

(1) f = 1805 MHz

(2) f = 1842.5 MHz

(3) f = 1880 MHz

Fig 7. Power gain and drain efficiency as function of load power; typical values



V_{DS} = 28 V; $V_{GS(amp)main}$ = 2.208 V; I_{Dq} = 746 mA; $V_{GS(amp)peak}$ = 0.80 V.

(1) f = 1807.5 MHz

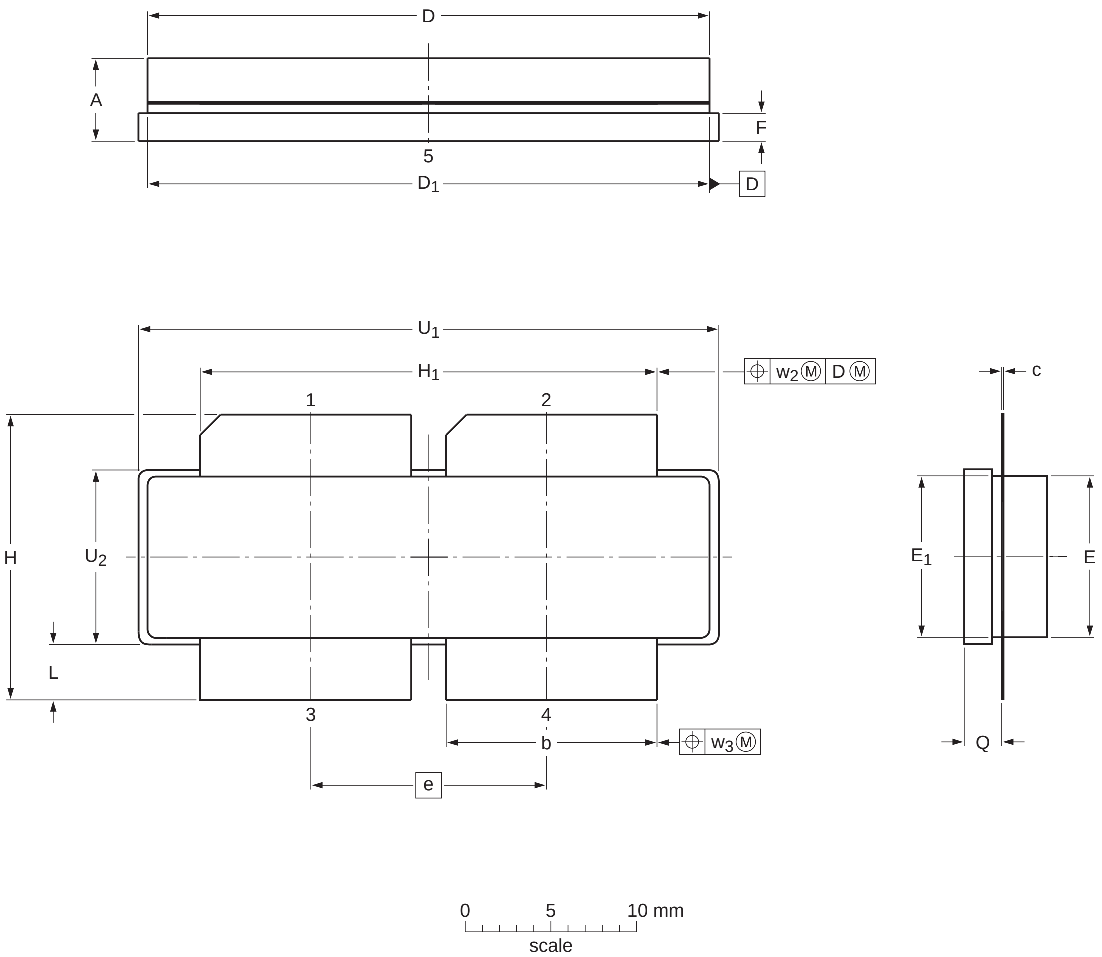
(2) f = 1842.5 MHz

(3) f = 1877.5 MHz

Fig 8. Input return loss as a function of load power; typical values

8. Package outline

Earless flanged balanced ceramic package; 4 leads **SOT539B**



Dimensions

Unit(1)		A	b	c	D	D_1	E	E_1	e	F	H	H_1	L	Q	U_1	U_2	w_2	w_3
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53		1.75	17.12	25.53	3.48	2.26	32.39	10.29		
	nom								13.72								0.25	0.25
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	2.01	32.13	10.03		
mm	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375		0.069	0.674	1.005	0.137	0.089	1.275	0.405		
	nom								0.54								0.01	0.01
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.079	1.265	0.395		

Note

1. millimeter dimensions are derived from the original inch dimensions.

sot539b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539B						~~11-10-28~~ 12-05-02

Fig 9. Package outline SOT539B

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
GSM	Global System for Mobile communications
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
PAR	Peak-to-Average Ratio
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF8G20LS-260A v.1	20120913	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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