

**HIGH SENSITIVITY CMOS HALL-EFFECT LATCH****AH921****General Description**

The AH921 is a Hall-effect latch designed in mixed signal CMOS technology. It is quite suitable for use in automotive, industrial and consumer applications.

Superior high-temperature performance is made possible through dynamic offset cancellation, which reduces the residual offset voltage normally caused by device over-molding, temperature dependencies, and thermal stress. The device integrates a voltage regulator, Hall-voltage generator, small-signal amplifier, chopper stabilization, schmitt trigger, and is directly drivable by the output.

An on-board regulator permits operation with supply voltage from 3.5V to 24V.

The AH921 is available in TO-92S-3 and SOT-23-3 packages, which are optimized for most applications.

**Features**

- Wide Operating Voltage Range from 3.5 to 24V
- Symmetrical Switch Points
- Chopper-stabilized Amplifier Stage
- Superior Temperature Stability
- Compact Size
- Built-in Pull-up Resistor
- ESD Rating: 3500V (Human Body Model)

**Applications**

- Brushless DC Motor Commutation
- Brushless DC Fan
- Solid-state Switch
- Revolution Counting
- Speed Detection
- High Sensitivity and Unconnected Switch

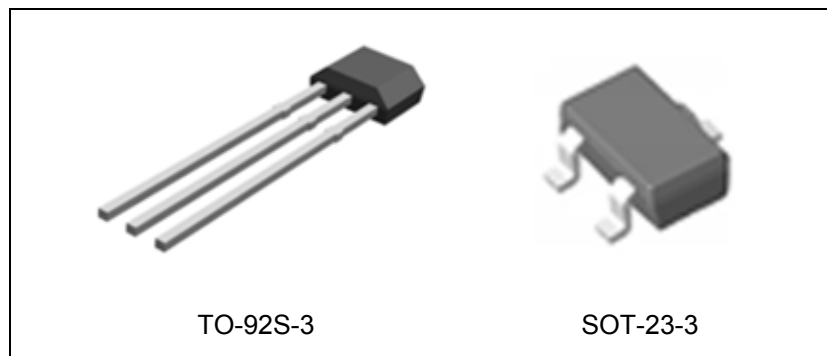


Figure 1. Package Types of AH921

**HIGH SENSITIVITY CMOS HALL-EFFECT LATCH**

**AH921**

**Pin Configuration**

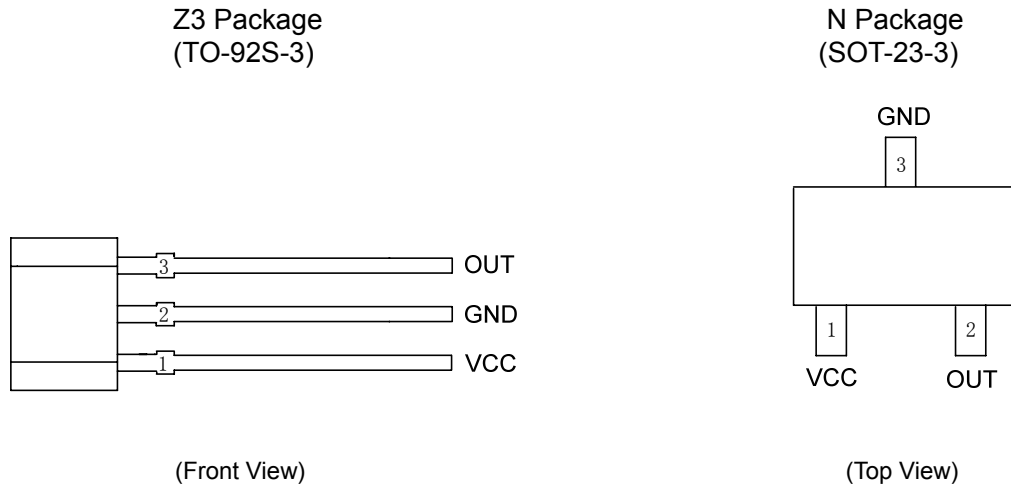


Figure 2. Pin Configuration of AH921

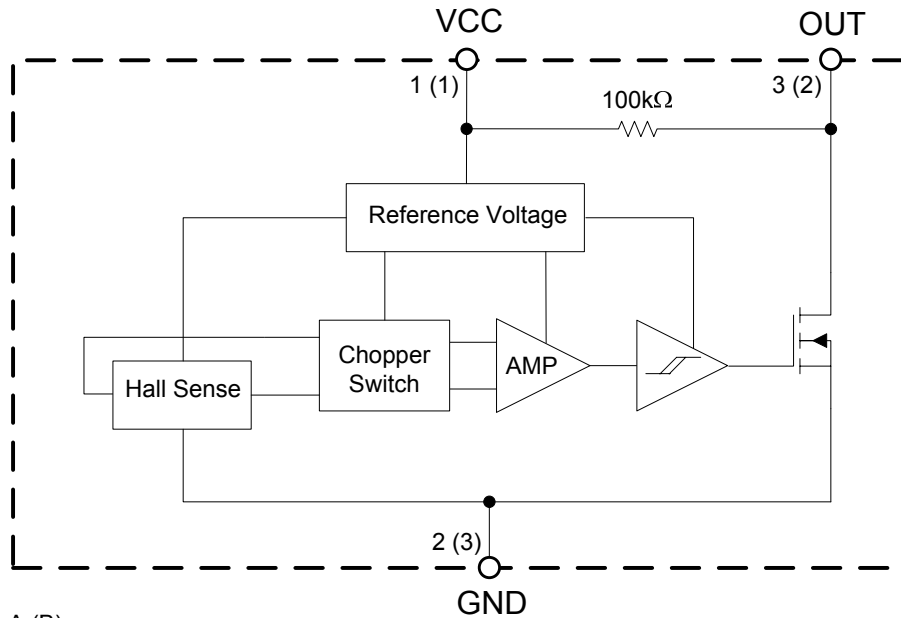
**Pin Description**

Pin Number		Pin Name	Function
TO-92S-3	SOT-23-3		
1	1	VCC	Supply voltage
2	3	GND	Ground pin
3	2	OUT	Output pin

**HIGH SENSITIVITY CMOS HALL-EFFECT LATCH**

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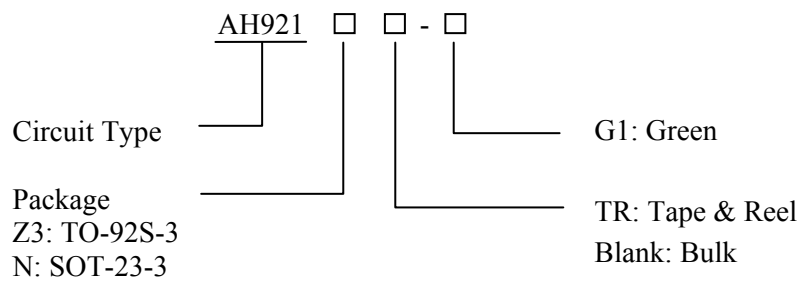
**Functional Block Diagram**



A (B)  
A for TO-92S-3  
B for SOT-23-3

Figure 3. Functional Block Diagram of AH921

**Ordering Information**



Package	Temperature Range	Part Number	Marking ID	Packing Type
TO-92S-3	-40 to 125°C	AH921Z3-G1	921	Bulk
SOT-23-3		AH921NTR-G1	GS6	Tape & Reel

BCD Semiconductor's Pb-free products, as designated with "G1" suffix in the part number, are RoHS compliant and green.

**HIGH SENSITIVITY CMOS HALL-EFFECT LATCH****AH921****Absolute Maximum Ratings (Note 1)**

Parameter	Symbol	Value		Unit
Supply Voltage	$V_{CC}$	28		V
Supply Current (Fault)	$I_{CC}$	5		mA
Output current (Continuous)	$I_{OUT}$	25		mA
Power Dissipation	$P_D$	TO-92S-3	400	mW
		SOT-23-3	230	
Operating Temperature	$T_A$	-50 to 150		°C
Storage Temperature	$T_{STG}$	-65 to 150		°C
Maximum Junction Temperature	$T_J(\text{Max})$	165		°C
ESD (Human Body Model)	ESD	3500		V

Note 1: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

**Recommended Operating Conditions**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	$V_{CC}$	3.5	24	V
Operating Temperature	$T_A$	-40	125	°C

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**AH921**
**Electrical Characteristics**
 $V_{CC}=12V$ ,  $T_A=25^{\circ}C$ , unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	$V_{CC}$	Operating	3.5	12	24	V
Supply Current	$I_{CC}$	$V_{CC}=12V$ , $B < B_{RP}$		3.0	5.0	mA
		$V_{CC}=12V$ , $B > B_{OP}$		3.0	5.0	mA
Saturation Voltage	$V_{SAT}$	$I_{OUT}=20mA$ , $B > B_{OP}$		185	500	mV
Output Leakage Current	$I_{LEAKAGE}$	$V_{CC}=V_{OUT}=24V$ , $B < B_{RP}$		0.1	10	$\mu A$
Output Rising Time	$t_{RISING}$	$C_L=20pF$		0.4	2	$\mu s$
Output Falling Time	$t_{FALLING}$	$C_L=20pF$		0.4	2	$\mu s$

**Magnetic Characteristics**
 $V_{CC}=12V$ ,  $T_A=25^{\circ}C$ , unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit
Operating Point	$B_{OP}$	5	22	40	Gauss
Releasing Point	$B_{RP}$	-40	-22	-5	Gauss
Hysteresis	$B_{HYS}$		45		Gauss

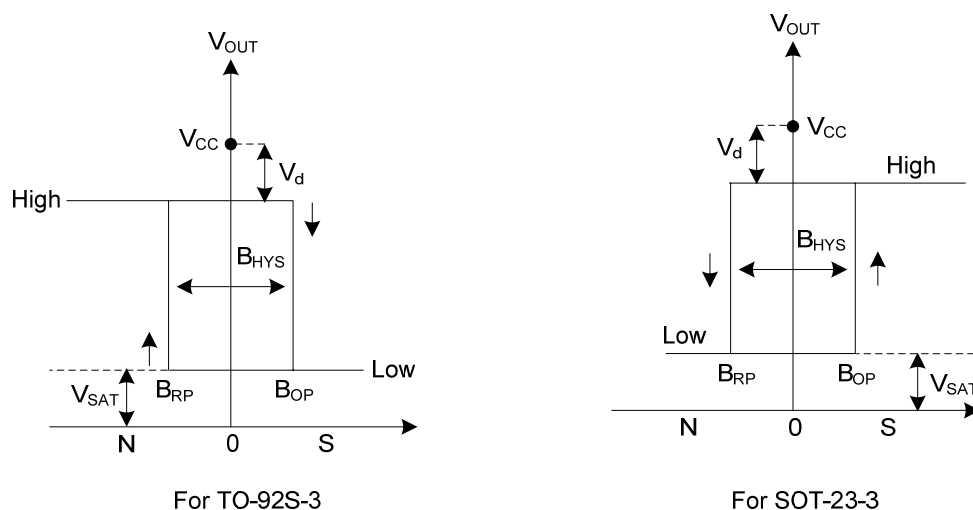


Figure 4. Magnetic Flux Density of AH921

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**Magnetic Characteristics (Continued)**

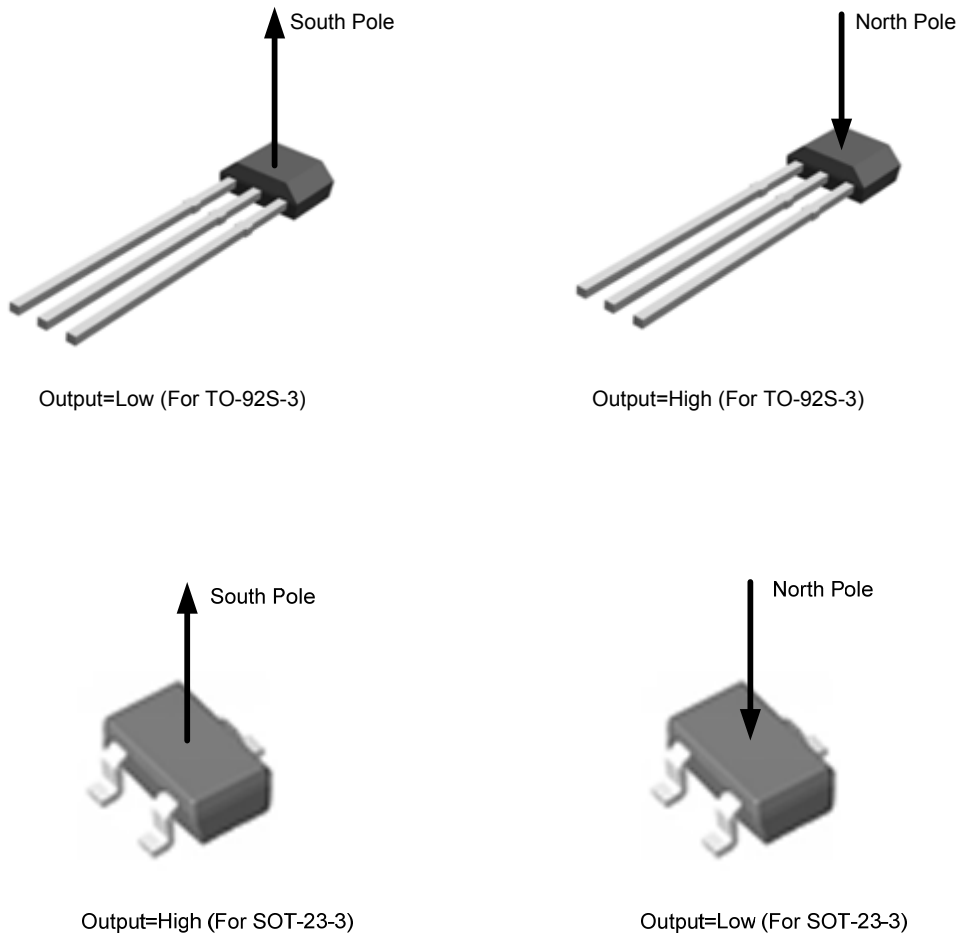


Figure 5. Output Status vs. Magnetic Pole

Package Type	Parameter	Test condition	Output
TO-92S-3	South Pole	$B > B_{OP}$	Low
	North Pole	$B < B_{RP}$	High
SOT-23-3	South Pole	$B > B_{OP}$	High
	North Pole	$B < B_{RP}$	Low

Table 1. Output Status vs. Magnetic Pole

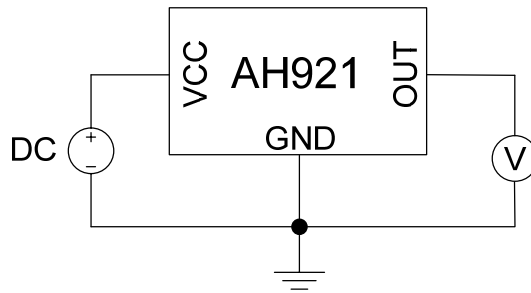
**Magnetic Characteristics (Continued)**


Figure 6. Magnetic Thresholds

Note 2:  $B_{OP}$  is determined by putting the device under magnetic field swept from  $B_{RP}(\text{Min})$  to  $B_{OP}(\text{Max})$  until the output is switched on.

Note 3:  $B_{RP}$  is determined by putting the device under magnetic field swept from  $B_{OP}(\text{Max})$  to  $B_{RP}(\text{Min})$  until the output is switched off.

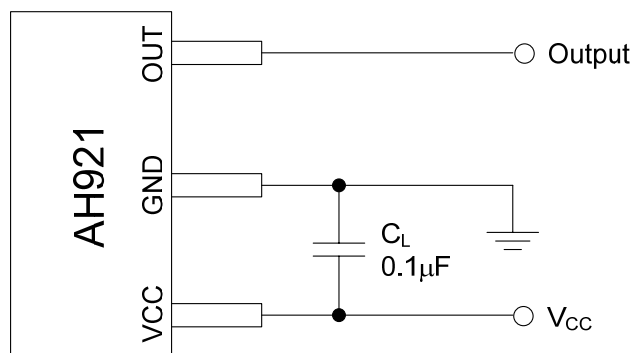
**Test Circuit and Test Conditions**


Figure 7. Test Circuit of AH921

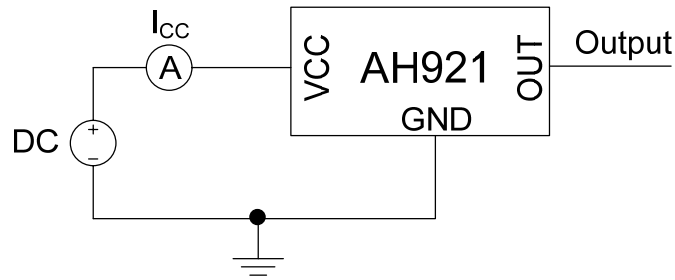
**Test Circuit and Test Conditions (Continued)**


Figure 8. Test Condition of AH921 (Supply Current)

Note 4: Output initial status is low when powering on.

Note 5: The supply current  $I_{CC}$  represents the average supply current. The output is open during measurement.

Note 6: The device is put under the magnetic field:  $B < B_{RP}$ .

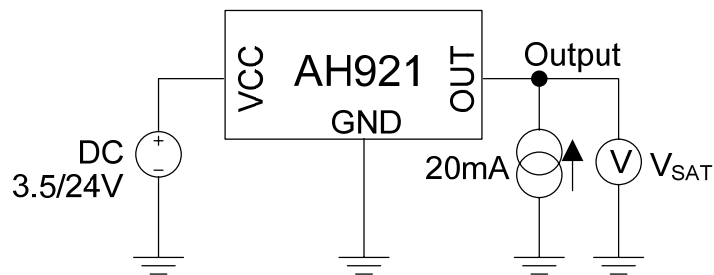


Figure 9. Test Condition of AH921 (Output Saturation Voltage)

Note 7: The output saturation voltage  $V_{SAT}$  is measured at  $V_{CC}=3.5V$  and  $V_{CC}=24V$ .

Note 8: The device is put under the magnetic field:  $B > B_{OP}$ .



**Test Circuit and Test Conditions (Continued)**

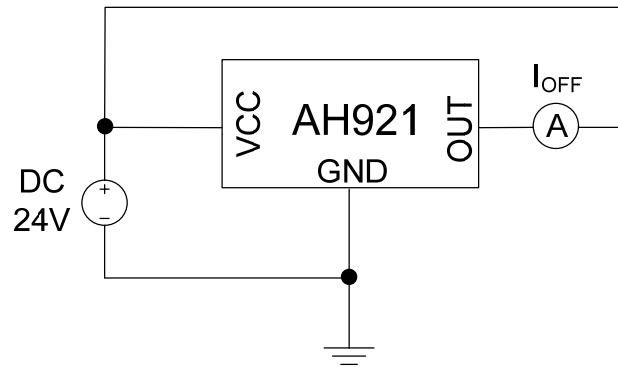


Figure 10. Test Condition of AH921 (Output Leakage Current)

Note 9: The device is put under the magnetic field:  $B < B_{RP}$ .

**Typical Performance Characteristics**

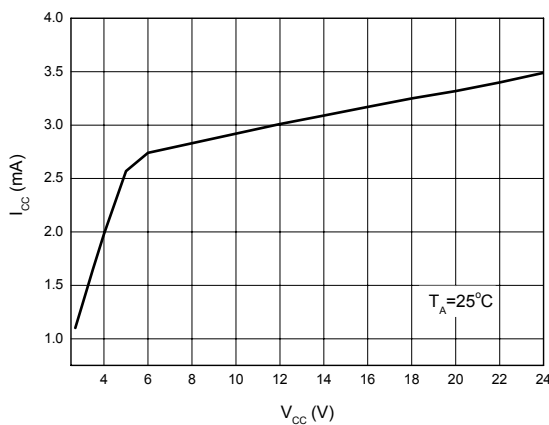


Figure 11. I<sub>CC</sub> vs. V<sub>CC</sub>

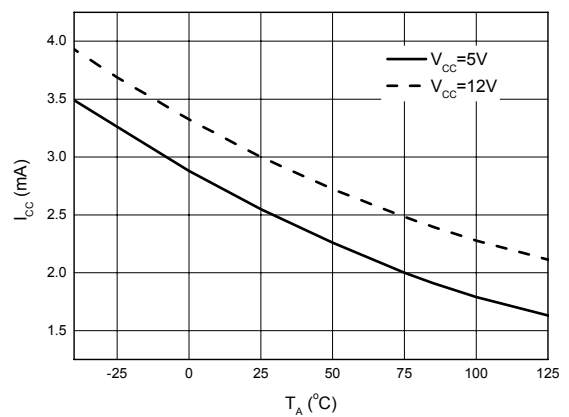


Figure 12. I<sub>CC</sub> vs. T<sub>A</sub>



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**Typical Performance Characteristics (Continued)**

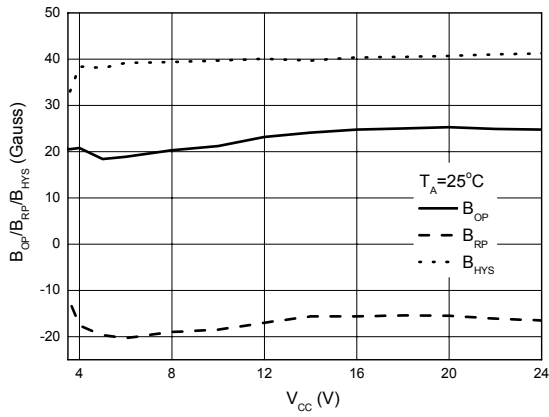


Figure 13. B<sub>OP</sub>/B<sub>RP</sub>/B<sub>HYS</sub> vs. V<sub>CC</sub>

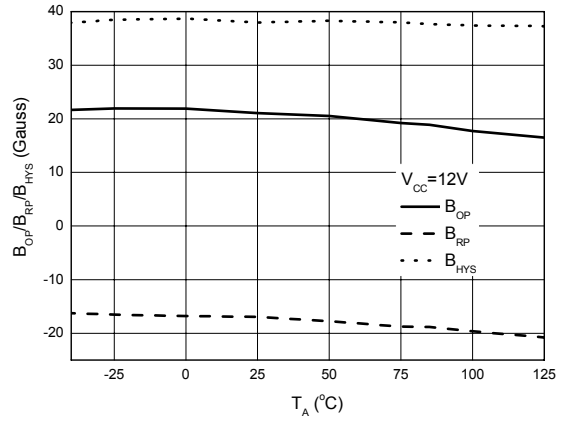


Figure 14. B<sub>OP</sub>/B<sub>RP</sub>/B<sub>HYS</sub> vs. T<sub>A</sub>

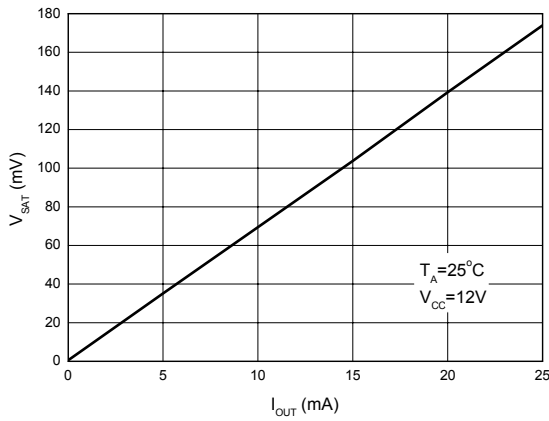


Figure 15. V<sub>SAT</sub> vs. I<sub>OUT</sub>

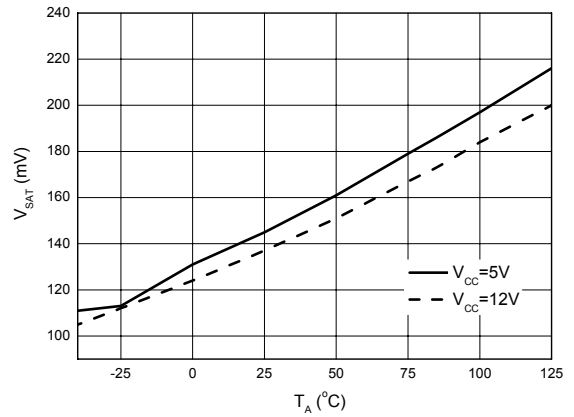


Figure 16. V<sub>SAT</sub> vs. T<sub>A</sub>

**HIGH SENSITIVITY CMOS HALL-EFFECT LATCH**

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**Typical Performance Characteristics (Continued)**

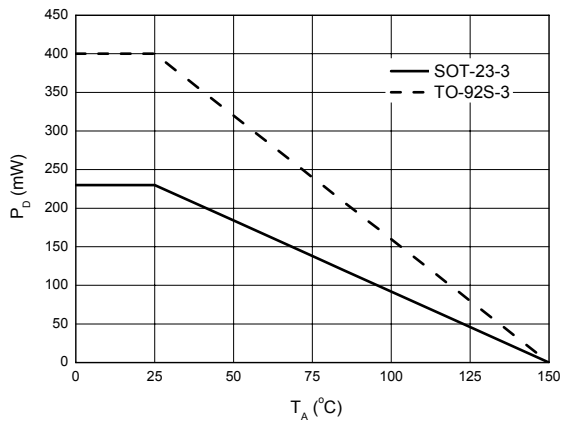


Figure 17. P<sub>D</sub> vs. T<sub>A</sub>

**Typical Application**

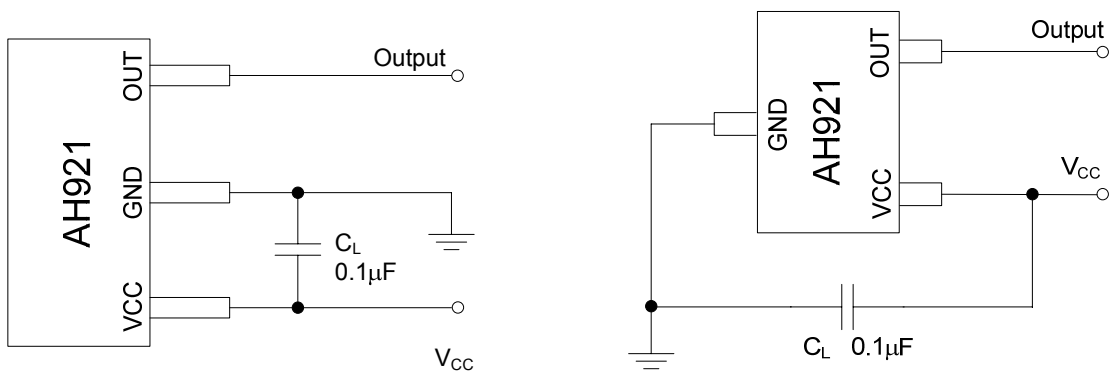


Figure 18. Typical Application Circuit of AH921

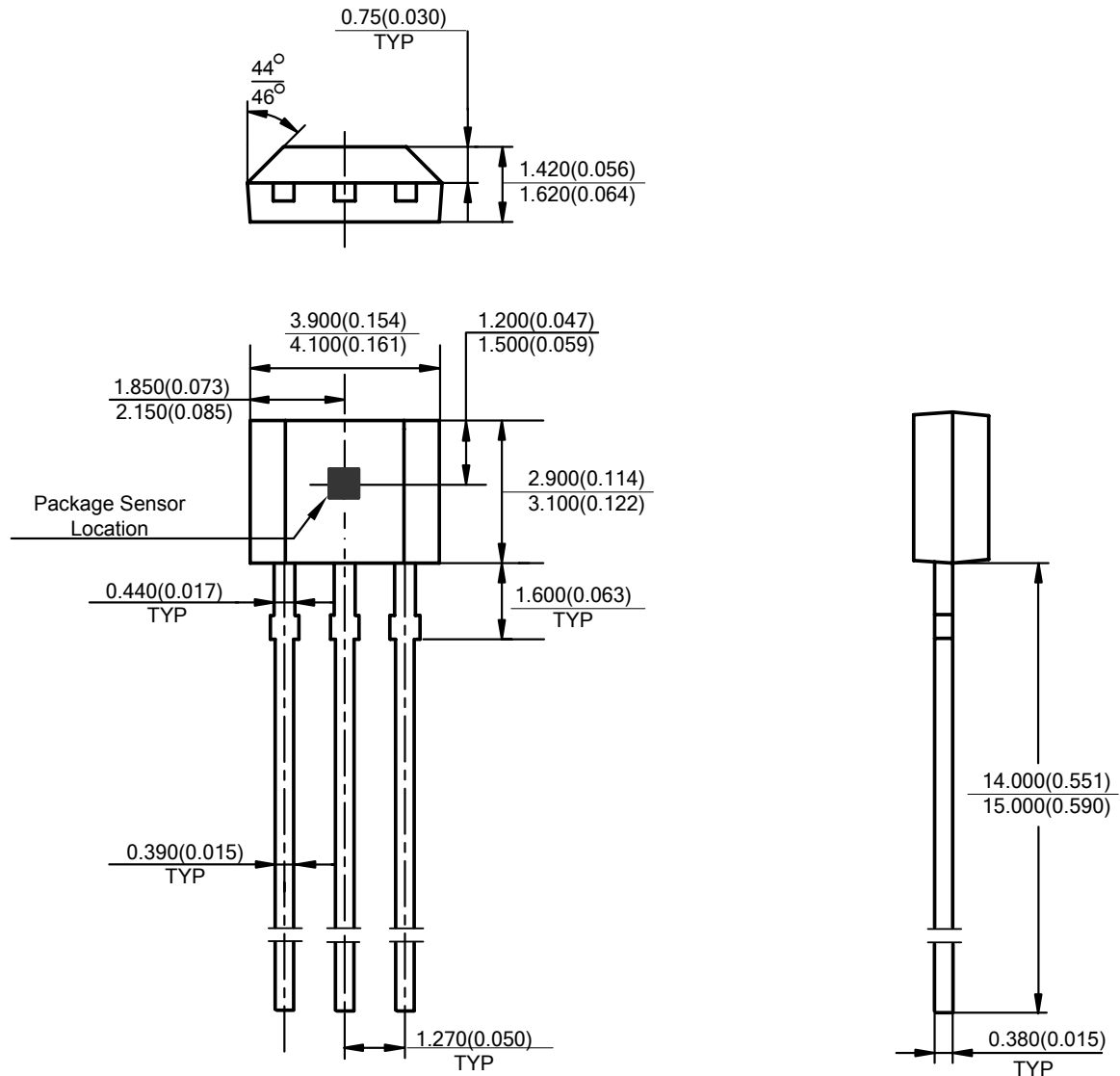
**HIGH SENSITIVITY CMOS HALL-EFFECT LATCH**

**AH921**

**Mechanical Dimensions**

**TO-92S-3**

**Unit: mm(inch)**



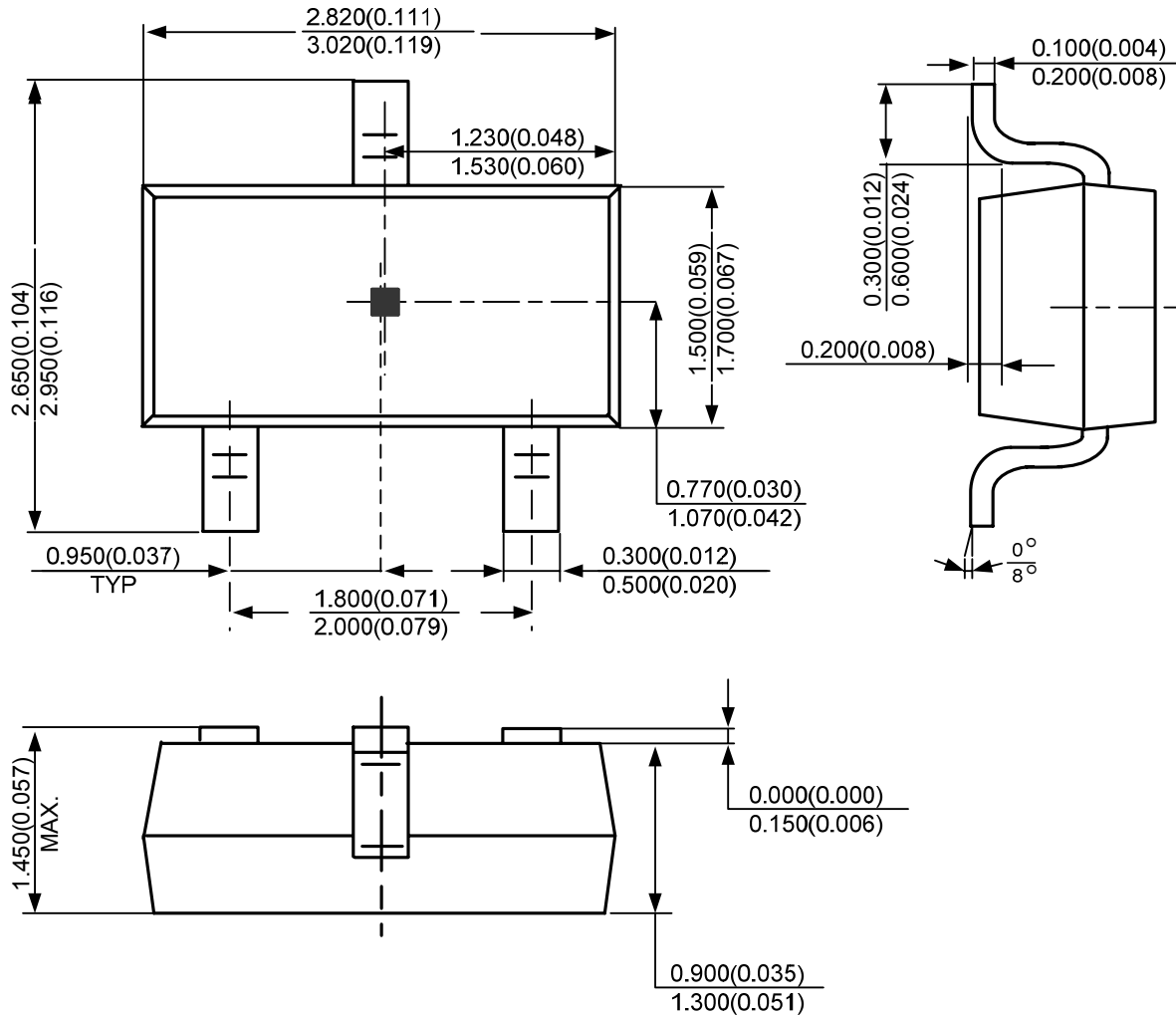
**HIGH SENSITIVITY CMOS HALL-EFFECT LATCH**

**AH921**

**Mechanical Dimensions (Continued)**

**SOT-23-3**

**Unit: mm(inch)**





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