

# 74LV132

## Quad 2-input NAND Schmitt trigger

Rev. 05 — 2 July 2009

Product data sheet

### 1. General description

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The 74LV132 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC132 and 74HCT132.

The 74LV132 contains four 2-input NAND gates which accept standard input signals. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

The gate switches at different points for positive and negative-going signals. The difference between the positive voltage  $V_{T+}$  and the negative voltage  $V_{T-}$  is defined as the input hysteresis voltage  $V_H$ .

### 2. Features

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- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Typical output ground bounce < 0.8 V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- Typical HIGH-level output voltage ( $V_{OH}$ ) undershoot: > 2 V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

### 3. Applications

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- Wave and pulse shapers for highly noisy environments
- Astable multivibrators
- Monostable multivibrators

### 4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV132N	-40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74LV132D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV132DB	-40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LV132PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LV132BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

### 5. Functional diagram

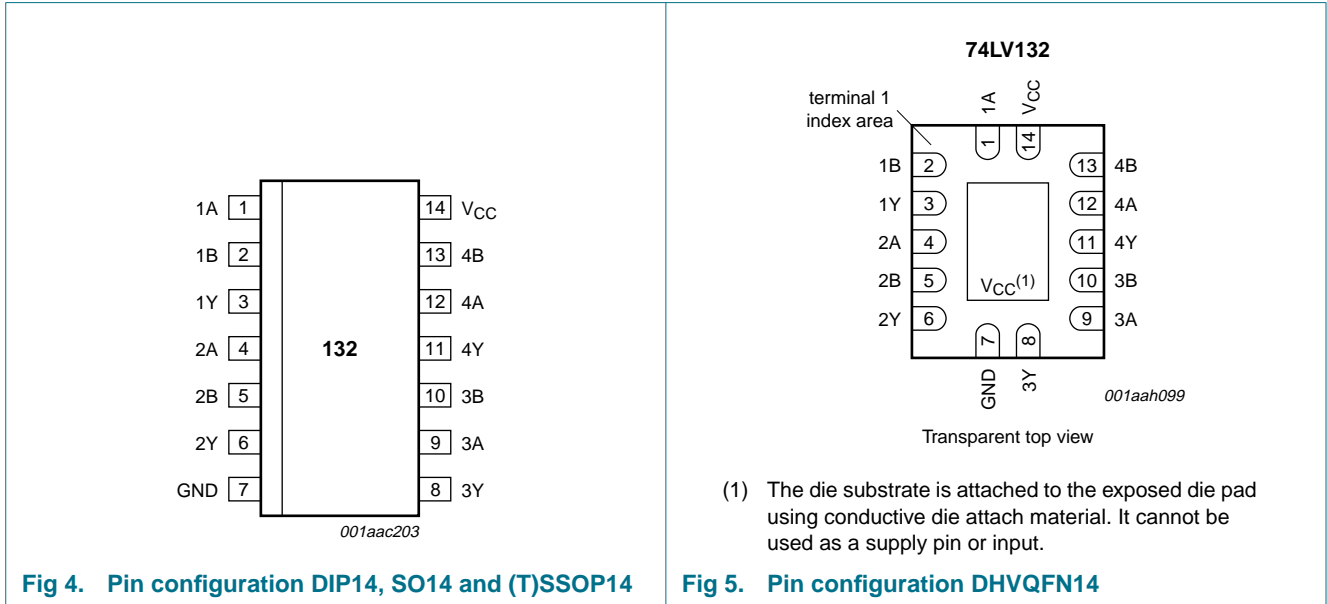
**Fig 1. Logic symbol**

**Fig 2. IEC logic symbol**

**Fig 3. Logic diagram (one gate)**

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A	1	data input
1B	2	data input
1Y	3	data output
2A	4	data input
2B	5	data input
2Y	6	data output
GND	7	ground (0 V)
3Y	8	data output
3A	9	data input
3B	10	data input
4Y	11	data output
4A	12	data input
4B	13	data input
V <sub>CC</sub>	14	supply voltage

## 7. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level.*

Input		Output
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

## 8. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	[1] -	±20	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	[1] -	±50	mA
$I_O$	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	±25	mA
$I_{CC}$	supply current		-	50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$			
	DIP14 package		[2] -	750	mW
	SO14 package		[3] -	500	mW
	(T)SSOP14 package		[4] -	500	mW
	DHVQFN14 package		[5] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2]  $P_{tot}$  derates linearly with 12 mW/K above 70 °C.

[3]  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

[4]  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.

[5]  $P_{tot}$  derates linearly with 4.5 mW/K above 60 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage <sup>[1]</sup>		1.0	3.3	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C

[1] The static characteristics are guaranteed from  $V_{CC} = 1.2$  V to  $V_{CC} = 5.5$  V, but LV devices are guaranteed to function down to  $V_{CC} = 1.0$  V (with input levels GND or  $V_{CC}$ ).

## 10. Static characteristics

**Table 6. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
$V_{OH}$	HIGH-level output voltage	$V_I = V_{T+}$ or $V_{T-}$						
		$I_O = -100 \mu\text{A}; V_{CC} = 1.2$ V	-	1.2	-	-	-	V
		$I_O = -100 \mu\text{A}; V_{CC} = 2.0$ V	1.8	2.0	-	1.8	-	V
		$I_O = -100 \mu\text{A}; V_{CC} = 2.7$ V	2.5	2.7	-	2.5	-	V
		$I_O = -100 \mu\text{A}; V_{CC} = 3.0$ V	2.8	3.0	-	2.8	-	V
		$I_O = -100 \mu\text{A}; V_{CC} = 4.5$ V	4.3	4.5	-	4.3	-	V
		$I_O = -6$ mA; $V_{CC} = 3.0$ V	2.4	2.82	-	2.2	-	V
		$I_O = -12$ mA; $V_{CC} = 4.5$ V	3.6	4.2	-	3.5	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{T+}$ or $V_{T-}$						
		$I_O = 100 \mu\text{A}; V_{CC} = 1.2$ V	-	0	-	-	-	V
		$I_O = 100 \mu\text{A}; V_{CC} = 2.0$ V	-	0	0.2	-	0.2	V
		$I_O = 100 \mu\text{A}; V_{CC} = 2.7$ V	-	0	0.2	-	0.2	V
		$I_O = 100 \mu\text{A}; V_{CC} = 3.0$ V	-	0	0.2	-	0.2	V
		$I_O = 100 \mu\text{A}; V_{CC} = 4.5$ V	-	0	0.2	-	0.2	V
		$I_O = 6$ mA; $V_{CC} = 3.0$ V	-	0.25	0.40	-	0.50	V
		$I_O = 12$ mA; $V_{CC} = 4.5$ V	-	0.35	0.55	-	0.65	V
$I_I$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	1.0	-	1.0	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	20.0	-	40	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input; $V_I = V_{CC} - 0.6$ V; $V_{CC} = 2.7$ V to 3.6 V	-	-	500	-	850	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	-	-	pF

[1] Typical values are measured at  $T_{amb} = 25$  °C.

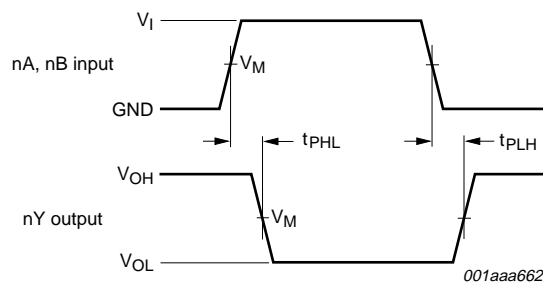
## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**  
*GND = 0 V; For test circuit see Figure 7.*

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nA, nB to nY; see Figure 6 <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	65	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	18	34	-	43	ns
		V <sub>CC</sub> = 2.7 V	-	15	24	-	30	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 15 pF <sup>[3]</sup>	-	10	-	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	-	12	20	-	25	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[3]</sup>	-	9.0	14	-	17	ns
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f <sub>i</sub> = 1 MHz; V <sub>i</sub> = GND to V <sub>CC</sub> <sup>[4]</sup>	-	24	-	-	-	pF

- [1] All typical values are measured at T<sub>amb</sub> = 25 °C.
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.
- [3] Typical values are measured at nominal supply voltage (V<sub>CC</sub> = 3.3 V and V<sub>CC</sub> = 5.0 V).
- [4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz, f<sub>o</sub> = output frequency in MHz  
 C<sub>L</sub> = output load capacitance in pF  
 V<sub>CC</sub> = supply voltage in V  
 N = number of inputs switching  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

## 12. Waveforms



Measurement points are given in Table 8.

V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

**Fig 6. The input (nA, nB) to output (nY) propagation delays**

Table 8. Measurement points

Supply voltage $V_{CC}$	Input $V_M$	Output $V_M$
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V
$\geq 4.5$ V	$0.5V_{CC}$	$0.5V_{CC}$

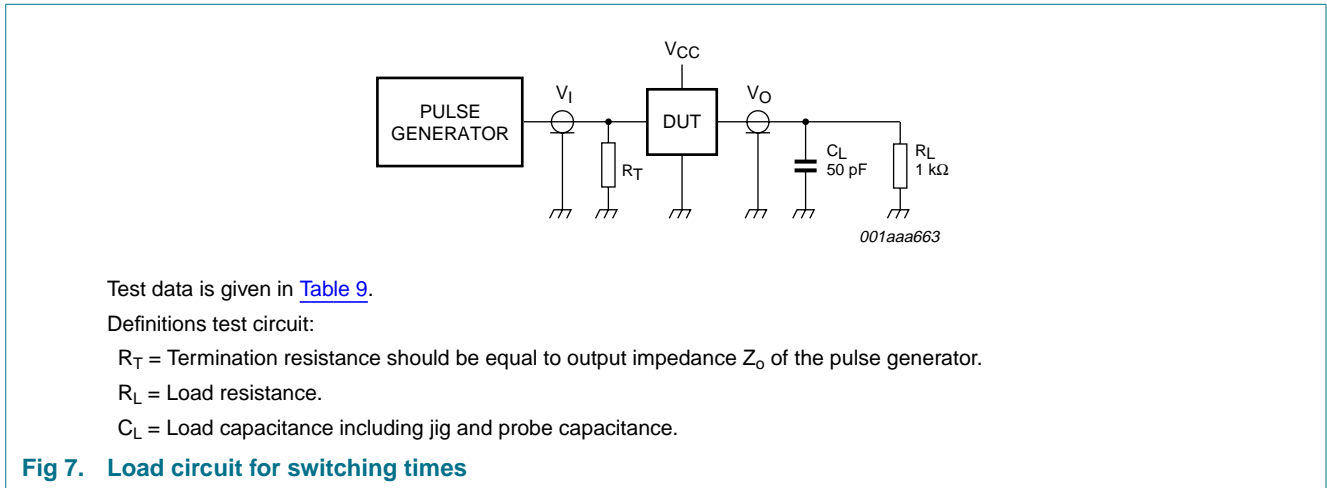


Table 9. Test data

Supply voltage $V_{CC}$	Input $V_I$	$t_r, t_f$
< 2.7 V	$V_{CC}$	$\leq 2.5$ ns
2.7 V to 3.6 V	2.7 V	$\leq 2.5$ ns
$\geq 4.5$ V	$V_{CC}$	$\leq 2.5$ ns

### 13. Transfer characteristics

Table 10. Transfer characteristics

$GND = 0$  V; For test circuit see [Figure 7](#).

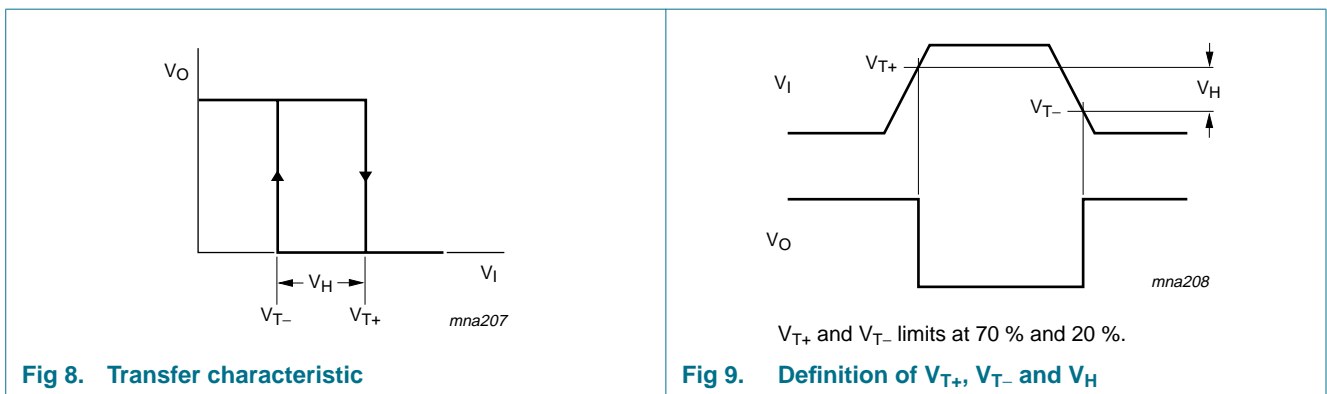
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
$V_{T+}$	positive-going threshold voltage	see <a href="#">Figure 6</a>						
		$V_{CC} = 1.2$ V	-	0.70	-	-	-	V
		$V_{CC} = 2.0$ V	0.8	1.10	1.4	0.8	1.4	V
		$V_{CC} = 2.7$ V	1.0	1.45	2.0	1.0	2.0	V
		$V_{CC} = 3.0$ V	1.2	1.60	2.2	1.2	2.2	V
		$V_{CC} = 3.6$ V	1.5	1.95	2.4	1.5	2.4	V
		$V_{CC} = 4.5$ V	1.7	2.50	3.2	1.7	3.2	V
$V_{CC} = 5.5$ V	2.1	3.00	3.9	2.1	3.9	V		

**Table 10. Transfer characteristics ...continued**  
*GND = 0 V; For test circuit see Figure 7.*

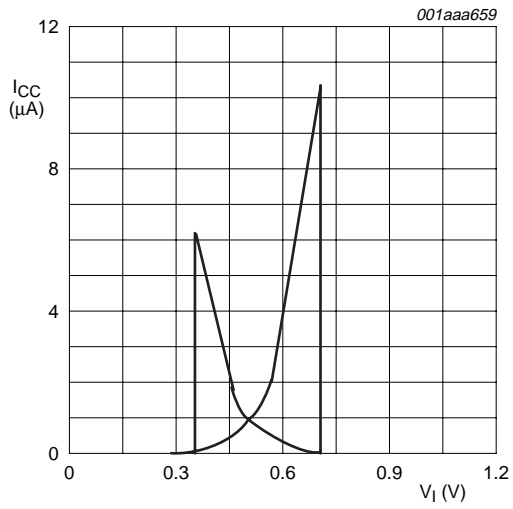
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
V <sub>T-</sub>	negative-going threshold voltage	see <a href="#">Figure 6</a>						
		V <sub>CC</sub> = 1.2 V	-	0.34	-	-	-	V
		V <sub>CC</sub> = 2.0 V	0.3	0.65	0.9	0.3	0.9	V
		V <sub>CC</sub> = 2.7 V	0.4	0.90	1.4	0.4	1.4	V
		V <sub>CC</sub> = 3.0 V	0.6	1.05	1.5	0.6	1.5	V
		V <sub>CC</sub> = 3.6 V	0.8	1.30	1.8	0.8	1.8	V
		V <sub>CC</sub> = 4.5 V	0.9	1.60	2.0	0.9	2.0	V
V <sub>H</sub>	hysteresis voltage (V <sub>T+</sub> - V <sub>T-</sub> ); see <a href="#">Figure 6</a>	V <sub>CC</sub> = 1.2 V	-	0.3	-	-	-	V
		V <sub>CC</sub> = 2.0 V	0.2	0.55	0.8	0.2	0.8	V
		V <sub>CC</sub> = 2.7 V	0.3	0.60	1.1	0.3	1.1	V
		V <sub>CC</sub> = 3.0 V	0.4	0.65	1.2	0.4	1.2	V
		V <sub>CC</sub> = 3.6 V	0.4	0.70	1.2	0.4	1.2	V
		V <sub>CC</sub> = 4.5 V	0.4	0.80	1.4	0.4	1.4	V
		V <sub>CC</sub> = 5.5 V	0.6	1.00	1.5	0.6	1.5	V

[1] All typical values are measured at T<sub>amb</sub> = 25 °C.

### 14. Waveforms transfer characteristics

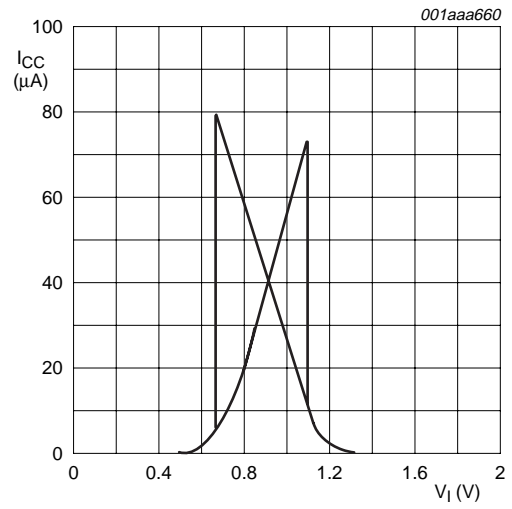






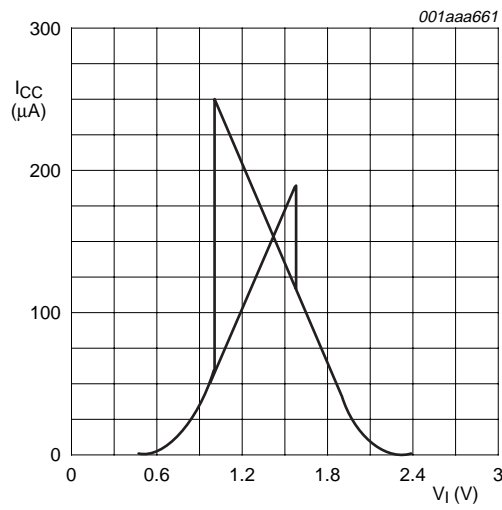
$V_{CC} = 1.2$  V.

Fig 10. Typical 74LV132 transfer characteristics



$V_{CC} = 2.0$  V.

Fig 11. Typical 74LV132 transfer characteristics



$V_{CC} = 3.0$  V.

Fig 12. Typical 74LV132 transfer characteristics

15. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

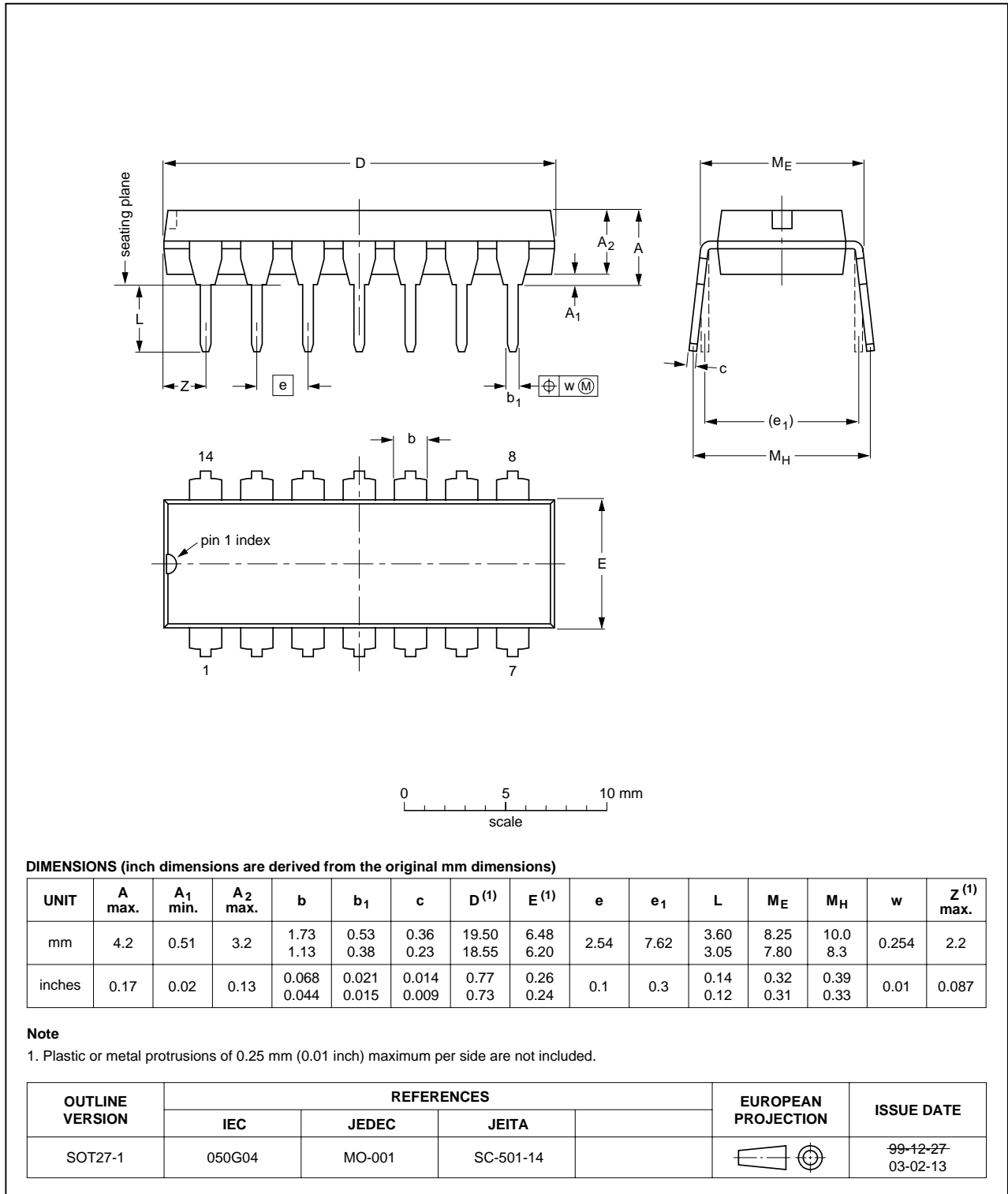


Fig 13. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

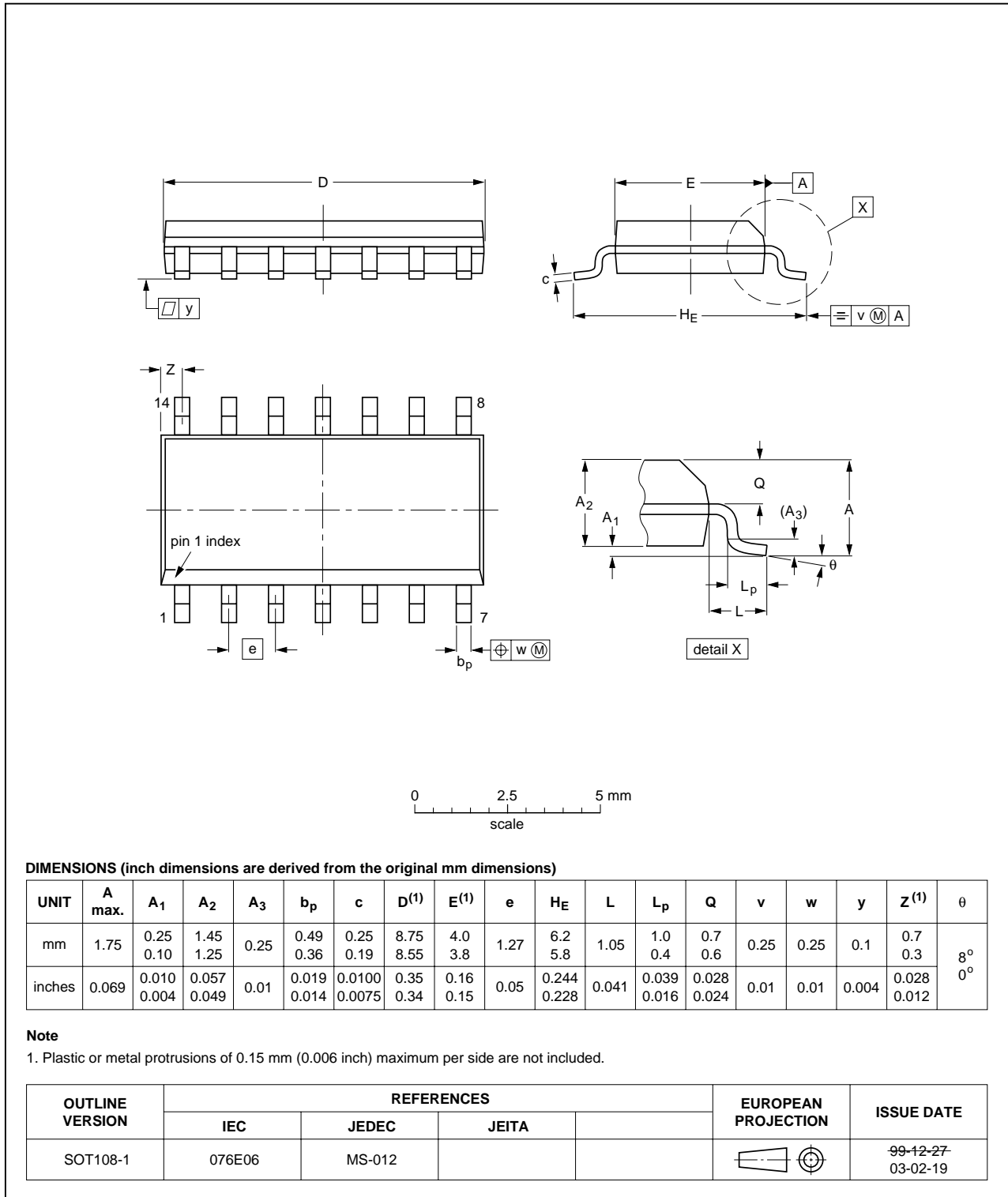


Fig 14. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

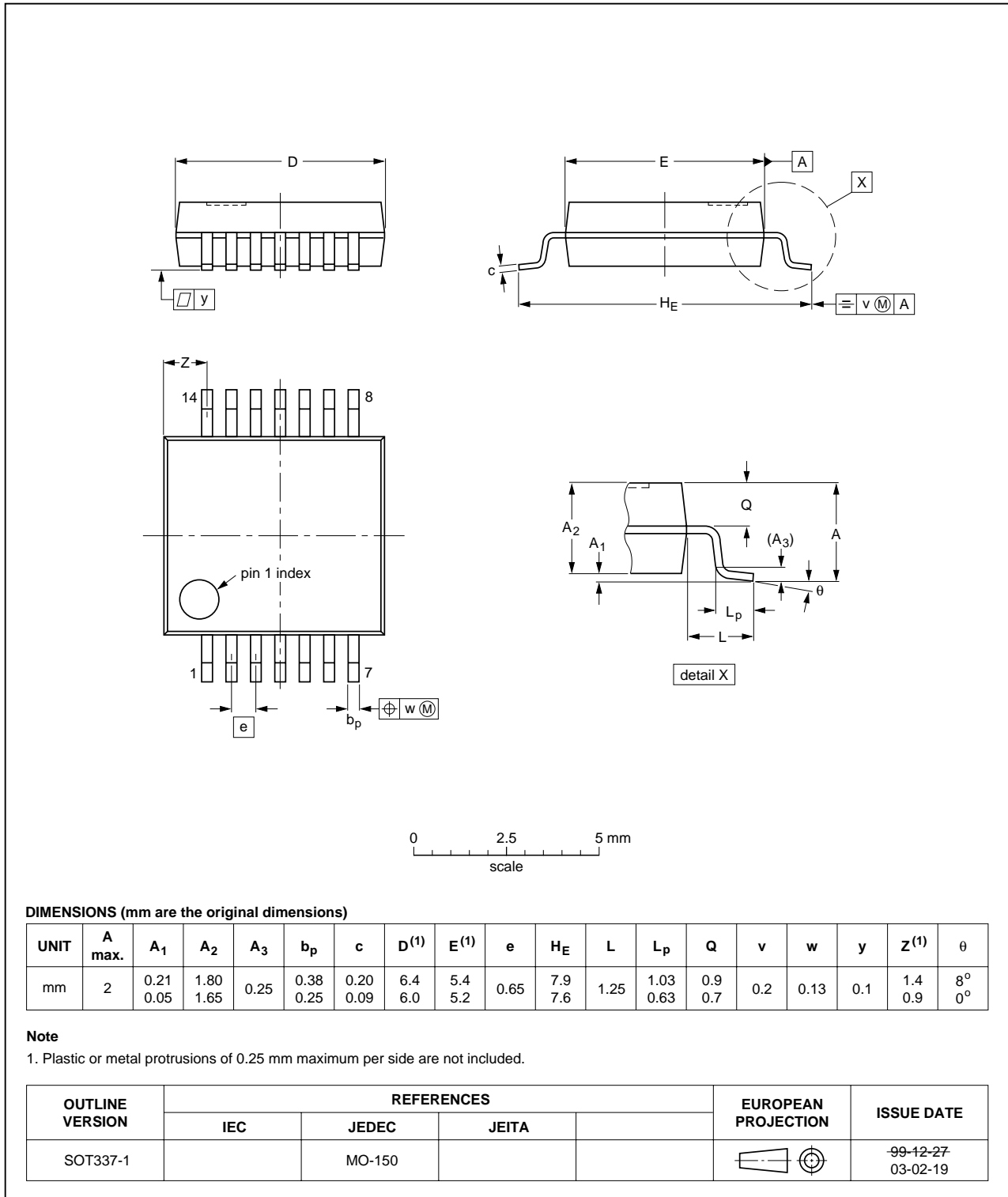


Fig 15. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

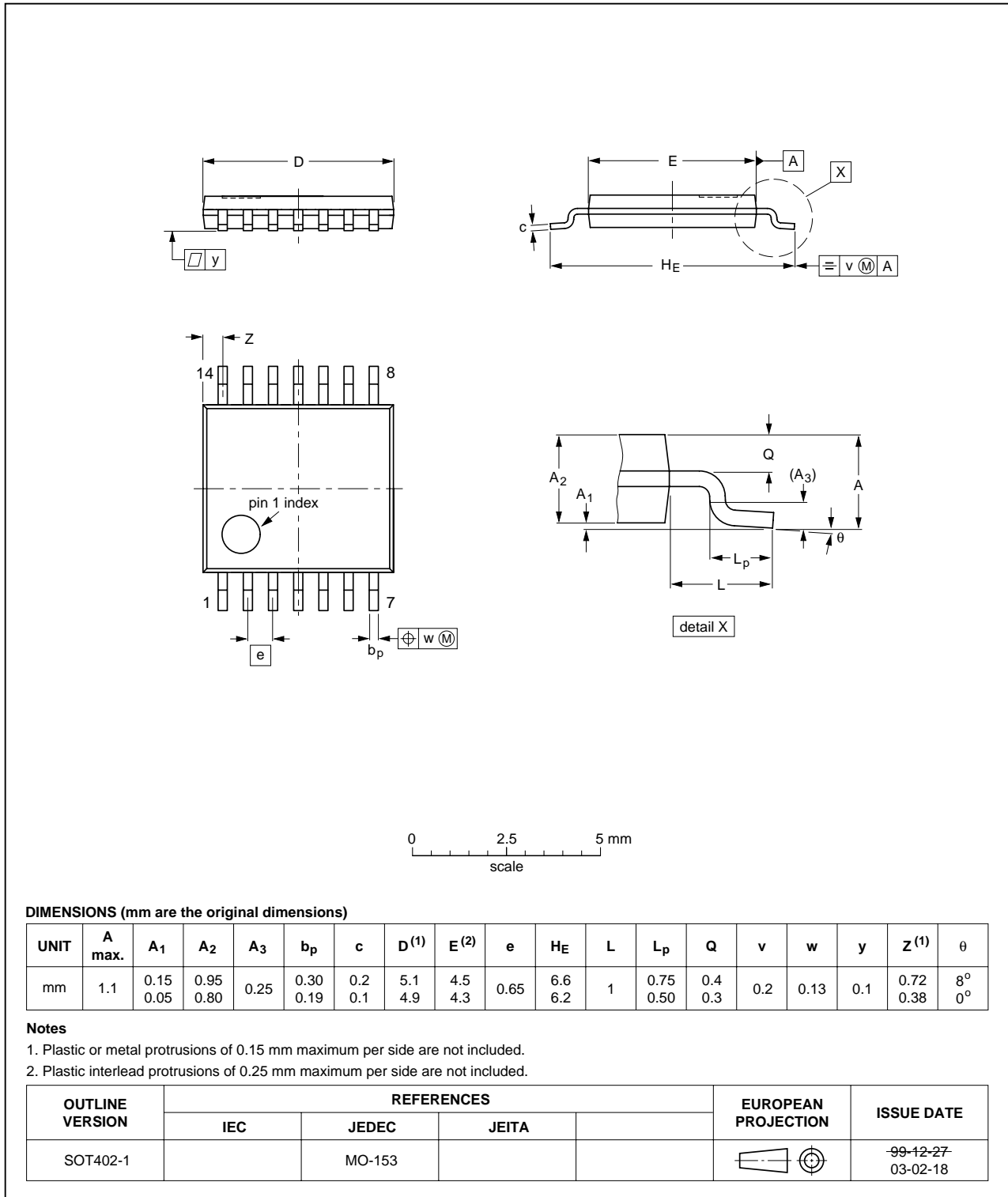


Fig 16. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

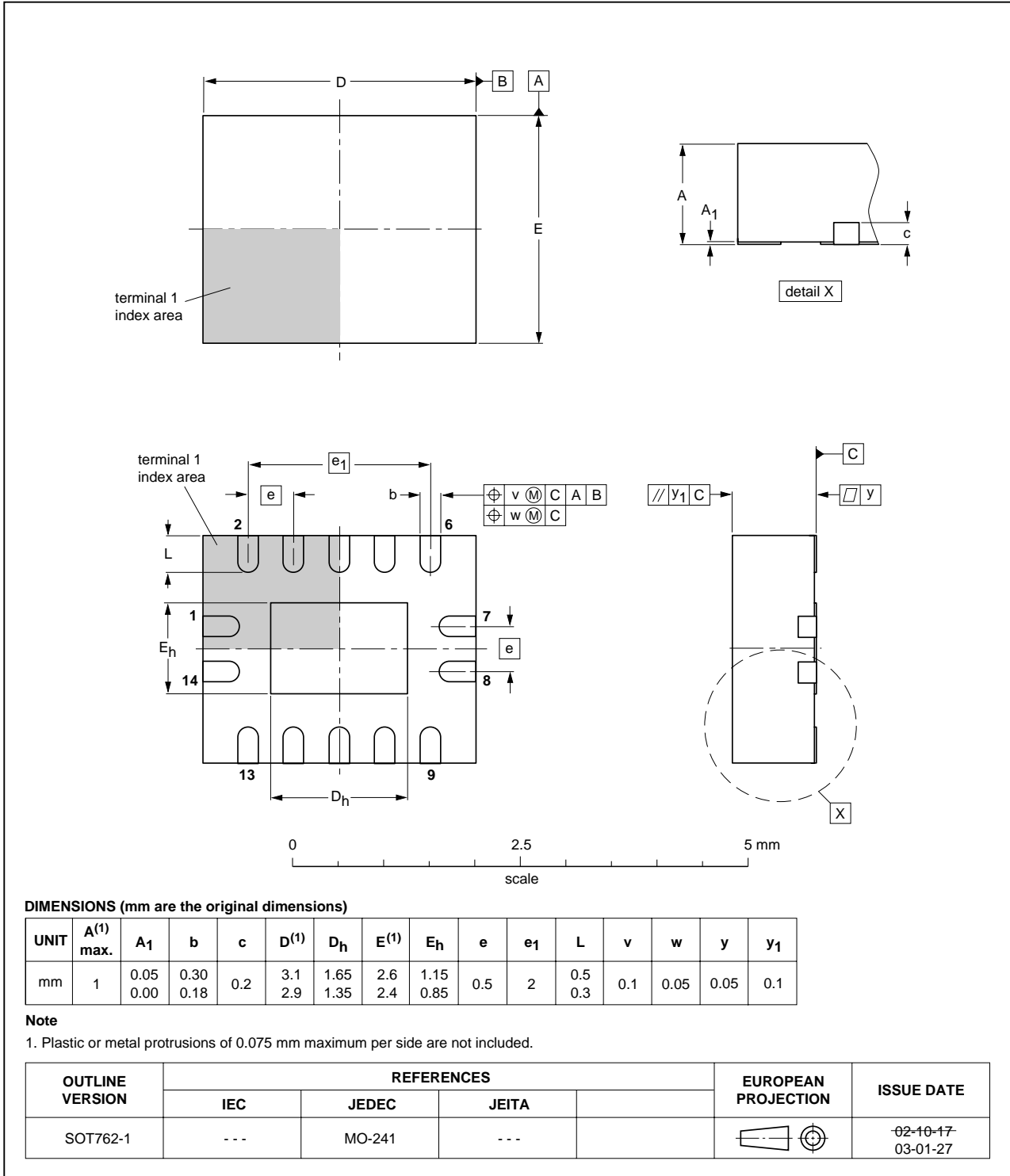


Fig 17. Package outline SOT762-1 (DHVQFN14)

## 16. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 17. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV132_5	20090702	Product data sheet	-	74LV132_4
Modifications:	<ul style="list-style-type: none"><li>• <a href="#">Table 6</a>: the conditions for HIGH-level output voltage and LOW-level output voltage have been changed.</li></ul>			
74LV132_4	20071112	Product data sheet	-	74LV132_3
74LV132_3	20040415	Product specification	-	74LV132_2
74LV132_2	19980428	Product specification	-	74LV132_1
74LV132_1	19970204	Product specification	-	-

## 18. Legal information

### 18.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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