

STT3585

3.5A, 20V, $R_{DS(ON)}$ 75m Ω
 -2.5A, -20V, $R_{DS(ON)}$ 160m Ω

N And P-Channel Enhancement Mode Power MOSFET

RoHS Compliant Product
 A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

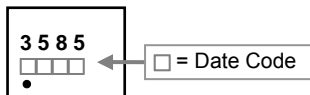
The STT3585 provide the designer with best combination of fast switching, low on-resistance and cost effectiveness.

The TSOP-6 package is universally used for all commercial-industrial surface mount applications.

FEATURES

- Low Gate Charge
- Low On-resistance

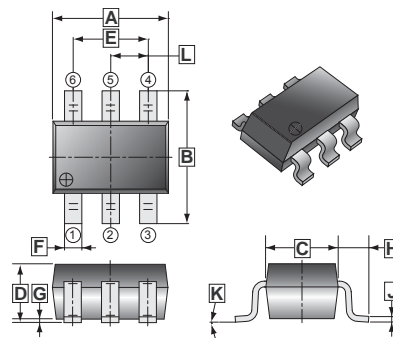
MARKING CODE



PACKAGE INFORMATION

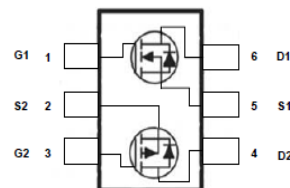
Package	MPQ	Leader Size
TSOP-6	3K	7 inch

TSOP-6



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	0	0.10
B	2.60	3.00	H	0.60	REF.
C	1.40	1.80	J	0.12	REF.
D	1.10	MAX.	K	0°	10°
E	1.90	REF.	L	0.95	REF.
F	0.30	0.50			

TOP VIEW



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings		Unit	
		N-Channel	P-Channel		
Drain-Source Voltage	V_{DS}	20	-20	V	
Gate-Source Voltage	V_{GS}	± 12	± 12	V	
Continuous Drain Current ³	I_D	$T_A = 25^\circ\text{C}$	3.5	-2.5	A
		$T_A = 70^\circ\text{C}$	2.8	-1.97	
Pulsed Drain Current ¹	I_{DM}	10	-10	A	
Power Dissipation	P_D	1.14		W	
Maximum Junction to Ambient ³	$R_{\theta JA}$	110		$^\circ\text{C} / \text{W}$	
Linear Derating Factor		0.01		$\text{W} / ^\circ\text{C}$	
Operating Junction & Storage Temperature Range	T_J, T_{STG}	-55~150		$^\circ\text{C}$	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions		
Static								
Drain-Source Breakdown Voltage	N-Ch	BV_{DSS}	20	-	-	V	$V_{GS}=0, I_D=250\mu\text{A}$	
	P-Ch		-20	-	-		$V_{GS}=0, I_D= -250\mu\text{A}$	
Breakdown Voltage Temp. Coefficient	N-Ch	$\Delta BV_{DSS}/\Delta T_J$	-	0.02	-	V/ $^\circ\text{C}$	Reference to 25°C , $I_D=1\text{mA}$	
	P-Ch		-	-0.01	-		Reference to 25°C , $I_D= -1\text{mA}$	
Gate-Threshold Voltage	N-Ch	$V_{GS(th)}$	0.5	-	1.2	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	
	P-Ch		-	-	-1.2		$V_{DS}=V_{GS}, I_D= -250\mu\text{A}$	
Forward Transconductance	N-Ch	g_{fs}	-	7	-	S	$V_{DS}=5\text{V}, I_D=3\text{A}$	
	P-Ch		-	4	-		$V_{DS}= -5\text{V}, I_D= -2\text{A}$	
Gate-Source Leakage Current	N-Ch	I_{GSS}	-	-	± 100	nA	$V_{GS}= \pm 12\text{V}$	
	P-Ch		-	-	± 100		$V_{GS}= \pm 12\text{V}$	
Drain-Source Leakage Current	N-Ch	I_{DSS}	-	-	1	μA	$V_{DS}=20\text{V}, V_{GS}=0$	
	P-Ch		-	-	-1		$V_{DS}= -20\text{V}, V_{GS}=0$	
	N-Ch		-	-	10		$V_{DS}=16\text{V}, V_{GS}=0$	
	P-Ch		-	-	-25		$V_{DS}= -16\text{V}, V_{GS}=0$	
Drain-Source On-Resistance ¹	N-Ch	$R_{DS(ON)}$	-	-	75	m Ω	$V_{GS}=4.5\text{V}, I_D=3.5\text{A}$	
	P-Ch		-	-	160		$V_{GS}= -4.5\text{V}, I_D= -2.5\text{A}$	
	N-Ch		-	-	125		$V_{GS}=2.5\text{V}, I_D=1.2\text{A}$	
	P-Ch		-	-	300		$V_{GS}= -2.5\text{V}, I_D= -2\text{A}$	
Total Gate Charge ¹	N-Ch	Q_g	-	4	7	nC	N-Channel $V_{DS}=16\text{V}, V_{GS}=4.5\text{V}, I_D=3\text{A}$	
	P-Ch		-	5	8			
Gate-Source Charge	N-Ch	Q_{gs}	-	0.7	-		P-Channel $V_{DS}= -16\text{V}, V_{GS}= -4.5\text{V}, I_D= -2\text{A}$	
	P-Ch		-	1	-			
Gate-Drain Charge	N-Ch	Q_{gd}	-	2	-			
	P-Ch		-	2	-			
Turn-on Delay Time ¹	N-Ch	$T_{d(on)}$	-	6	-		nS	N-Channel $V_{DS}=15\text{V}, R_G=3.3\Omega, R_D=15\Omega$ $V_{GS}=5\text{V}, I_D=1\text{A}$
	P-Ch		-	6	-			
Rise Time	N-Ch	T_r	-	8	-			P-Channel $V_{DS}= -10\text{V}, R_G=3.3\Omega, R_D=10\Omega$ $V_{GS}= -10\text{V}, I_D= -1\text{A}$
	P-Ch		-	17	-			
Turn-off Delay Time	N-Ch	$T_{d(off)}$	-	10	-			
	P-Ch		-	16	-			
Fall Time	N-Ch	T_f	-	3	-			
	P-Ch		-	5	-			
Input Capacitance	N-Ch	C_{iss}	-	430	520	pF		N-Channel $V_{GS}=0, V_{DS}=20\text{V}, f=1.0\text{MHz}$
	P-Ch		-	630	750			
Output Capacitance	N-Ch	C_{oss}	-	55	-		P-Channel $V_{GS}=0, V_{DS}= -20\text{V}, f=1.0\text{MHz}$	
	P-Ch		-	50	-			
Reverse Transfer Capacitance	N-Ch	C_{rss}	-	40	-			
	P-Ch		-	40	-			
Gate Resistance	N-Ch	R_g	-	1.4	1.7	Ω	$f=1.0\text{MHz}$	
	P-Ch		-	7	10			

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Source-Drain Diode							
Forward On Voltage ¹	N-Ch	V _{SD}	-	-	1.2	V	I _S =1.2A, V _{GS} =0
	P-Ch		-	-	-1.2		I _S = -1.2A, V _{GS} =0
Reverse Recovery Time	N-Ch	T _{RR}	-	16	-	ns	I _S =3A, V _{GS} =0 ,dI/dt=100A/μs
	P-Ch		-	20	-		I _S = -2A, V _{GS} =0 ,dI/dt=100A/μs
Reverse Recovery Charge	N-Ch	Q _{rr}	-	8	-	nC	I _S =3A, V _{GS} =0 ,dI/dt=100A/μs
	P-Ch		-	15	-		I _S = -2A, V _{GS} =0 ,dI/dt=100A/μs

Notes:

- 1 Pulse width limited by Max. junction temperature.
- 2 Pulse width ≤ 300μs, duty cycle ≤ 2%.
- 3 Surface mounted on 1 in² copper pad of FR4 board; t ≤ 5 sec. 180°C/W when mounted on min. copper pad.

CHARACTERISTICS CURVE (N-Channel)

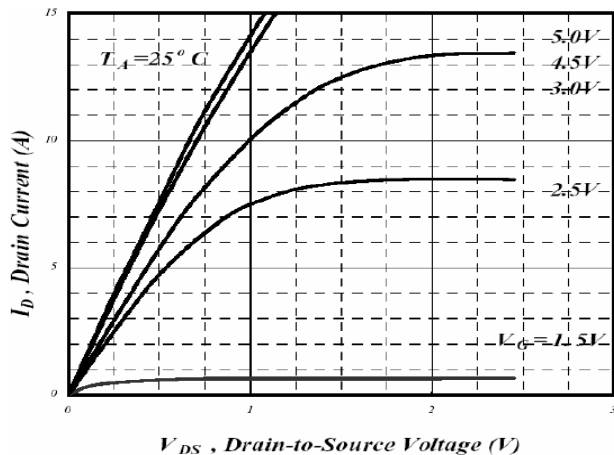


Fig 1. Typical Output Characteristics

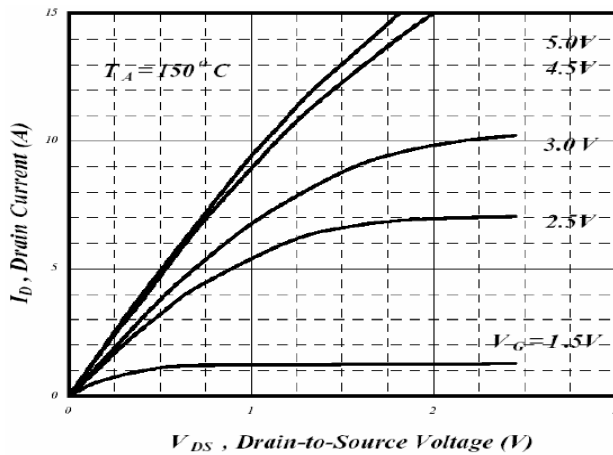


Fig 2. Typical Output Characteristics

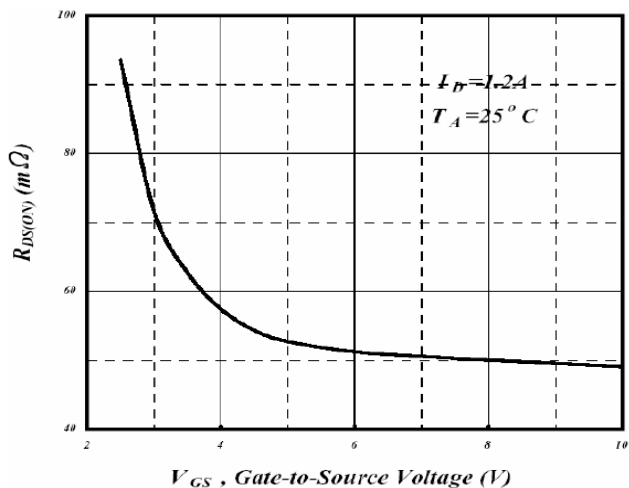


Fig 3. On-Resistance v.s. Gate Voltage

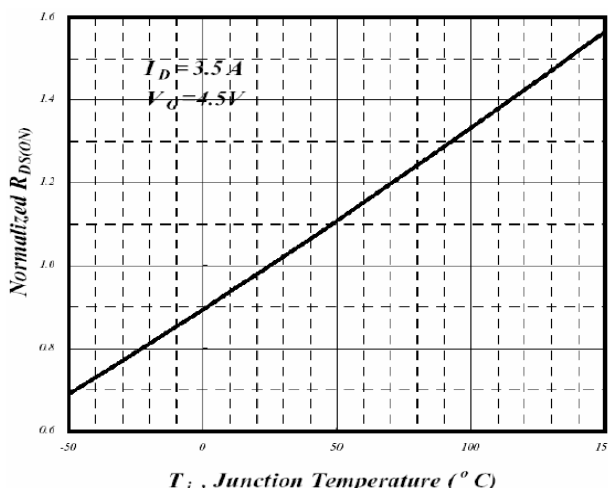


Fig 4. Normalized On-Resistance v.s. Junction Temperature

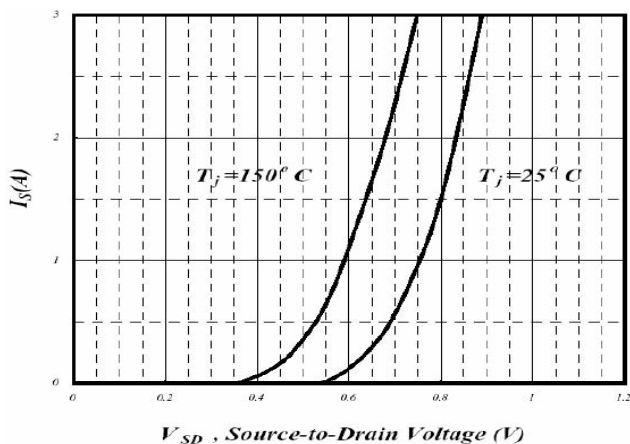


Fig 5. Forward Characteristics of Reverse Diode

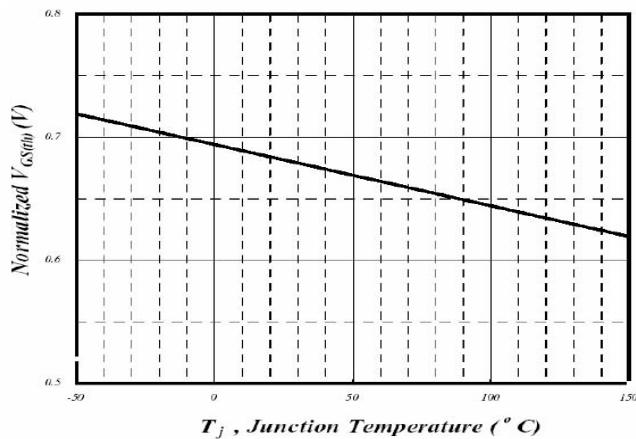


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

CHARACTERISTICS CURVE (N-Channel)

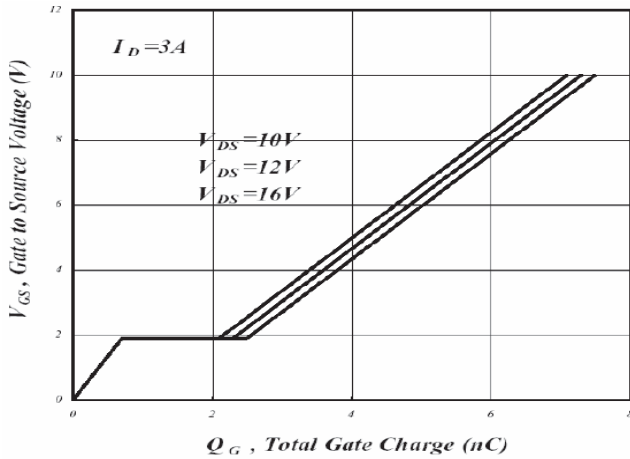


Fig 7. Gate Charge Characteristics

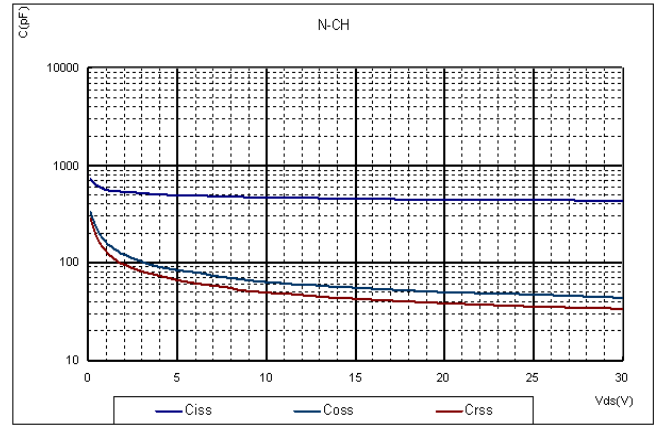


Fig 8. Typical Capacitance Characteristics

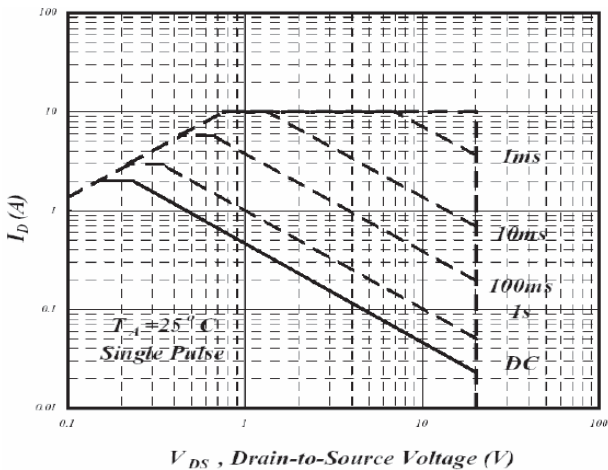


Fig 9. Maximum Safe Operating Area

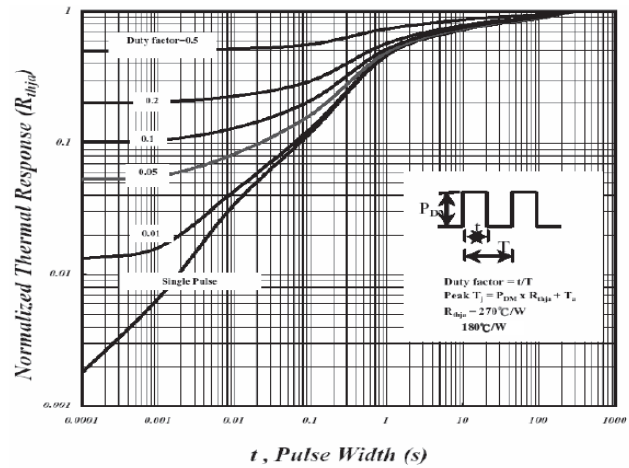


Fig 10. Effective Transient Thermal Impedance

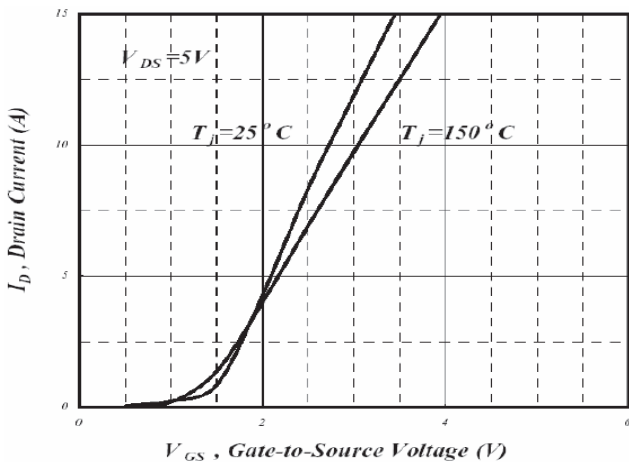


Fig 11. Transfer Characteristics

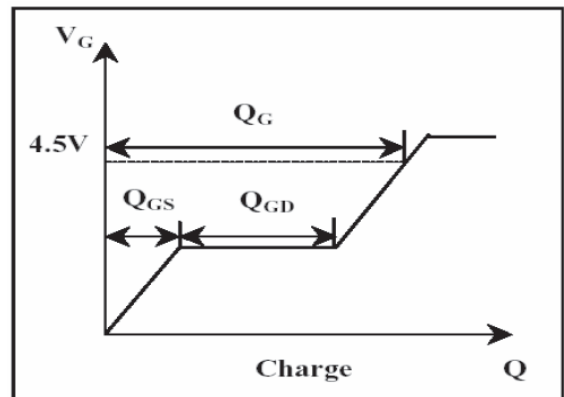


Fig 12. Gate Charge Waveform

CHARACTERISTICS CURVE (P-Channel)

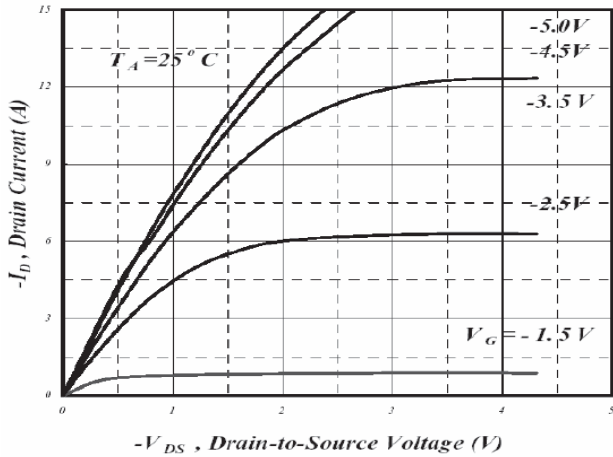


Fig 1. Typical Output Characteristics

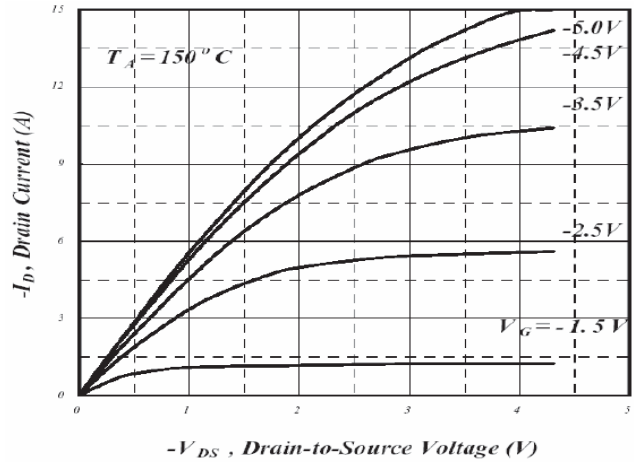


Fig 2. Typical Output Characteristics

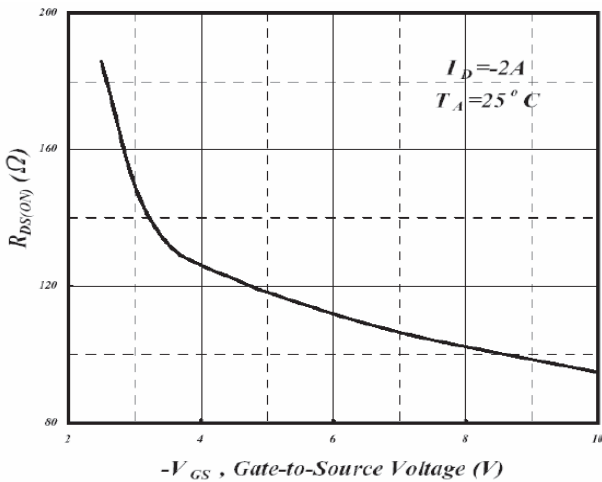


Fig 3. On-Resistance v.s. Gate Voltage

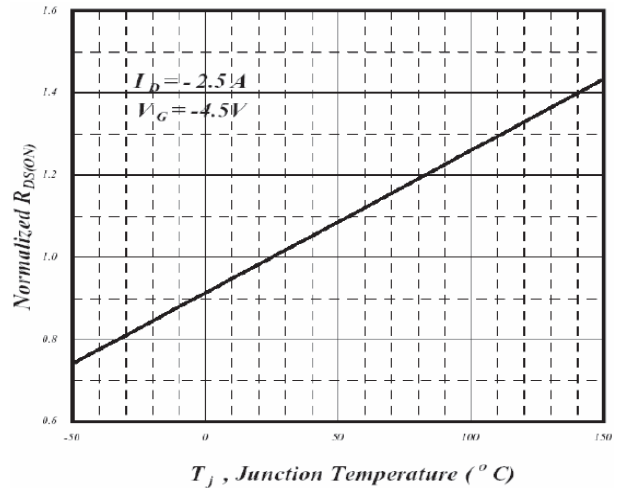


Fig 4. Normalized On-Resistance v.s. Junction Temperature

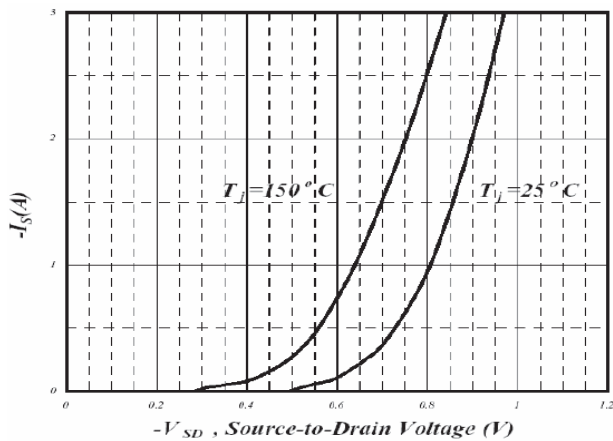


Fig 5. Forward Characteristics of Reverse Diode

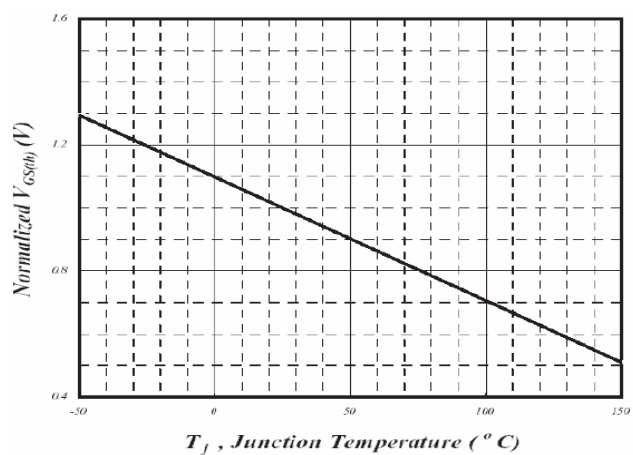


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

CHARACTERISTICS CURVE (P-Channel)

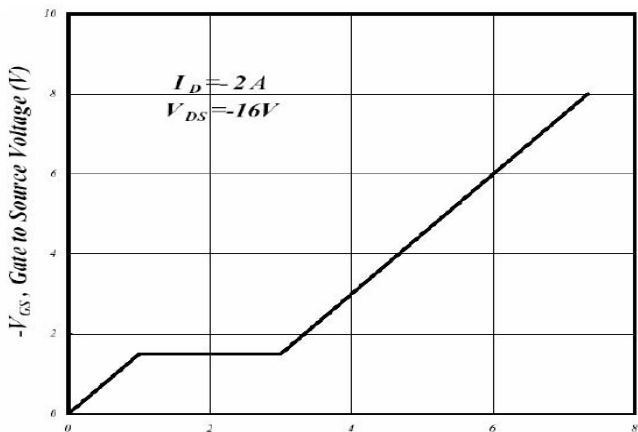


Fig 7. Gate Charge Characteristics

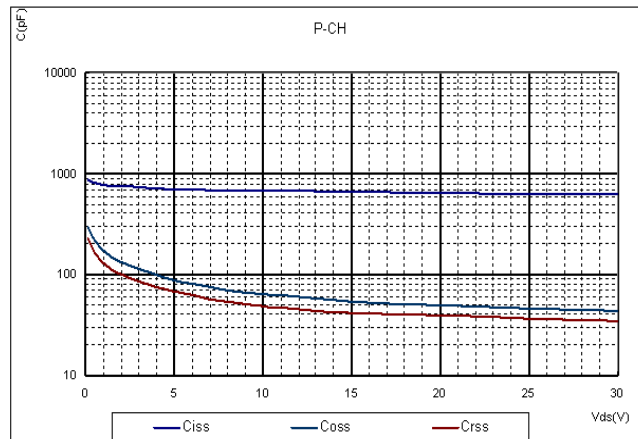


Fig 8. Typical Capacitance Characteristics

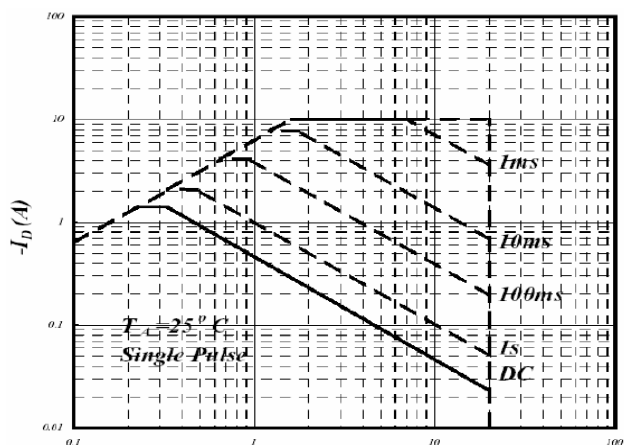


Fig 9. Maximum Safe Operating Area

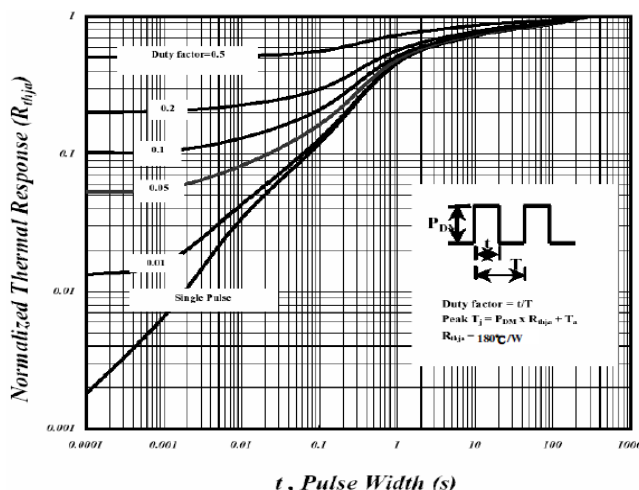


Fig 10. Effective Transient Thermal Impedance

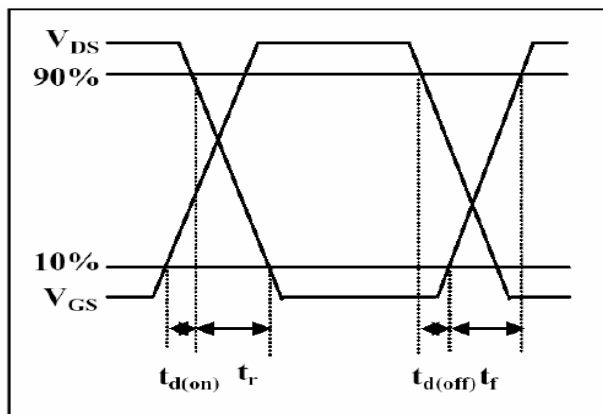


Fig 11. Switching Time Waveform

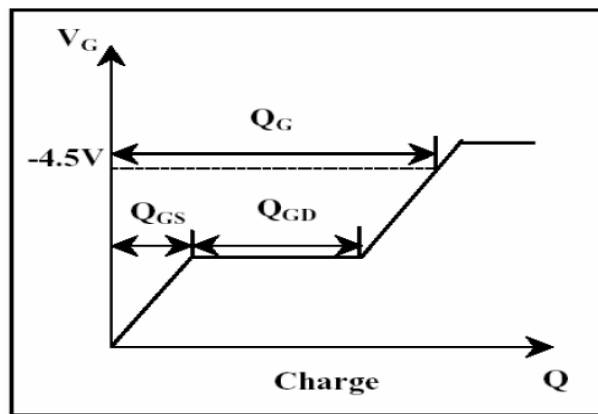


Fig 12. Gate Charge Waveform