PA97DR

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FEATURES

- HIGH VOLTAGE — 900V (±450V)
- LOW QUIESCENT CURRENT — 600µA
- HIGH OUTPUT CURRENT — 10mA

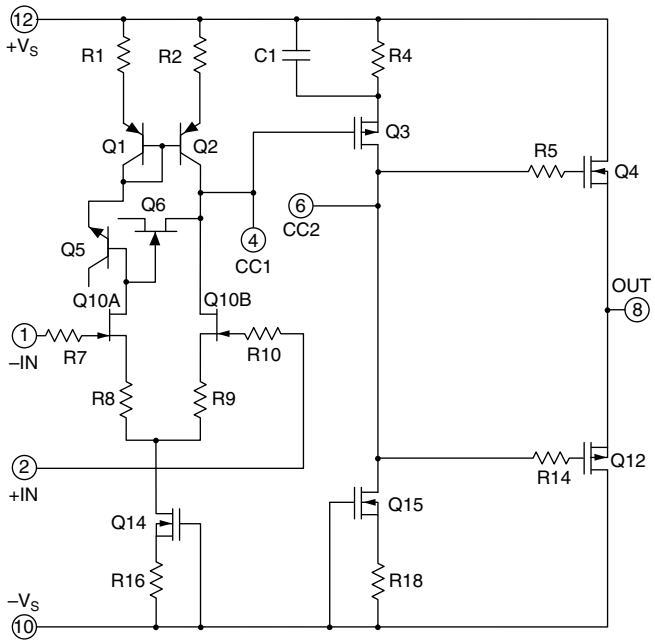
APPLICATIONS

- MASS SPECTROMETERS
- SCANNING COILS
- HIGH VOLTAGE INSTRUMENTATION
- PROGRAMMABLE POWER SUPPLIES UP TO 880V
- SEMICONDUCTOR MEASUREMENT EQUIPMENT

DESCRIPTION

The PA97DR is a high voltage MOSFET operational amplifier designed as a low cost solution for driving continuous output currents up to 10mA and pulse currents to 15mA into capacitive loads. The safe operating area (SOA) has no second breakdown limitations. The MOSFET output stage is biased class C for low quiescent current operation. External compensation provides flexibility in choosing bandwidth and slew rate for the application. APEX's SIP05 package uses a minimum of board space allowing for high density circuit boards.

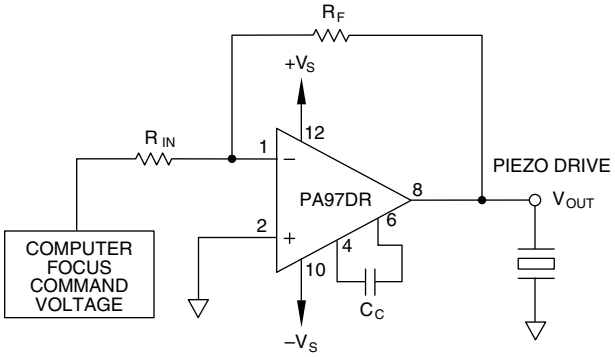
EQUIVALENT SCHEMATIC



PATENTED

7-PIN SIP
PACKAGE STYLE DR

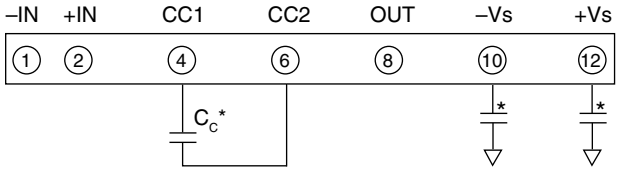
TYPICAL APPLICATION



LOW POWER, PIEZOELECTRIC POSITIONING

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA97DR reduces the costs of power supplies and cooling with its advantages of low cost and low quiescent power consumption while increasing circuit density with the SIP package.

EXTERNAL CONNECTIONS



* .01F or greater ceramic power supply bypassing required. CC = 10pF minimum, 1kV NPO (COG).

PHASE COMPENSATION

GAIN	CC
≥10	10pF

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	900V
OUTPUT CURRENT, source, sink	15mA, within SOA
POWER DISSIPATION, continuous @ T_C = 25°C	5W
INPUT VOLTAGE, differential[3]	±20V
INPUT VOLTAGE, common mode (See Text)	$\pm V_S$
TEMPERATURE, pin solder - 10s max	220°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

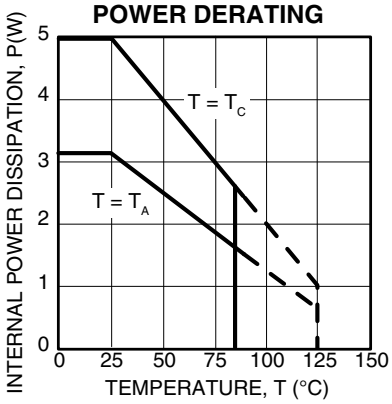
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			.5	5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	50	µV/°C
OFFSET VOLTAGE, vs. supply			10	25	µV/V
OFFSET VOLTAGE, vs. time			75		µV/kh
BIAS CURRENT, initial			200	2000	pA
BIAS CURRENT, vs. supply			4		pA/V
OFFSET CURRENT, initial			50	500	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE[3]	V_S=±250V See Note 3	$\pm V_S \mp 30$			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V	80	98		dB
NOISE	10KHz BW, R_S = 1KΩ, C_C = 10pF		2		µVrms
GAIN					
OPEN LOOP, @ 15Hz	R_L = 5KΩ, C_C = 10pF	94	111		dB
GAIN BANDWIDTH PRODUCT at 1MHz	R_L = 5KΩ, C_C = 10pF		1		MHz
POWER BANDWIDTH	R_L = 5KΩ, C_C = 10pF		2		kHz
PHASE MARGIN, A_V = 100	Full temperature range		60		°
OUTPUT					
VOLTAGE SWING[3]	I_O = 10mA	$\pm V_S \mp 24$	$\pm V_S \mp 20$		V
CURRENT, continuous		10			mA
SLEW RATE, A_V = 100	C_C = 10pF		8		V/µs
SETTLING TIME to .1%	C_C = 10pF, 2V step		2		µs
RESISTANCE	10mA Load		100		Ω
POWER SUPPLY					
VOLTAGE[5]	See note 5	±50	±300	±450	V
CURRENT, quiescent,			.6	1	mA
THERMAL					
RESISTANCE, AC, junction to case[4]	Full temperature range, F > 60Hz			20	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F < 60Hz			25	°C/W
RESISTANCE, junction to air	Full temperature range		40		°C/W
TEMPERATURE RANGE, case		–25		+85	°C

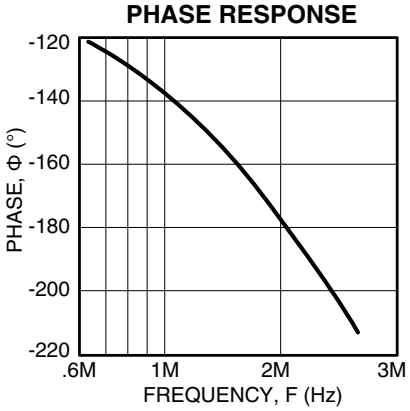
NOTES:
1. Unless otherwise noted: T_C = 25°C, DC input specifications are ± value given. Power supply voltage is typical rating. C_C = 10pF.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. Although supply voltages can range up to ± 450V the input pins cannot swing over this range. The input pins must be at least 30V from either supply rail but not more than 500V from either supply rail. See text for a more complete description of the common mode voltage range.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Derate max supply rating .625 V/°C below 25°C case. No derating needed above 25°C case.

CAUTION The PA97DR is constructed from MOSFET transistors. ESD handling procedures must be observed.

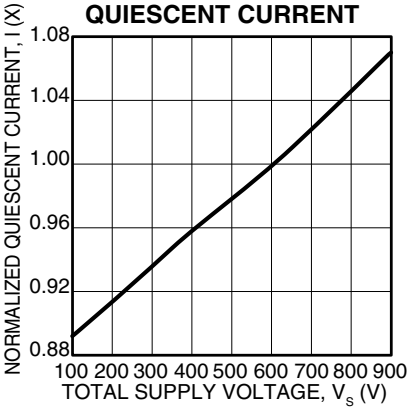
POWER DERATING



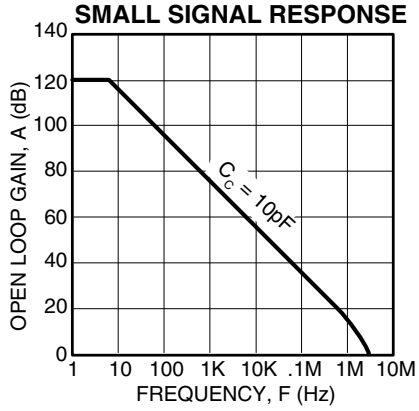
PHASE RESPONSE



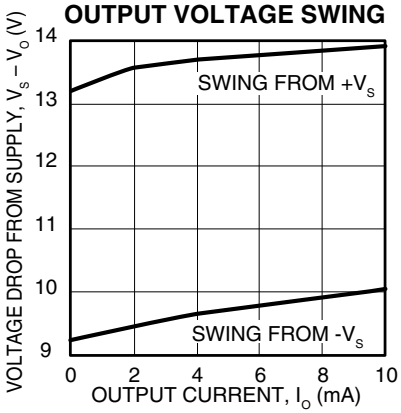
QUIESCENT CURRENT



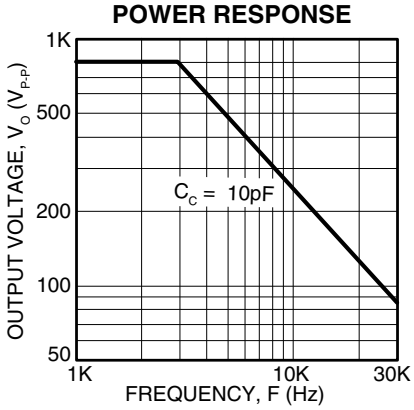
SMALL SIGNAL RESPONSE



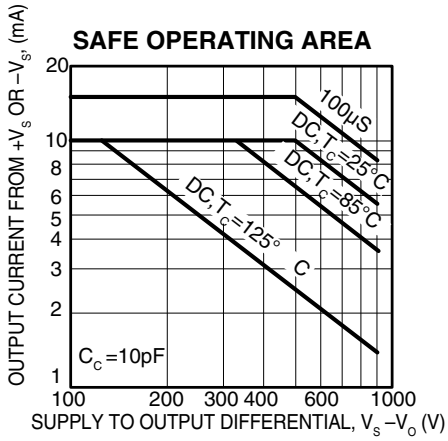
OUTPUT VOLTAGE SWING



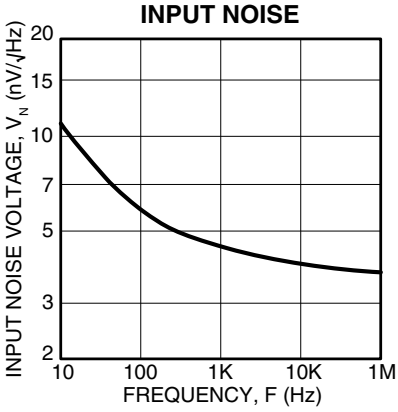
POWER RESPONSE



SAFE OPERATING AREA



INPUT NOISE



GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

CURRENT LIMIT

The PA97DR has no provision for current limiting the output.

COMMON MODE INPUT RANGE

Operational amplifiers are usually designed to have a common mode input voltage range that approximates the power supply voltage range. However, to keep the cost as low as possible and still meet the requirements of most applications the common mode input voltage range of the PA97DR is restricted. The input pins must always be a least 30V from either supply voltage but never more than 500V. This means that the PA97 cannot be used in applications where the supply voltages are extremely unbalanced. For example, supply voltages of +800V and –100V would not be allowed in an application where the non-inverting pin is grounded because in normal operation both input pins would be at 0V and the difference voltage between the positive supply and the input pins would be 800V. In this kind of application, however, supply voltages +500V and -100V does meet the input common mode voltage range requirements since the maximum difference voltage between the inputs pins and the supply voltage is 500V (the maximum allowed). The output has no such restrictions on its voltage swing. The output can swing within 24V of either supply voltage regardless of value so long as the total supply voltage does not exceed 900V.

INPUT PROTECTION

Although the PA97DR can withstand differential input voltages up to ±20V, additional external protection is recommended. In most applications 1N4148 or 1N914 signal diodes are sufficient (D1, D2 in Figure 2a). In more demanding applications where low leakage or low capacitance are of concern 2N4416 or 2N5457-2N5459 JFETs connected as diodes will be required (Q1, Q2 in Figure 2b). In either case the input differential voltage will be clamped to ±.7V. This is sufficient overdrive to produce maximum power bandwidth. Note that this protection does not automatically protect the amplifier from excessive common mode input voltages.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversal as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

EXTERNAL COMPONENTS

The compensation capacitor Cc must be rated for the total supply voltage. 10pF NPO (COG)capacitor rated at 1kV is recommended.

Of equal importance is the voltage rating and voltage coefficient of the gain setting feedback resistor. Typical voltage ratings of low wattage resistors are 150 to 250V. Up to 900 V can appear across the feedback resistor. High voltage rated resistors can be obtained. However a 1 megohm feedback resistor composed of five 200k resistors in series will produce the proper voltage rating.

CAUTIONS

The operating voltages of the PA97DR are potentially lethal. During circuit design develop a functioning circuit at the lowest possible voltages. Clip test leads should be used for "hands off" measurements while troubleshooting. With no internal current limit, proper choice of load impedance and supply voltage is required to meed SOA limitiations. An output short circuit will destroy the amplifier within milliseconds.

STABILITY

The PA97DR is stable at gains of 10 or more with a NPO (COG) compensation capacitor of 10pF. The compensation capacitor, Cc, in the external connections diagram must be rated at 1000V working voltage and mounted closely to pins 4 and 6 to prevent spurious oscillation. A compensation capacitor less than 10pF is not recommended.