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19-5243; Rev 0; 4/10

# Phase Redundancy Power Supervisor



## General Description

The MAX5973 protects individual slave phases of a phase redundant DC-DC converter. The power protection functions comprise an electronic circuit-breaker controller driving an external n-channel MOSFET at the step-down power input, and an internal 3.3V switch for the slave phase-controller power. To protect the output bus, an “ideal diode” controller drives an external n-channel MOSFET at the slave phase output. Serial data to and from the slave phase is buffered by the MAX5973 to prevent a failure of one phase from interrupting communication to the remaining phases. Similarly, the differential analog error signals for the phase controller are also buffered.

An overvoltage comparator and switched-node monitoring function allows the MAX5973 to disable a phase that has a shorted (or latched-on) high-side MOSFET.

A fault-status output and a $\overline{\text{FAULTIN}}$ input allow a master device to monitor and control each MAX5973 device.

The MAX5973 is offered in a 5mm x 5mm, 40-pin TQFN package and is fully specified from -40°C to +85°C.

## Applications

Phase Redundant DC-DC Converters

Step-Down Power Supplies

## Features

- **9V to 14V Operating Range**
- **Electronic Circuit-Breaker Controller Drives External n-Channel MOSFET**
- **Internal, 350mA MOSFET for 3.3V Power**
- **Open-Drain Ideal Diode Controller Drives External n-Channel MOSFET**
- **Serial Data Bus Loop/Bypass Function**
- **Serial Data Clock Buffer**
- **Dual Analog Error-Signal Buffer Amplifiers**
- **Active-Low $\overline{\text{FAULTIN}}$ Input**
- **Output Overvoltage and High-Side Switch Failure Protection**
- **Input and Output Undervoltage Lockout Functions**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX5973ETL+ | -40°C to +85°C | 40 TQFN-EP* |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

**EP = Exposed pad.*



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim’s website at www.maxim-ic.com.

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# Phase Redundancy Power Supervisor

## ABSOLUTE MAXIMUM RATINGS

PWR, CBSET, CBP, CBM, DOR, SOR, GOR to GND ..... -0.3V to +24V
GPS to GND ..... Capacitive Connection Only
$\overline{FAULTIN}$ to GND ..... -0.3V to ($V_{STBY}$ + 0.3V)
BYP, REFOUT to GND ..... -0.3V to +6V
CMPIN to GND ..... -0.3V to +4.5V
LXIN, AUXOV to GND ..... -0.3V to +4V
GPS ..... (GND - 0.3V) to ($V_{CBP}$ + 9V) (internally clamped)
STBY, AUXIN, AUXOUT, OVIN, OVREF to GND ..... -0.3V to +6V
ERRINA, ERRINB, ERROUTA, ERROUTB to GND ..... -0.3V to +6V
CMPOUT, $\overline{FAULTOUT}$, CLKIN, CLKOUT, BUSIN, BUSOUT, LOOPIN, LOOPOUT to GND ..... -0.3V to ($V_{STBY}$ + 0.3V)
PGND, AGND to GND ..... -0.3V to +0.3V
DOR to SOR ..... -1V to +6V
GMOUT to GND ..... -0.3V to +6V
$\overline{FAULTOUT}$ Current ..... +25mA
Input/Output Current (all other pins) ..... 20mA
Continuous Power Dissipation ($T_A$ = +70°C)
40-Pin TQFN, Single-Layer Board (derate 22.2mW/°C above +70°C) ..... 1777.8mW
40-Pin TQFN, Multilayer Board (derate 35.7mW/°C above +70°C) ..... 2857.1mW
Junction-to-Ambient Thermal Resistance (Note 1)
$\theta_{JA}$, Single-Layer Board ..... 45°C/W
$\theta_{JA}$, Multilayer Board ..... 35.7°C/W
Junction-to-Case Thermal Resistance (Note 1)
$\theta_{JC}$, Single-Layer and Multilayer Board ..... 2°C/W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{STBY}$ = 3.3V, $V_{AUXIN}$ = 3.3V, $V_{PWR}$ = 9V to 14V, $T_J$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{STBY}$ = 3.3V, $V_{PWR}$ = 12V, $V_{AUXIN}$ = 3.3V, and $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| PWR Operating Voltage Range | $V_{PWR}$ | | 9 | | 14 | V |
| Supply Current | $I_{PWR}$ | $V_{PWR}$ = 14V | | 3.75 | 6.5 | mA |
| PWR Undervoltage Lockout | $V_{PWR,UV}$ | $V_{PWR}$ rising | | 8.25 | 9 | V |
| PWR Undervoltage Lockout Hysteresis | $V_{PWR,UV-HYS}$ | $V_{PWR}$ falling | | 1 | | V |
| Internal Regulator | $V_{BYP}$ | | | 5.25 | | V |
| STBY Operating Voltage Range | $V_{STBY}$ | | 2.75 | | 5.5 | V |
| STBY Undervoltage Lockout | $V_{STBY,UV}$ | $V_{STBY}$ rising | 2.15 | 2.45 | 2.75 | V |
| STBY Undervoltage Lockout Hysteresis | $V_{STBY,UV-HYS}$ | $V_{STBY}$ falling | | 100 | | mV |
| STBY Current | $I_{STBY}$ | $V_{STBY}$ = 5.5V | | 2.5 | 5 | mA |
| **PRECISION CONTROL INPUT ($\overline{FAULTIN}$)** | | | | | | |
| Leakage Current | $I_{\overline{FAULTIN}}$ | $V_{STBY}$ = $V_{\overline{FAULTIN}}$ = 5.5V | | | 1 | µA |
| $\overline{FAULTIN}$ Low Delay | $t_{SD}$ | $V_{\overline{FAULTIN}}$ < $V_{IL}$ to $V_{GPS}$ - $V_{CBP}$ = 2V, $C_{GPS}$ = 12nF | | 750 | 1500 | ns |
| Startup Fault Blanking Time | $t_{SU}$ | $\overline{FAULTIN}$ low > $V_{AUXIN}$ > $V_{AUXIN,UV}$ to $V_{\overline{FAULTOUT}}$ < $V_{OL\_\overline{FAULTOUT}}$ | 9 | 10 | 11.25 | ms |
| **UNCOMMITTED COMPARATOR (CMPIN)** | | | | | | |
| Comparator Reference | $V_{CMP,REF}$ | $V_{CMPIN}$ rising | 1.18 | 1.23 | 1.28 | V |
| Leakage Current | $I_{CMPIN}$ | $V_{CMPIN}$ = 2V | | | 1 | µA |


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## ELECTRICAL CHARACTERISTICS (continued)

($V_{STBY}$ = 3.3V, $V_{AUXIN}$ = 3.3V, $V_{PWR}$ = 9V to 14V, $T_J$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{STBY}$ = 3.3V, $V_{PWR}$ = 12V, $V_{AUXIN}$ = 3.3V, and $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Hysteresis | $V_{CMP,HYS}$ | $V_{CMPIN}$ falling | | 25 | | mV |
| **POWER SWITCH DRIVER (GPS, CBSET, CBP, CBM)** | | | | | | |
| GPS High Voltage | $V_{GPS,HI}$ | $V_{PWR} \geq$ 10V, $\overline{FAULTIN}$ high, relative to CBP | 7 | 8 | 10 | V |
| | | $V_{PWR}$ < 10V | 5.5 | 7.5 | 9.0 | |
| GPS High Comparator Threshold | $V_{GPS,TH}$ | $V_{GPS}$ - $V_{CBM}$ | 4.5 | 5 | 5.5 | V |
| GPS Pullup Current | $I_{GPS,UP}$ | $V_{GPS}$ = $V_{GPSHI}$ - 2V | 17 | 20 | 23 | µA |
| GPS Pulldown Current | $I_{GPS,DN}$ | $V_{GPS}$ - $V_{CBP}$ = 2V | | 500 | | mA |
| GPS Pulldown Resistance | $R_{GPS,DN}$ | $I_{GPS}$ = 400mA | | | 15 | Ω |
| CBSET Voltage Range | | $V_{PWR}$ - $V_{CBSET}$ | 10 | | 80 | mV |
| Circuit-Breaker Offset Voltage | | $V_{CBSET}$ - $V_{CBM}$ | -2 | | +2 | mV |
| CBSET Current | $I_{CBSET}$ | | 19.5 | 20 | 20.5 | µA |
| Circuit-Breaker Response Time | $t_{CB}$ | ($V_{CBP}$ - $V_{CBM}$) = ($V_{CBP}$ - $V_{CBSET}$) + 10mV to $V_{GPS}$ - $V_{CBP}$ = 2V, $C_{GPS}$ = 12nF | | 225 | 375 | ns |
| **INTERNAL POWER SWITCH (AUXIN, AUXOUT, AUXOV)** | | | | | | |
| AUXIN, AUXOUT Operating Range | $V_{AUX}$ | | 2.6 | | 5.5 | V |
| AUX On-Resistance | $R_{ON}$ | AUXIN to AUXOUT, $I_{AUXOUT}$ = 75mA | | 350 | 500 | mΩ |
| AUX Circuit-Breaker Threshold | $I_{AUX,CB}$ | | 300 | 350 | 400 | mA |
| AUXIN Undervoltage Lockout | $V_{AUXIN,UV}$ | $V_{AUXIN}$ rising | 2.30 | 2.45 | 2.6 | V |
| AUXIN Undervoltage Lockout Hysteresis | $V_{AUXIN,UV-HYS}$ | $V_{AUXIN}$ falling | | 100 | | mV |
| AUXOUT Undervoltage Lockout | $V_{AUXOUT,UV}$ | $V_{AUXOUT}$ rising | 2.0 | 2.15 | 2.3 | V |
| AUXOUT Undervoltage Lockout Hysteresis | $V_{AUXOUT, UV-HYS}$ | $V_{AUXOUT}$ falling | | 100 | | mV |
| Overvoltage Protection Threshold | $V_{AUXOV,TH}$ | | 690 | 700 | 710 | mV |
| AUXOUT Startup dV/dt | $SR_{AUXOUT}$ | $C_{AUXIN}$ = 10µF, $C_{AUXOUT}$ = 1µF | 7.5 | 11.5 | 17 | kV/s |
| AUXOV Leakage Current | $I_{AUXOV}$ | $V_{AUXOV}$ = 700mV | -1 | | +1 | µA |
| **IDEAL DIODE DRIVER (GOR, SOR, DOR)** | | | | | | |
| SOR, DOR Common-Mode Range | | Relative to GND | 0.050 | | 6.0 | V |
| SOR Input Resistance to Ground | $R_{SOR}$ | $V_{SOR}$ = 5V | 0.5 | 1 | 2 | MΩ |



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## ELECTRICAL CHARACTERISTICS (continued)

($V_{STBY}$ = 3.3V, $V_{AUXIN}$ = 3.3V, $V_{PWR}$ = 9V to 14V, $T_J$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{STBY}$ = 3.3V, $V_{PWR}$ = 12V, $V_{AUXIN}$ = 3.3V, and $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| DOR Input Resistance to Ground | $I_{DOR}$ | $V_{DOR}$ = 5V | 0.5 | 1 | 2 | MΩ |
| GOR Input Current | $I_{GOR,DN}$ | $V_{GOR}$ = $V_{SOR}$ + 2V | | 2 | | A |
| GOR Input Resistance | $R_{GOR,DN}$ | $I_{GOR}$ = 400mA | | | 2 | Ω |
| GOR Input Resistance to Ground | $I_{GOR,HI}$ | $V_{GOR}$ = 12V | 0.5 | 1 | 2 | MΩ |
| Reverse-Current Blocking Threshold | $V_{RCBLK}$ | $V_{DOR}$ - $V_{SOR}$ rising | 3 | 5 | 7 | mV |
| Reverse-Current Blocking Hysteresis | $V_{RCHYS}$ | $V_{DOR}$ - $V_{SOR}$ falling | | 3.3 | 10 | mV |
| Reverse-Current Blocking Response Time | $t_{RCBLK}$ | $V_{DOR}$ - $V_{SOR}$ = $V_{RCBLK}$ + 10mV to $V_{GOR}$ = $V_{SOR}$ + 2V with $C_{GOR}$ = 6.5nF, $R_{GOR}$ = 1kΩ | | 250 | 400 | ns |
| **SWITCH NODE MONITOR (LXIN)** | | | | | | |
| LXIN Overvoltage Threshold | $V_{LXIN,TH}$ | $V_{LXIN}$ rising | 690 | 700 | 710 | mV |
| LXIN Overvoltage Hysteresis | $V_{LXIN,HYS}$ | $V_{LXIN}$ falling | | 25 | | mV |
| LXIN Overvoltage Response Time | $t_{LXIN}$ | $V_{LXIN}$ - $V_{LXIN,TH}$ = 50mV to $V_{GPS}$ - $V_{CBP}$ = 2V, $C_{GPS}$ = 12nF | | 250 | 400 | ns |
| Leakage Current | $I_{LXIN}$ | $V_{LXIN}$ = 700mV | | | 1 | µA |
| **ERROR SIGNAL BUFFER AMPLIFIER (ERRINA, ERRINB, ERROUTA, ERROUTB)** | | | | | | |
| Input Offset Voltage | $V_{OS}$ | | -8 | 0 | +8 | mV |
| Common-Mode Voltage Range | $V_{CM}$ | Relative to GND | 0.1 | | 3.3 | V |
| ERRIN_ Bias Current | $I_{ERRIN\_}$ | $V_{ERRIN\_}$ = 0.1V to 3.3V | | | 200 | nA |
| Gain | $AV_{ERRIN\_}$ | $V_{ERRIN\_}$ = 0.2V to 3.3V, $I_{ERROUT}$ = 100µA | 0.995 | 1.000 | 1.005 | V/V |
| Power-Supply Rejection Ratio | PSRR | To PWR at f = 10kHz | | 85 | | dB |
| | | To PWR at f = 1MHz | | 50 | | |
| -3dB Bandwidth | BW | | | 8 | | MHz |
| Slew Rate | SR | | | 5 | | V/µs |
| Output Short-Circuit Current | $I_{ERROUT\_SC}$ | Sourcing at 10mV error, $V_{ERRIN\_}$ = 3.3V | | 750 | | µA |
| | | Sinking at 10mV error, $V_{ERRIN\_}$ = 1.0V | | 350 | | |
| | | Sinking at 10mV error, $V_{ERRIN\_}$ = 100mV | | 70 | | |



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## ELECTRICAL CHARACTERISTICS (continued)

($V_{STBY}$ = 3.3V, $V_{AUXIN}$ = 3.3V, $V_{PWR}$ = 9V to 14V, $T_J$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{STBY}$ = 3.3V, $V_{PWR}$ = 12V, $V_{AUXIN}$ = 3.3V, and $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **SERIAL BUS LOOP/BYPASS (BUSIN, LOOPOUT, LOOPIN, BUSOUT, CLKIN, CLKOUT, $\overline{FAULTIN}$)** | | | | | | |
| Input Logic-Low (BUSIN, LOOPIN, CLKIN, $\overline{FAULTIN}$) | $V_{IL\_}$ | | | | 0.25 x $V_{STBY}$ | V |
| Input Logic-High (BUSIN, LOOPIN, CLKIN, $\overline{FAULTIN}$) | $V_{IH\_}$ | | 0.7 x $V_{STBY}$ | | | V |
| Output Logic-Low (LOOPOUT, BUSOUT, CLKOUT) | $V_{OL\_}$ | Sinking 3mA | | | 200 | mV |
| Output Logic-High (LOOPOUT, BUSOUT, CLKOUT) | $V_{OH\_}$ | Sourcing 3mA | 0.9 x $V_{STBY}$ | | | V |
| BUSIN Leakage Current | $I_{BUSIN}$ | $V_{BUSIN}$ = $V_{STBY}$ = 5.5V | | | 1 | µA |
| LOOPIN Leakage Current | $I_{LOOPIN}$ | $V_{LOOPIN}$ = $V_{STBY}$ = 5.5V | | | 1 | µA |
| CLKIN Leakage Current | $I_{CLKIN}$ | $V_{CLKIN}$ = $V_{STBY}$ = 5.5V | | | 1 | µA |
| Propagation Delay | $t_{PD\_BUS}$ | BUSIN to LOOPOUT | | 20 | | ns |
| | | LOOPIN to BUSOUT | | 20 | | |
| | | BUSIN to BUSOUT | | 20 | | |
| | | CLKIN to CLKOUT | | 20 | | |
| **OPEN-DRAIN OUTPUT ($\overline{FAULTIN}$, CMPOUT)** | | | | | | |
| Output Logic-Low | $V_{OL\_\overline{FAULTOUT}}$ | $I_{\overline{FAULTOUT}}$ = 5mA, $I_{CMPOUT}$ = 5mA | | | 0.4 | V |
| Open-Drain Leakage Current | $I_{LKG\_\overline{FAULTOUT}}$ | $V_{\overline{FAULTOUT}}$ = $V_{STBY}$ = 5.5V, $V_{CMPOUT}$ = 5.5V | | | 1 | µA |
| **REFOUT** | | | | | | |
| Reference Voltage | $V_{REFOUT}$ | $I_{REFOUT}$ = 1mA | 690 | 700 | 710 | mV |
| **CURRENT-AMPLIFIER OUTPUT (GMOUT)** | | | | | | |
| Transconductance | | $V_{CBP}$ - $V_{CBM}$ = 10mV to 80mV | 9 | 10 | 11 | mA/V |
| Input Offset Voltage | $V_{CBP}$ - $V_{CBM}$ | $V_{CBP}$ - $V_{CBM}$ = 10mV, $I_{GMOUT}$ = 100µA | -2 | | +2 | mV |
| Transconductance Temperature Variation | $T_{GMOUT}$ | $V_{CBP}$ - $V_{CBM}$ = 80mV, $T_A$ = +25°C to +85°C | | 85 | | ppm/°C |
| Input Range for $V_{CBP}$ - $V_{CBM}$ | | | | | 80 | mV |
| Input Bias Current | $I_{CBP}$ | $V_{CBP}$ = $V_{CBM}$ = 12V | -1 | | +1 | µA |
| | $I_{CBM}$ | $V_{CBP}$ = $V_{CBM}$ = 12V | -1 | | +1 | |
| Maximum Output Voltage | | | 3 | | | V |
| Output Resistance | | $V_{CBP}$ - $V_{CBM}$ = 80mV | | 350 | | kΩ |



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## ELECTRICAL CHARACTERISTICS (continued)

($V_{STBY}$ = 3.3V, $V_{AUXIN}$ = 3.3V, $V_{PWR}$ = 9V to 14V, $T_J$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{STBY}$ = 3.3V, $V_{PWR}$ = 12V, $V_{AUXIN}$ = 3.3V, and $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **OVERVOLTAGE COMPARATOR (OVREF, OVIN)** | | | | | | |
| OVIN Voltage Range | | $V_{OVREF} > V_{LCKOUT}$ | 0.425 | | 2 | V |
| OVREF Voltage Range | | | $V_{LCKOUT}$ | | 2 | V |
| OVREF Lockout Voltage | $V_{LKCOUT}$ | $V_{OVREF}$ rising, $V_{OVREF} < V_{LCKOUT}$ disables OVREF comparator | 425 | 450 | 475 | mV |
| OVREF Lockout Voltage Hysteresis | $V_{OVREF,HYS}$ | | | 37.5 | | mV |
| OVIN Input Offset Error | | $V_{OVREF}$ = 700mV | -5 | 0 | +5 | mV |
| OVIN Comparator Hysteresis | $V_{OVIN,HYS}$ | | | 50 | | mV |
| OVIN, OVREF Input Leakage Current | $I_{LKG\_OVIN}$ | $V_{OVIN}$ = 700mV | | | 1 | µA |
| Propagation Delay | $t_{PD\_OVIN}$ | $V_{OVIN}$ - $V_{OVREF}$ = 50mV to $V_{GPS}$ - $V_{CBP}$ = 2V, $C_{GPS}$ = 12nF | | 325 | 500 | ns |
| **THERMAL CHARACTERISTICS** | | | | | | |
| Thermal Shutdown | | $T_J$ rising | | +150 | | °C |
| Thermal Shutdown Hysteresis | | $T_J$ falling | | 20 | | °C |

**Note 2:** All devices 100% production tested at $T_A$ = +25°C and $T_A$ = +85°C. Limits over the temperature range are guaranteed by design.



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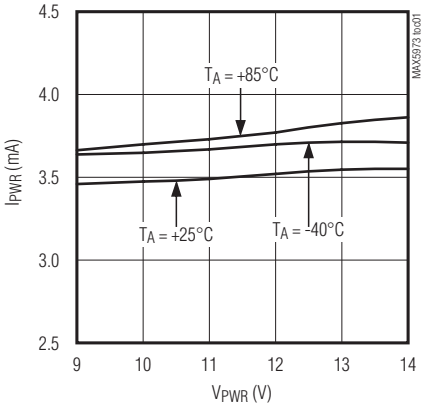
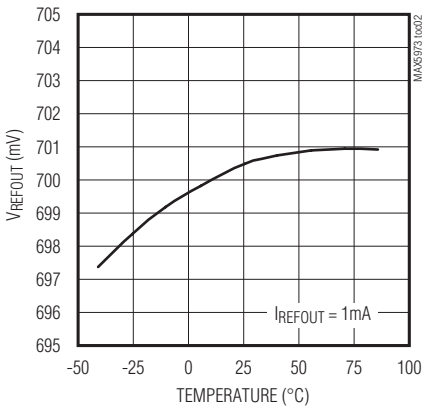
## Typical Operating Characteristics

($V_{STBY}$ = 3.3V, $V_{AUXIN}$ = 3.3V, $V_{PWR}$ = 12V, $C_{GPS}$ = 12nF, and $T_A$ = +25°C, unless otherwise noted.)

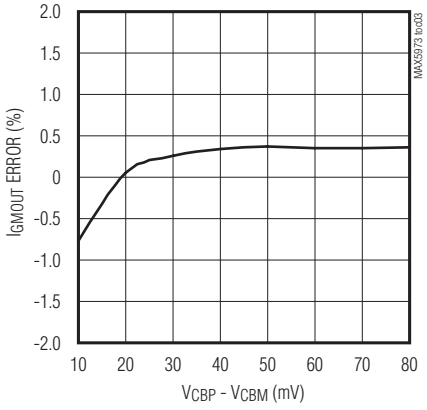
**IPWR vs. VPWR**



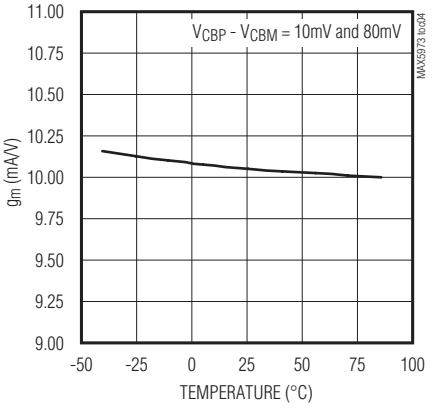

**VREFOUT vs. TEMPERATURE**



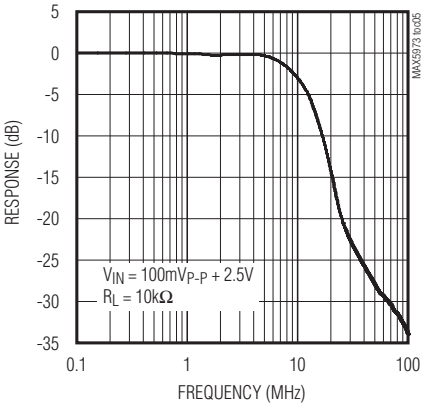

**IGMOUT ERROR vs. VCBP - VCBM**



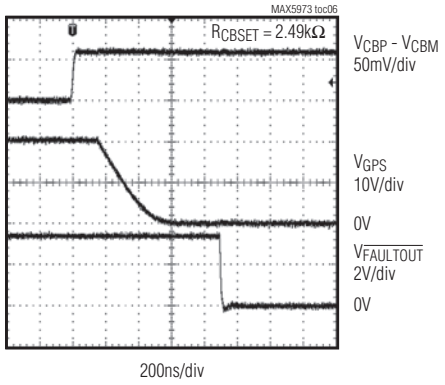

**TRANSCONDUCTANCE vs. TEMPERATURE**



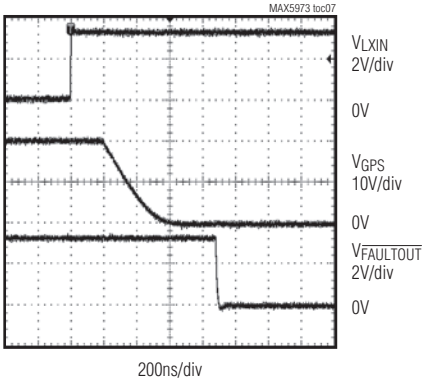

**ERROR-AMPLIFIER FREQUENCY RESPONSE**




**CIRCUIT BREAKER TO GPS LOW AND FAULTOUT LOW-RESPONSE TIME**




**LXIN TO GPS LOW AND FAULTOUT LOW-RESPONSE TIME**



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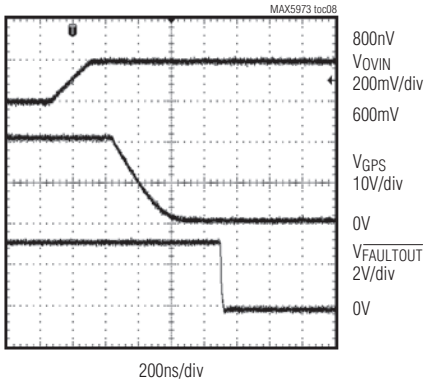
# Phase Redundancy Power Supervisor

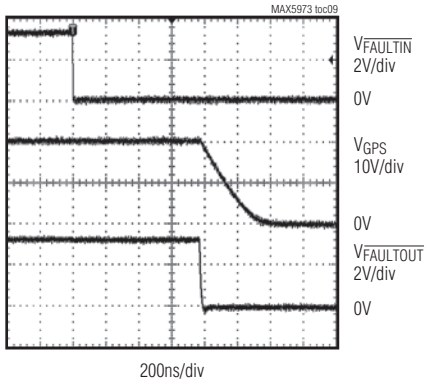
## Typical Operating Characteristics (continued)

($V_{STBY}$ = 3.3V, $V_{AUXIN}$ = 3.3V, $V_{PWR}$ = 12V, $C_{GPS}$ = 12nF, and $T_A$ = +25°C, unless otherwise noted.)

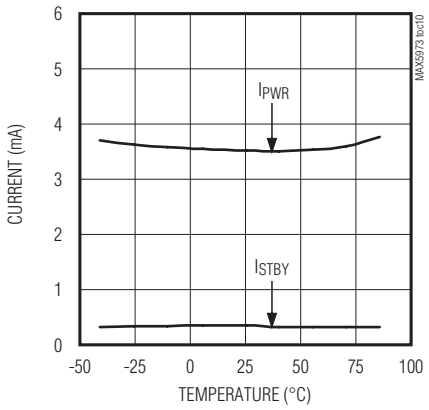
**OVIN TO GPS LOW AND $\overline{FAULTOUT}$ LOW-RESPONSE TIME**



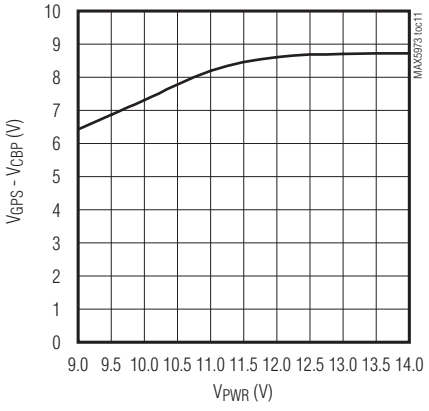

**$\overline{FAULTIN}$ TO GPS LOW AND $\overline{FAULTOUT}$ LOW-RESPONSE TIME**



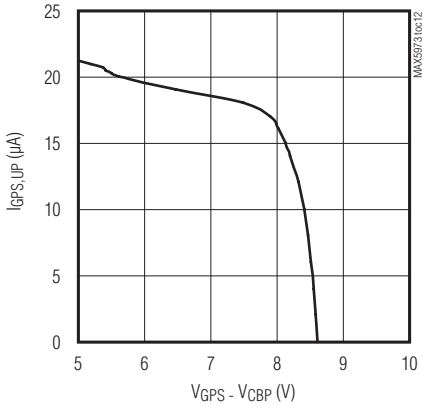

**$I_{PWR}$ AND $I_{STBY}$ vs. TEMPERATURE**



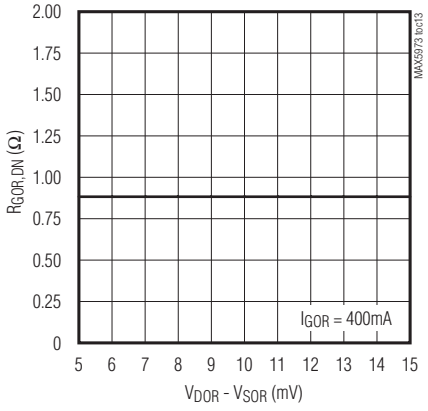

**$V_{GPS}$ - $V_{CBP}$ vs. $V_{PWR}$**



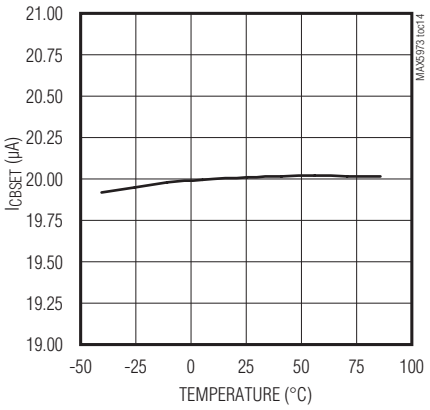

**$I_{GPS,UP}$ vs. $V_{GPS}$ - $V_{CBP}$**




**$R_{GOR,DN}$ vs. $V_{DOR}$ - $V_{SOR}$**




**$I_{CBSET}$ vs. TEMPERATURE**



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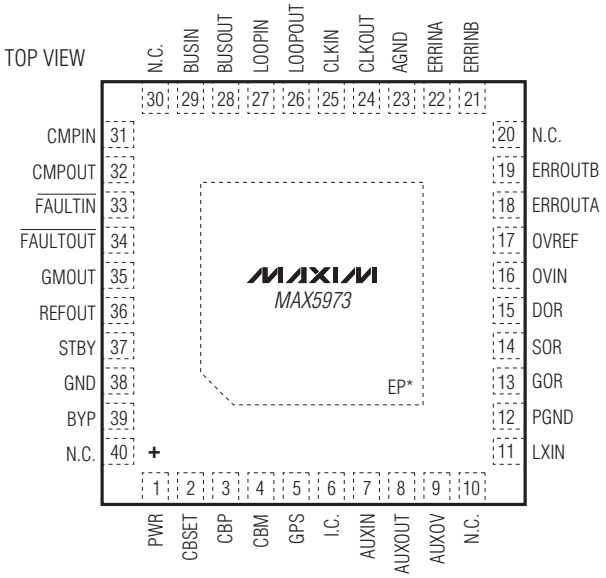
## Pin Configuration




*CONNECT TO AGND.

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | PWR | Power-Supply Input. Nominally 12V, with 9V UVLO. Connect to the 12V supply through a 10Ω to 100Ω resistor and bypass with a 1µF capacitor. |
| 2 | CBSET | 12V Circuit-Breaker Threshold Voltage Set Input. CBSET is driven by a 20µA current sink. Connect a resistor between CBSET and CBP to set the circuit-breaker trip threshold. |
| 3 | CBP | 12V Current-Sense Positive Input. Connect to the high side of an external sense resistor at the source of the 12V n-channel MOSFET switch. |
| 4 | CBM | 12V Current-Sense Negative Input. Connect to the low side of an external sense resistor at the drain of the 12V n-channel MOSFET switch. |
| 5 | GPS | Gate Drive For External 12V Input-Power n-Channel MOSFET Switch |
| 6 | I.C. | Internal Connection. Connect to GND. |
| 7 | AUXIN | Auxiliary 3.3V Power Switch Input |
| 8 | AUXOUT | Auxiliary 3.3V Power Switch Output. Connect to the 3.3V power input of the phase regulator. |
| 9 | AUXOV | Auxiliary 3.3V Power Switch Overvoltage Protection Input |
| 10, 20, 30, 40 | N.C. | No Connection. Not internally connected. |
| 11 | LXIN | High-Side Switch Failure Detection Input. If LXIN rises above the failure detection threshold voltage, the input switches will turn off to prevent a shorted high-side switch from causing an overvoltage condition. Connect to the phase converter's LX node through an RC divider-filter circuit. |
| 12 | PGND | Power Ground |



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# Phase Redundancy Power Supervisor

## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 13 | GOR | Gate Drive For External Output ORing n-Channel MOSFET Switch. This is an open-drain output with strong pulldown capability. |
| 14 | SOR | Source ORing Sense Connection. Connect SOR to the source of the external ORing n-channel MOSFET. |
| 15 | DOR | Drain ORing Sense Connection. Connect DOR to the drain of the external ORing n-channel MOSFET. |
| 16 | OVIN | Overvoltage Comparator Input. Connect to the output of the combined slave phases through a resistive divider. |
| 17 | OVREF | Overvoltage Comparator Reference Input. Connect to an overvoltage threshold reference that varies with the output-voltage set point. |
| 18 | ERROUTA | Channel A Analog Error Signal Unity-Gain Buffer Output |
| 19 | ERROUTB | Channel B Analog Error Signal Unity-Gain Buffer Output |
| 21 | ERRINB | Channel B Analog Error Signal Unity-Gain Buffer Input |
| 22 | ERRINA | Channel A Analog Error Signal Unity-Gain Buffer Input |
| 23 | AGND | Analog Signal Ground |
| 24 | CLKOUT | Clock Buffer Output. Connect to the slave phase data-clock input. |
| 25 | CLKIN | Clock Buffer Input. Connect to the master data-clock signal. |
| 26 | LOOPOUT | Serial Bus Loop Output. Serial bus loop output to the phase regulator. |
| 27 | LOOPIN | Serial Bus Loop Input. Serial bus loop input from the phase regulator. This input is normally connected to BUSOUT, but is disconnected and ignored in the event of a fault. |
| 28 | BUSOUT | Serial Bus Loop/Bypass Output. This output is connected to the LOOPIN input during normal operation, and connected to BUSIN in the event of a fault. Connect to the BUSIN input on the next phase, or return to the master data input if there are no more phases. |
| 29 | BUSIN | Serial Bus Loop/Bypass Input. This input is connected to LOOPOUT during normal operation, and internally connected to BUSOUT in the event of a fault. Connect to the bus master data output or BUSOUT of the previous phase. |
| 31 | CMPIN | Uncommitted Comparator Negative Input |
| 32 | CMPOUT | Uncommitted Comparator Open-Drain Output |
| 33 | $\overline{\text{FAULTIN}}$ | External Enable Control Input. Pull this input to ground to disable the associated phase regulator. |
| 34 | $\overline{\text{FAULTOUT}}$ | Open-Drain Fault Output. $\overline{\text{FAULTOUT}}$ asserts low if there is a failure of the associated phase controller. |
| 35 | GMOUT | Transconductance Current-Sense Amplifier Output. Connect all phases' GMOUT pins to a single resistor to sum the input currents for all phases in a domain. |
| 36 | REFOUT | Reference Output |
| 37 | STBY | Standby Power Input. Power to this input must be cycled to unlatch the device after a fault condition. |
| 38 | GND | Ground |
| 39 | BYP | Internal Regulator Bypass Connection. Connect to ground through a 1µF capacitor. |
| — | EP | Exposed Pad. Internally connected to AGND. Connect this thermal pad to the ground plane and use multiple vias to a solid copper pour on the bottom layer of the PCB. |



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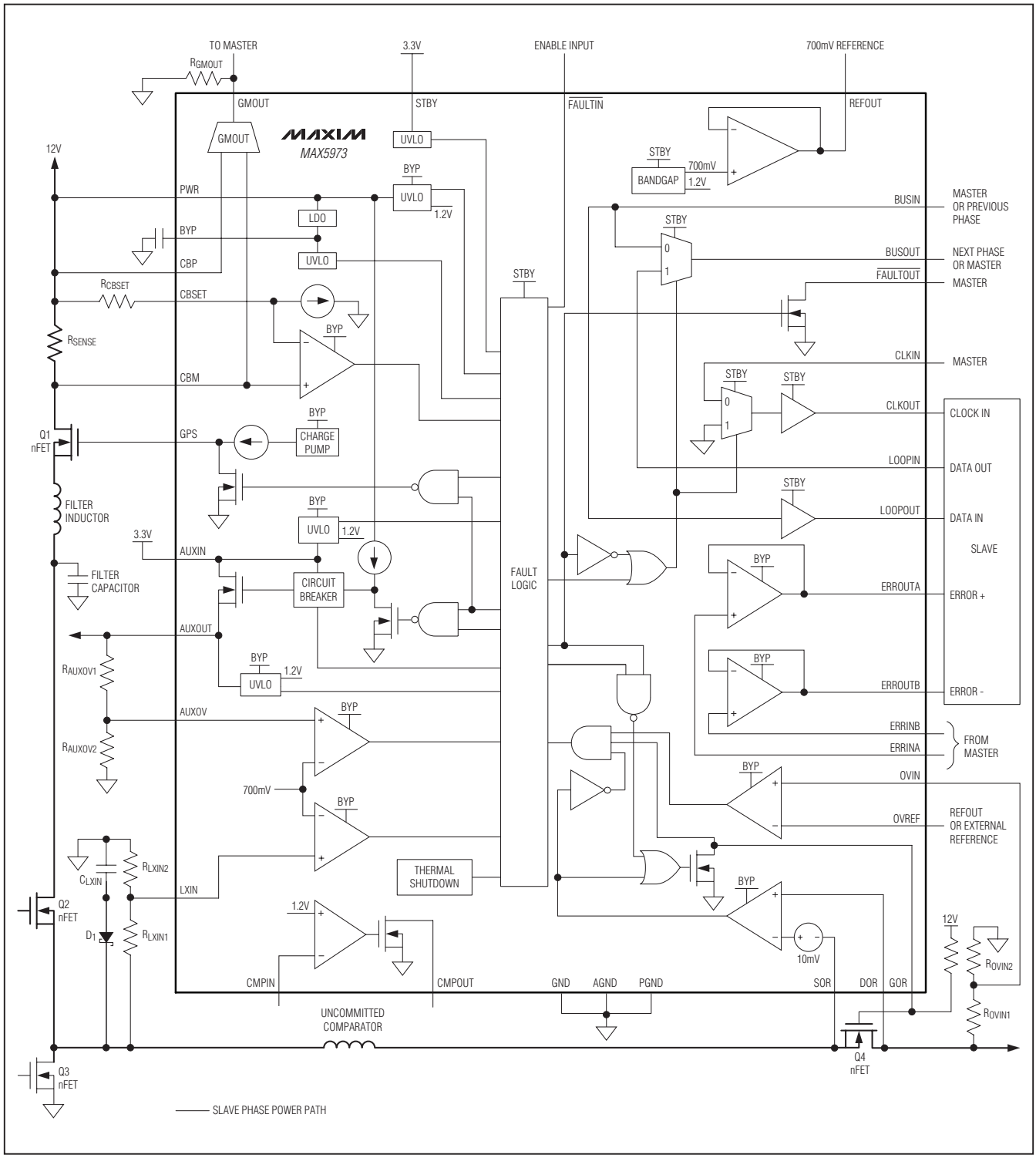
## Functional Diagram



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# Phase Redundancy Power Supervisor

## Detailed Description

The MAX5973 phase redundancy power supervisor monitors and protects an individual slave phase in phase redundant DC-DC converters.

The device features an external power switch and an "ideal diode" ORing controller that isolates an individual slave from the multiphase DC-DC converter combined input and output when a fault is present. The programmable circuit breaker sets the current limit of the slave phase and generates a fault response when it is exceeded. An integrated transconductance current-sense amplifier continuously monitors the current flowing through the external power switch during normal operation. To provide true phase-redundancy, the ORing diode controller drives an n-channel reverse-current blocking MOSFET at the output of the slave. An internal auxiliary power switch allows the MAX5973 to monitor and protect the 3.3V supply powering the slave phase controller against undervoltage, overvoltage, and overcurrent conditions. A comparator input monitors the switching node of the slave phase for high-side switch failure detection, and an overvoltage comparator input monitors the combined multiphase DC-DC converter output for overvoltage conditions.

The MAX5973 also features a serial bus loop/bypass, clock buffer, error signal buffers, an uncommitted comparator, and thermal shutdown protection.

### Fault Output

The $\overline{FAULTOUT}$ output is an open-drain output that is driven low whenever a fault condition has occurred. The $\overline{FAULTOUT}$ output latches low in the event of any of the following conditions:

When any of the fault conditions listed in Table 1 occur, the part will trigger a fault condition and the events in Table 2 will occur.

Once a fault condition has occurred, the only way to clear the fault condition is by cycling the STBY voltage below its undervoltage threshold.

### Fault Input

The $\overline{FAULTIN}$ input is a logic-level input. After a power-up is initiated, the MAX5973 will wait for approximately 10ms after AUXOUT has risen above its undervoltage lockout threshold. At this time, the device will check the status of the $\overline{FAULTIN}$ input. If the voltage at $\overline{FAULTIN}$ is below $V_{IL}$, the MAX5973 will initiate a fault which will pull the GPS and GOR gate-drive outputs low and shut down the internal power switch between AUXOUT and AUXIN. In addition, any time after a normal power-up, the $\overline{FAULTIN}$ input can be driven low by the user to cause the GPS and GOR outputs to pull down and the internal power switch to shut down.

## Table 1. Fault Conditions

| EVENTS THAT CAUSE A LATCHED FAULT | |
|---|---|
| **TYPE OF FAULT** | **DESCRIPTION** |
| $\overline{FAULTIN}$ Low | $\overline{FAULTIN}$ input is pulled below the $V_{IL}$ threshold after power-up |
| $I_{MAIN}$ Fault | GPS pulled low because of CBP/CBM circuit-breaker trip |
| $V_{GPS}$ Fault | GPS output below $V_{GPS,TH}$ for longer than $t_{SU}$ (when commanded high on power-up) **or** AUXOUT below its undervoltage lockout threshold after $t_{SU}$ (when commanded high on power-up) |
| $I_{AUX}$ Fault | AUXIN/AUXOUT circuit-breaker trip |
| $V_{AUX}$ Fault | AUXOV input above 700mV threshold |
| Overvoltage Fault | Output overvoltage fault (OVIN above OVREF and OVREF above $V_{LCKOUT}$) combined with GOR commanded high (i.e., slave forcing overvoltage) |
| LXIN Fault | Failed high-side switch or excessive duty cycle |
| Slave Startup Failed | $\overline{FAULTIN}$ was not high by $t_{SU}$ = 10ms after $UVLO_{AUXOUT}$ satisfied |
| $V_{GPS}$ Failure | GPS goes below $V_{GPS,TH}$ for 10ms any time after the part has powered up |
| Thermal Shutdown | Thermal shutdown circuit has activated |

## Table 2. Fault Response

| FAULT RESPONSE | |
|---|---|
| **ACTION** | **DESCRIPTION** |
| BUSIN routed to BUSOUT | The MUX that drives the BUSOUT signal will allow the BUSIN signal to pass directly to BUSOUT |
| CLKOUT pulled low | CLKOUT will be driven low |
| GOR pulled low | GOR will be pulled low by the $I_{GOR,DN}$ current (2A typ) |
| GPS pulled low | GPS will be pulled low by the $I_{GPS,DN}$ current (500mA typ) |
| AUXIN to AUXOUT switch opened | The gate of the switch connecting AUXIN to AUXOUT will be pulled low |
| $\overline{FAULTOUT}$ pulled low | An open-drain driver will pull $\overline{FAULTOUT}$ low |



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### External Power Switch Controller

The MAX5973 includes an electronic circuit-breaker controller for an external high-side n-channel switch. This switch allows or blocks +12V input power to the slave DC-DC controller. The GPS output drives the gate of the external MOSFET to +8V above the voltage present at CBP.

An external sense resistor placed at the drain of the external MOSFET is used to detect overcurrent events. The CBP and CBM inputs are connected across this resistor to measure the input current.

A precision current sink drives the CBSET input; a resistor connected between CBP and CBSET establishes a circuit-breaker threshold. If the voltage across the sense resistor (CBP to CBM) exceeds the voltage across the set resistor (CBP to CBSET), the GPS output pulls the gate of the external MOSFET to CBP, and eventually to ground, blocking the flow of current to a shorted phase.

The GPS output is also pulled low if $\overline{\text{FAULTIN}}$ is low, or in the event of an overvoltage fault (confirmed by the ideal-diode controller) or the switched-node monitor. A circuit-breaker shutdown of the internal power switch will also cause GPS to pull down with a 500mA (typ) current sink.

### Transconductance Current-Sense Amplifier

The MAX5973 includes a precision transconductance amplifier that senses the voltage between CBP and CBM, and outputs a current signal at GMOUT. This signal can be combined in parallel with the GMOUT signals from other MAX5973 devices to provide a summed current-sense signal for all phases in a redundant-phase converter.

The GMOUT pins of all MAX5973 devices in a multiphase converter should be connected to a single resistor to ground. The voltage across this resistor is proportional to the combined input current of all phases. Appropriate selection of the resistor value allows the voltage gain of the current-sense signals to be tailored to the requirements of an analog-to-digital converter.

To generate an accurate average current signal, the external current-sense resistor should be separated from the high-side switch of the step-down phase by an LC filter. Otherwise, large step current pulses at the input of the phase will cause inaccurate current-sense output.

### Ideal ORing Diode Controller

The MAX5973 controls an external n-channel MOSFET at the output of the redundant phase to prevent reverse current flow, while still allowing forward current to flow with low resistive loss and voltage drop.

During normal operation, the open-drain GOR output is high impedance to allow an external pullup resistor to drive the gate of this external n-channel switch above the potential at SOR. If the differential voltage between the DOR and SOR inputs exceeds 5mV, the GOR output pulls down with a 2A (typ) current sink to SOR, blocking reverse current. When DOR falls to 1.7mV or less above SOR, the GOR output goes high impedance again to allow forward current flow from the phase.

The state of the GOR output is used in conjunction with the overvoltage comparator to determine if the associated phase is driving an overvoltage condition.

### Auxiliary 3.3V Power Switch

An internal MOSFET and current-sense circuit is used to control 3.3V power to the slave phase controller. During normal operation, 3.3V power flows through the MAX5973 from AUXIN to AUXOUT and to the redundant phase controller.

If the current exceeds the internal 350mA (typ) $I_{AUX,CB}$ circuit-breaker threshold, the internal switch is disabled and the MAX5973 shuts down the phase. In addition, the GPS output will pull down and block 12V power as well.

An undervoltage lockout feature prevents power from flowing through the internal switch below the $V_{AUXIN,UV}$ threshold.

A programmable overvoltage protection function is implemented by connecting a resistor-divider from AUXOUT to AUXOV to ground. If the AUXOV input rises above its 700mV threshold, a fault condition is detected and the MAX5973 shuts down all switches and pulls the $\overline{\text{FAULTOUT}}$ output low.

If the internal power switch will not be used, AUXIN should be connected to STBY, AUXOUT should be left unconnected, and AUXOV should be connected to ground.

### Switched-Node Monitor

The LXIN input is connected through an RC filter to the high side of the inductor of the associated DC-DC phase. This input is monitored by an overvoltage comparator. If the voltage at LXIN rises above $V_{LXIN,TH}$, the MAX5973 concludes that the high-side converter switch has failed. Under this condition, the MAX5973 pulls down and latches the GPS and GOR gate-drive outputs to isolate the failed phase and prevent an overvoltage condition at the load.



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# Phase Redundancy Power Supervisor

The RC filter between the inductor and LXIN should be designed so that switching at normal duty cycle does not cause LXIN to rise above $V_{LXIN,TH}$. A small Schottky diode can be used to discharge the RC filter when the rectifier is conducting, allowing cycle-by-cycle protection.

### Overvoltage Comparator

The OVIN input is connected to the load voltage (combined output of all phases) and is compared to the OVREF input voltage. If OVIN rises above OVREF while the GOR output is low because reverse current is present, the MAX5973 will take no action and will wait for OVIN to fall below OVREF. However, if OVIN is above OVREF and the GOR output is also high, the MAX5973 has detected a failure in its associated phase controller (it is driving the overvoltage condition) and will pull down and latch the GPS and GOR outputs.

### Thermal Shutdown

The MAX5973 features thermal shutdown. When the junction temperature of the device exceeds +150°C (typ), a fault response disables the slave phase of the device. The fault condition remains until the junction temperature drops by 20°C (typ) and the voltage at STBY is cycled below its UVLO threshold.

### Serial Bus Loop/Bypass and Clock Buffer

The MAX5973 incorporates logic that normally routes and buffers digital serial data from BUSIN to LOOPOUT, and from LOOPIN to BUSOUT. However, if a fault condition is detected and the MAX5973 must disable its slave phase, then BUSIN is connected directly to BUSOUT and the signal at LOOPIN is ignored. See Figure 1.

A logic buffer (CLKIN to CLKOUT) is included in the MAX5973 to pass the switching frequency synchronization clock signal from the master to the slave. In the event of a slave failure, the buffer prevents the master clock signal from being corrupted. The clock signal output (CLKOUT) to a disabled slave goes low if the MAX5973 detects a fault condition.

BUSIN, LOOPIN, and CLKIN are CMOS inputs referred to the STBY input voltage. The BUSOUT, LOOPOUT, and CLKOUT output are CMOS outputs powered by the STBY voltage.

If the loop/bypass circuit and clock buffer are not used, BUSIN, LOOPIN, and CLKIN should be connected to ground, and BUSOUT, LOOPOUT, and CLKOUT should be left unconnected.

### Error Signal Buffers

The MAX5973 includes two unity-gain buffer amplifiers for the analog differential error signals that are sent in parallel to each phase. The buffer amplifiers prevent a failed phase controller from collapsing or distorting the analog error signals. The signals are received at ERRINA and ERRINB, and the buffered signals are output at ERROUTA and ERROUTB, respectively.

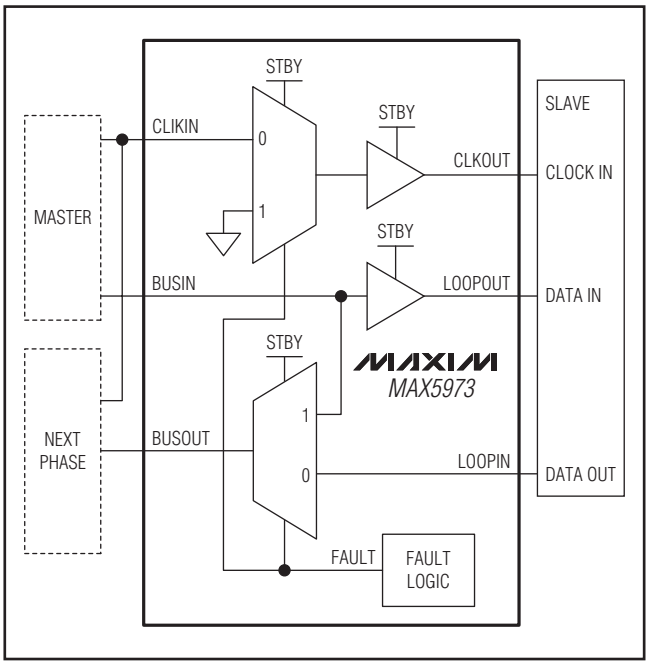


*Figure 1. Serial Loop/Bypass and Clock Buffer*



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## Applications Information

### Power Sequencing

The MAX5973 internal logic is powered from the STBY input. This supply should be established before the PWR and AUXIN supplies are brought up. A controlled restart can be performed by lowering the PWR and AUXIN supplies while STBY remains powered. After a fault condition has occurred, all supplies must be removed to unlatch the fault condition in the MAX5973 state machine.

Startup Sequence:

1) Establish $V_{STBY}$.
2) Establish $V_{PWR}$.
3) Establish $V_{AUXIN}$.

Normal Restart Sequence:

1) Remove $V_{AUXIN}$.
2) Remove $V_{PWR}$.
3) Establish $V_{PWR}$.
4) Establish $V_{AUXIN}$.

Unlatch from Fault Condition Sequence:

1) Remove $V_{AUXIN}$.
2) Remove $V_{PWR}$.
3) Remove $V_{STBY}$.
4) Repeat Startup Sequence.

### Transconductance Current-Sense Amplifier

The current-sense resistor, $R_{SENSE}$, must be connected between CBP and CBM to sense the average slave input current. The voltage drop across $R_{SENSE}$ should be less than or equal to 80mV, therefore $R_{SENSE}$ should be selected based on the following equation:

$$R_{SENSE} \times I_{SENSE,FS} \le 80mV$$

where $I_{SENSE,FS}$ is the full-scale slave input current. A Kelvin sense connection should be used to connect $R_{SENSE}$ to CBP and CBM. A capacitor between CBP and CBM can be used to help smooth the input current waveform. An inductive filter between the external FET and the slave high-side switch may be required to smooth the actual input current.

An output resistor, $R_{GMOUT}$, must be connected between the transconductance current-sense amplifier output GMOUT and AGND. The transconductance, $g_M$, is typically 10mA/V:

$$R_{GMOUT} \times g_M \times V_{SENSE,FS} \le 3V$$

### Circuit-Breaker Protection (CBSET)

The circuit-breaker threshold is programmed by connecting the resistor $R_{CBSET}$ between the high-side of $R_{SENSE}$ and CBSET.

$$R_{CBSET} = \frac{I_{SENSE,CB} \times R_{SENSE}}{20\mu A}$$

where $I_{SENSE,CB}$ is the desired circuit-breaker current limit. Remember to allow some margin between the maximum expected input current and the circuit-breaker limit to allow for normal load transients plus ripple and noise.

### Auxiliary Input OV Protection (AUXOV)

The output of a resistive divider supplied by AUXOUT is connected to AUXOV. An internal comparator compares the voltage at AUXOV and disables the internal switch and issues a fault if the voltage exceeds the 700mV threshold.

### High-Side Switch Failure (LXIN)

The high-side switch failure detection input LXIN monitors the average voltage at the switching node LX of the phase controller. The high-side switch failure threshold is set by an RC circuit and a Schottky diode. The Schottky diode D1 connected in parallel with $R_{LXIN1}$ is used to discharge the filter on every cycle of the DC-DC converter, allowing the MAX5973 to monitor each cycle for a high-side switch failure.

Begin by selecting a maximum failure detection time $t_{HIGH}$ that is larger than one switching period. The values of $R_{LXIN1}$ and $R_{LXIN2}$ should be chosen to keep $V_{LXIN}$ below its absolute maximum rating of 4V even when the input voltage is applied to LXIN continuously.

$$V_{IN} \times \left( \frac{R_{LXIN2}}{R_{LXIN1} + R_{LXIN2}} \right) < 4V$$

Diode D1 will discharge $C_{LXIN}$ to the Schottky $V_F$ voltage when Q3 is on. The MAX5973 will shut down the DC-DC converter when $V_{LXIN}$ = 700mV. During normal operation, capacitor $C_{LXIN}$ must not rise by 700mV - $V_F$. This can be achieved by sizing $C_{LXIN}$ and the charging current through $R_{LXIN1}$. The approximate average charging current with Q2 on and Q3 off is

$$I_{CLXIN,UP} = \frac{V_{IN} - \left( \frac{700mV - V_F}{2} \right)}{R_{LXIN1}} - \frac{(700mV - V_F)}{2 \times R_{LXIN2}}$$



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The value of capacitor $C_{LXIN}$ can then be chosen according to:

$$C_{LXIN} = \frac{I_{CLXIN,UP} \times t_{HIGH}}{700mV - V_F}$$

The values of $R_{LXIN1}$ and $R_{LXIN2}$ should also be chosen to minimize power dissipation:

$$P_{DISS} = \left( \frac{V_{IN}^2}{R_{LXIN1} + R_{LXIN2}} \right) \times D_{AVG}$$

where $D_{AVG}$ is the average duty cycle.

### Output Overvoltage Protection (OVIN)

The output of a resistive divider supplied by the combined multiphase output is connected to OVIN. An internal comparator compares the voltage at OVIN with either REFOUT or an external reference to determine if an overvoltage condition is present.

### Layout Considerations

Kelvin connections should be used for the nodes connecting CBP and CBM to $R_{SENSE}$, and the nodes connecting DOR and SOR to the ORing n-channel MOSFET.





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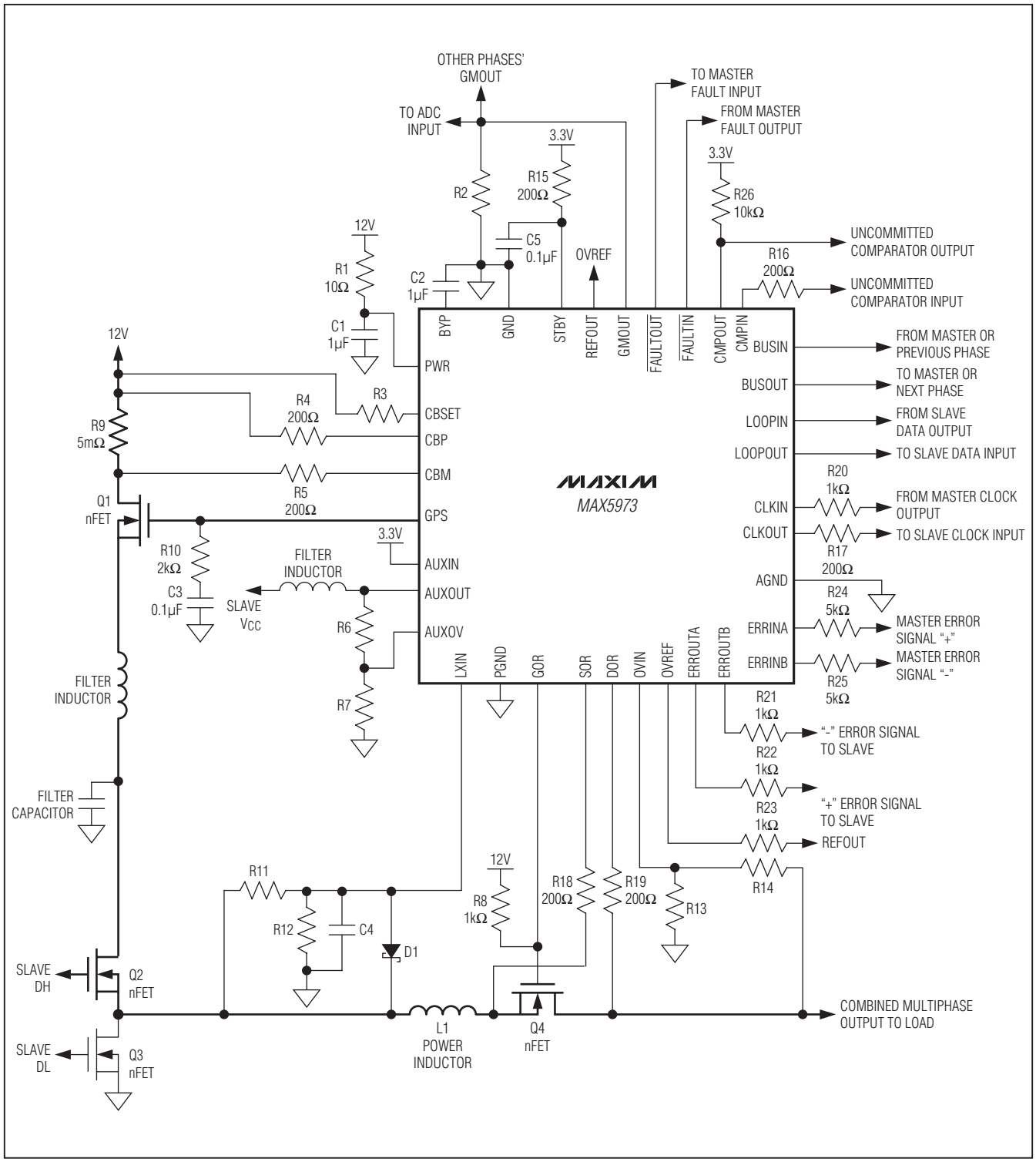
## Typical Application Circuit



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# Phase Redundancy Power Supervisor

## Chip Information

PROCESS: BiCMOS

## Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|---|---|---|
| 16 TQFN-EP | T1655+3 | 21-0140 |



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## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 4/10 | Initial release | — |

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