ES_LPC435x/3x/2x/1x

Errata sheet LPC435x/3x/2x/1x

Rev. 2 — 20 October 2012 **Errata sheet**

Document information

Info	Content
Keywords	LPC4357FET256; LPC4357JET256; LPC4357JBD208; LPC4353FET256; LPC4353JET256; LPC4353JBD208; LPC4337FET256; LPC4337JET256; LPC4337JBD144; LPC4337JET100; LPC4333FET256; LPC4333JET256; LPC4333JBD144; LPC4333JET100; LPC4327JBD144; LPC4327JET100; LPC4325JBD144; LPC4325JET100; LPC4323JBD144; LPC4323JET100; LPC4322JBD144; LPC4322JET100; LPC4317JBD144; LPC4317JET100; LPC4315JBD144; LPC4315JET100; LPC4313JBD144; LPC4313JET100; LPC4312JBD144; LPC4312JET100 errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

Revision history

Rev	Date	Description
2	20121020	• Added PWR.1, IRC.1. • Removed AES.1, ETM.1, RGU.1, SPIFI.1; documented in user manual. • Updated EEPROM.1, C_CAN.1, IBAT.1. • Added LPC432x and LPC431x parts. • Document title changed from ES_LPC4357_53_37_33 to ES_LPC435X_3X_2X_1X.
1.1	20120808	• Added RGU.1 and EEPROM.1. • Corrected C_CAN0/C_CAN1 peripheral assignment.
1	20120717	• Initial version.

Contact information

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1. Product identification

The LPC435x/3x/2x/1x devices (hereafter referred to as 'LPC43xx') typically have the following top-side marking:

LPC43xxxxxxxx

xxxxxxxx

xxxYYWWxR[x]

The last/second to last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC43xx:

Table 1. Device revision table

Revision identifier (R)	Revision description
'-'	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
C_CAN.1	Writes to CAN registers write through to other peripherals	'-'	Section 3.1
EEPROM.1	Limited EEPROM retention and endurance	'-' (with date code <1242)	Section 3.2
MCPWM.1	MCPWM abort pin not functional	'-'	Section 3.3
PMC.1	PMC.x power management controller fails to wake up from deep sleep, power down, or deep power down	'-'	Section 3.4

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Product version(s)	Detailed description
IBAT.1	VBAT supply current higher than expected	'-'	Section 4.1
IRC.1	IRC frequency variation higher than expected	'-'	Section 4.2
PWR.1	Higher than expected IO current	'-'	Section 4.3

Table 4. Errata notes table

Errata notes	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

3. Functional problems detail

3.1 C_CAN.1: Writes to CAN registers write through to other peripherals

Introduction:

Controller Area Network (CAN) is the definition of a high performance communication protocol for serial data communication. The C_CAN controller is designed to provide a full implementation of the CAN protocol according to the CAN Specification Version 2.0B. The C_CAN controller allows to build powerful local networks with low-cost multiplex wiring by supporting distributed real-time control with a very high level of security.

Problem:

On the LPC43xx, there is an issue with the C_CAN controller AHB bus address decoding that applies to both C_CAN controllers. It affects the C_CAN controllers when peripherals on the same bus are used. Writes to the ADC, DAC, I2C, and I2S peripherals can update registers in the C_CAN controller. Specifically, writes to I2C0, MCPWM, and I2S can affect C_CAN1. Writes to I2C1, DAC, ADC0, and ADC1 can affect C_CAN0. The spurious C_CAN controller writes will occur at the address offset written to the other peripherals on the same bus. For example, a write to ADC0 CR register which is at offset 0 in the ADC, will result in the same value being written to the C_CAN0 CNTL register which is at offset 0 in the C_CAN controller. Writes to the C_CAN controller will not affect other peripherals.

Work-around:

Workarounds include: Using a different C_CAN peripheral. Peripherals I2C1, DAC, ADC0, and ADC1 can be used at the same time as C_CAN1 is active without any interference. The I2C0, MCPWM, and I2S peripherals can be used at the same time as C_CAN0 is active without any interference. Another workaround is to gate the register clock to the CAN peripheral in the CCU. This will prevent any writes to other peripherals from taking effect in the CAN peripheral. However, gating the CAN clock will prevent the CAN peripheral from operating and transmitting or receiving messages. This workaround is most useful if your application is modal and can switch between different modes such as an I2S mode and a CAN mode. Another workaround is to avoid writes to the peripherals while CAN is active. For example, the ADC could be configured to sample continuously or when triggered by a timer, before the CAN is configured. Afterwards, C_CAN0 can be used since the ADC will operate without requiring additional writes.

3.2 EEPROM.1: Limited EEPROM retention and endurance

Introduction:

The LPC43xx contain a 16384 byte EEPROM memory with endurance of > 100 k erase / program cycles.

Problem:

On the LPC43xx LBGA parts with date code <1242, EEPROM endurance and retention may be less than specified. All newer parts will have fully tested EEPROMs.

Work-around:

Using longer EEPROM write times will increase retention.

3.3 MCPWM.1: MCPWM Abort pin is not functional

Introduction:

The Motor Control PWM engine is optimized for three-phase AC and DC motor control applications, but can be used in many other applications that need timing, counting, capture, and comparison. The MCPWM contains a global Abort input that can force all of the channels into a passive state and cause an interrupt.

Problem:

The MCPWM Abort input is not functional.

Work-around:

The MCPWM Abort function can be emulated in software with the use of a non-maskable interrupt combined with an interrupt handler that shuts down the PWM. This will result in a small delay on the order of 50 main clock cycles or about 1/3 of a microsecond at 150 MHz. Alternatively, the State Configurable Timer (SCT) can be configured to implement MCPWM functionality including an Abort input. The SCT can respond to external inputs in one clock cycle.

3.4 PMC.1: PMC.x power management controller fails to wake up from Deep Sleep, Power Down, or Deep Power Down

Introduction:

The PMC implements the control sequences to enable transitioning between different power modes and controls the power state of each peripheral. In addition, wake-up from any of the power-down modes based on hardware events is supported.

Problem:

When the chip is in a transition from active to Deep Sleep, Power Down, or Deep Power Down, wakeup events are not captured and they will block further wakeup events from propagating. The time window for this transition is 6 uS and is not affected by the chip clock speed. After a wakeup event is received during the PMC transition, the chip can only recover by using an external hardware reset or by cycling power.

Work-around:

Make sure that a wakeup signal is not received during the Deep Sleep, Power Down, or Deep Power Down transition period. An example circuit to work around this could include an external 6 uS one shot which could be triggered via software using a GPIO line when entering Deep Sleep, Power Down, or Deep Power Down mode. The one-shot's output could be used to gate the wakeup signal(s) to prevent receiving a wakeup signal during the PMC transition period. Depending on the system design, it may also be needed to latch the wakeup signal(s) so that they will still be present after the one-shot's 6 uS timeout.

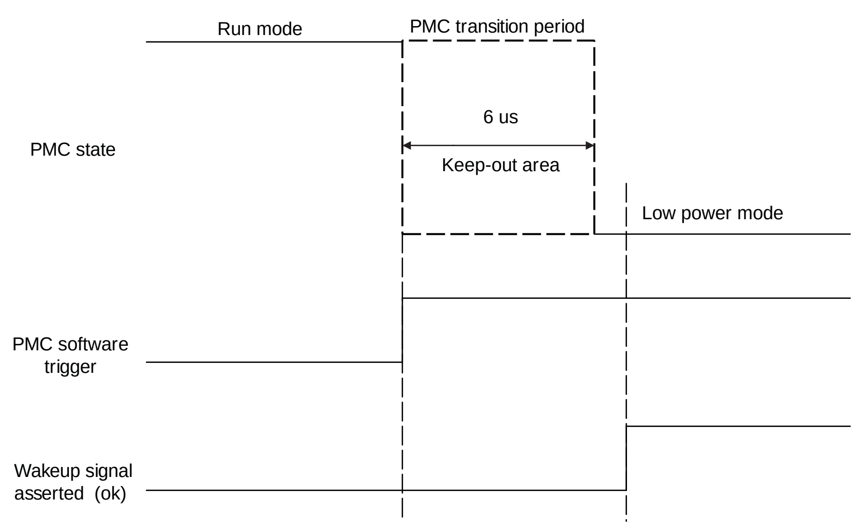

Fig 1. PMC wakeup keep-out area

4. AC/DC deviations detail

4.1 IBAT.1: VBAT supply current higher than expected

Introduction:

The LPC43xx contain a Real-Time Clock which measures the passage of time. The RTC has an ultra-low power design to support battery powered systems with a dedicated battery supply pin.

Problem:

On the LPC43xx, high current consumption of about 70 uA or higher may occur on the VBAT power supply pin due to current drain from the RTC_ALARM and SAMPLE pins.

On the LPC43xx, at temperatures lower than 0 °C, high current consumption up to 25 uA may occur on the VBAT power supply pin while VDD is present if VDD < VBAT. This is seen during Deep Sleep, Power Down, and Deep Power Down modes.

Work-around:

VBAT current consumption due to RTC_ALARM and SAMPLE pins can be lowered significantly by configuring the RTC_ALARM pin and SAMPLE pins as "Inactive" by setting the ALARMCTRL 7:6 field in CREG0 to 0x3 and the SAMPLECTRL 13:12 field in CREG0 to 0x3. These bits persist through power cycles and reset, as long as VBAT is present.

To work-around the current consumption at temperatures less than 0 °C, keep the VBAT voltage less than VDD. For example, use a 3.0 V VBAT voltage with a 3.3 V VDD supply. This also avoids current consumption during active mode which can occur when VBAT > VDD (see datasheet for details).

4.2 IRC.1: IRC frequency variation higher than expected

Introduction:

The IRC is used as the clock source for the WWDT and/or as the clock that drives the PLLs and the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

Problem:

On LPC43xx flash-based parts, the IRC currently has a non-linear behavior at high temperatures. This results in worse IRC accuracy than specified in the Data Sheet.

Work-around:

Many of the peripherals on these parts require use of an external crystal to meet timing accuracy even at the specified accuracy. The IRC is typically used during boot up and during UART and CAN In-Application Programming. It is recommended to avoid use of UART and CAN IAP at elevated temperatures to ensure accuracy.

Table 5. Errata sheet spec: ±2 %

T_{amb} = +55 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.76	12.00	12.24	MHz

Table 6. Errata sheet spec: ±3.5 %

T_{amb} = +85 °C to +105 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.58	12.00	12.42	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

4.3 PWR.1: Higher than expected IO current

Introduction:

The LPC43xx contain several low-power modes.

Problem:

On the LPC43xx, high current consumption of about 70 uA or higher may occur on the VDDIO power supply pin in the 256 BGA package.

Work-around:

In Deep Power Down mode the VDDREG, VDDA and VDDIO supplies can be powered off to reduce those supply currents to zero. In other modes no work-around is possible.

5. Errata notes detail

5.1 n/a

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7. Contents

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