Ordering number : ENA0137

SANYO Semiconductors
DATA SHEET

LC87F1364A

CMOS IC
FROM 64K byte, RAM 1K byte on-chip

8-bit 1-chip Microcontroller with Low-speed USB

Overview

The SANYO LC87F1364A is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 166ns, integrates on a single chip a number of hardware features such as 64K-byte flash ROM (onboard programmable), 1024-byte RAM, an on-chip debugger, a sophisticated 16-bit timers/counters (may be divided into 8-bit timers), 16-bit timers (may be divided into 8-bit timers or 8-bit PWMs), four 8-bit timers with a prescaler, a base timer serving as a time-of-day clock, a high-speed clock counter, a synchronous SIO interface (with automatic block transmit/receive function), an asynchronous/synchronous SIO interface, a UART interface (full duplex), a USB (Low-Speed) interface, two 12-bit PWM channels, an 8-bit 9-channel AD converter, and a 29-source 10-vector address interrupt feature.

Features

■Flash ROM
- Block-erasable in 128-byte units
- 65536 × 8 bits

■Minimum Bus Cycle Time
- 166ns (CF = 6MHz)

Note: The bus cycle time here refers to the ROM read speed.

■Minimum Instruction Cycle Time (tCYC)
- 500ns (CF = 6MHz)

* This product is licensed from Silicon Storage Technology, Inc. (USA), and manufactured and sold by SANYO Semiconductor Co., Ltd.

SANYO Semiconductor Co., Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

■Ports

- I/O ports
  Ports whose I/O direction can be designated in 1 bit units 9 (P1n, P70)
  Ports whose I/O direction can be designated in 4 bit units 8 (P0n)
- USB ports 2 (D+, D-)
- Dedicated oscillator ports 2 (XT1, XT2)
- Reset pins 1 ($\overline{RES}$)
- Power pins 1 ($V_{SS}1$, $V_{DD}1$)

■Timers

- Timer 0: 16-bit timer/counter with a capture register.
  Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture registers) × 2 channels
  Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture registers)
  + 8-bit counter (with an 8-bit capture register)
  Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
  Mode 3: 16-bit counter (with a 16-bit capture register)
- Timer 1: 16-bit timer that supports PWM/toggle output capabilities)
  Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) × 2 channels
  Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
  Mode 2: 16-bit timer with an 8-bit prescaler (with toggle output)
  (The lower-order 8 bits can be used as a timer with toggle output.)
  Mode 3: 16-bit timer with an 8-bit prescaler (with toggle output)
  (The lower-order 8 bits can be used as PWM.)
- Base timer
  1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
  2) Interrupts programmable in 5 different time schemes
- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler
- Timer 7: 8-bit timer with a 6-bit prescaler

■SIO

- SIO0: Synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3tCYC)
  3) Automatic continuous data transmission (1 to 256 bits)

- SIO1: 8-bit asynchronous/synchronous serial interface
  Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

■Full Duplex UART

- UART1
  1) Data length: 7/8/9 bits selectable
  2) Stop bits: 1 bit (2 bits in continuous transmission mode)
  3) Baud rate: 16/3 to 8192/3 tCYC

■AD Converter: 8 bits × 9 channels

■PWM: Multifrequency 12-bit PWM × 2 channels

■USB Controller
- USB Specification rev. 1.1 (Low-Speed) compatible
- Supports a maximum of 2 user-defined endpoints.

Endpoint		EP0	EP1	EP2
Transfer Type	Control	enable	enable	-
	Interrupt	-	enable	enable
Max. payload		8	8	8

■Watchdog Timer
- External RC watchdog timer
- Interrupt and reset signals selectable

■Interrupts
- 29 sources, 10 vector addresses

1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/USB bus active
4	0001BH	H or L	INT3/base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/USB bus reset/USB suspend/UART1 receive
8	0003BH	H or L	SIO1/USBERR/USBPOV/USBENP/USBNAK/ USBSTL/UART1 transmit
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/PWM0/PWM1/T4/T5

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels: 512 levels (the stack is allocated in RAM.)

■High-speed Multiplication/Division Instructions
- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation Circuits
- RC oscillation circuit (internal): For system clock
- CF oscillation circuit: For system clock, USB interface
- Crystal oscillation circuit: For system clock, time-of-day clock
- PLL circuit (internal): For system clock, USB interface

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) Canceled by a system reset or occurrence of an interrupt.
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The PLL base clock generator, CF, RC and crystal oscillators automatically stop operation.
  2) There are four ways of resetting the HOLD mode.
     (1) Setting the reset pin to the lower level.
     (2) Setting at least one of the INT0, INT1, and INT2 pins to the specified level
     (3) Having an interrupt source established at port 0
     (4) Having an bus active interrupt source established in the USB interface circuit
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  1) The PLL base clock generator, CF and RC oscillator automatically stop operation.
  2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  3) There are five ways of resetting the X'tal HOLD mode.
     (1) Setting the reset pin to the low level
     (2) Setting at least one of the INT0, INT1, and INT2 pins to the specified level
     (3) Having an interrupt source established at port 0
     (4) Having an interrupt source established in the base timer circuit
     (5) Having an bus active interrupt source established in the USB interface circuit

■Package Form

- MFP24S(300mil): Lead-free type

■Development Tools

- On-chip debugger: TCB87 type-A or TCB87 type-B + LC87F1364A

■Flash ROM Programming Boards

Package	Programming boards
MFP24S(300mil)	W87F5300M

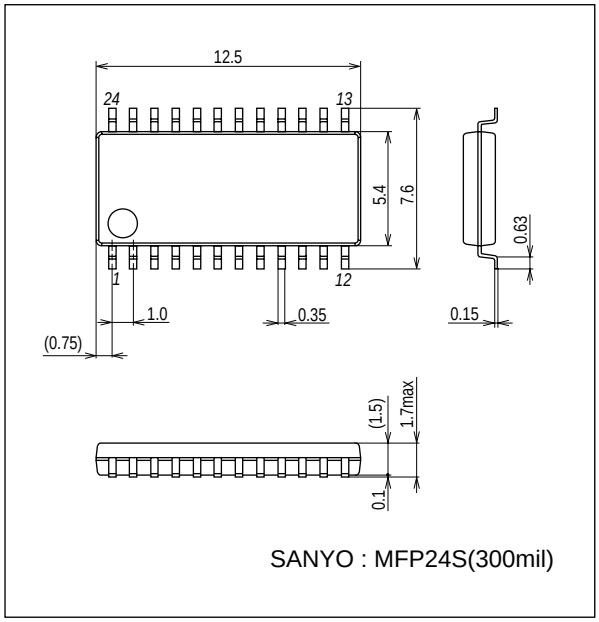
■Recommended EPROM Programmer

Maker	Model	Supported version	Device
Flash Support Group, Inc. (Single)	AF9708/AF9709/AF9709B (including product of Ando Electric Co.,Ltd)	After 02.40	LC87F1364A
SANYO	SKK(SANYO FWS)	Application Version: After 1.03 Chip Data Version: After 2.01	LC87F1364

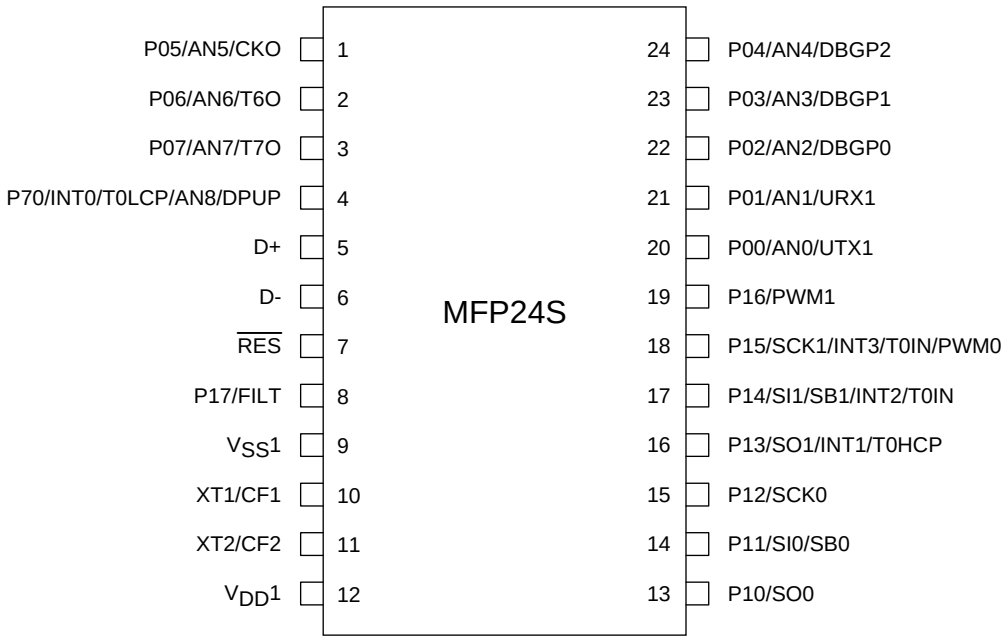
Package Dimensions

unit : mm (typ)

3112B



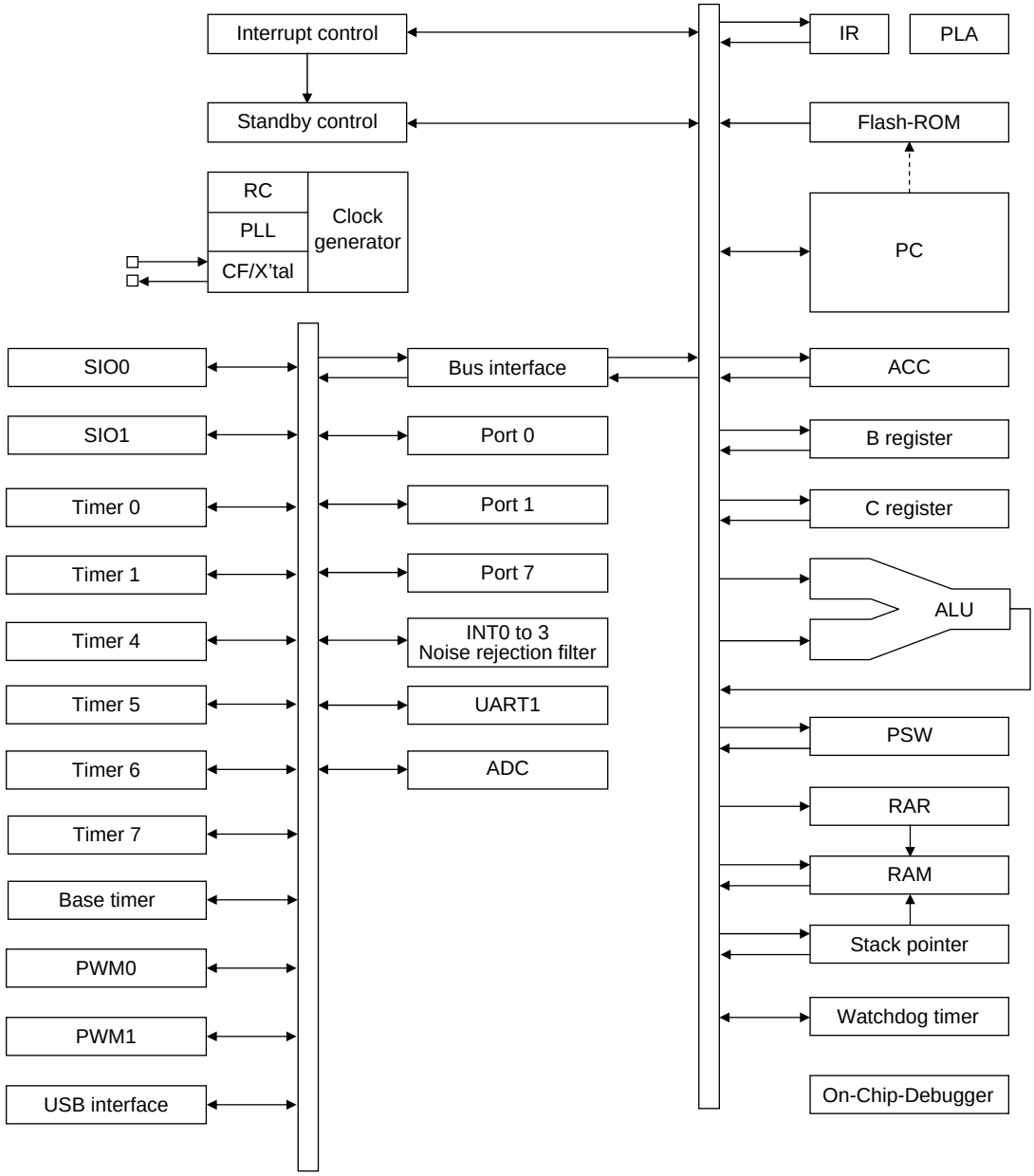
Pin Assignment



Top view

MFP	NAME
1	P05/AN5/CKO
2	P06/AN6/T6O
3	P07/AN7/T7O
4	P70/INT0/T0LCP/AN8/DPUP
5	D+
6	D-
7	$\overline{RES}$
8	P17/FILT
9	$V_{SS}1$
10	XT1/CF1
11	XT2/CF2
12	$V_{DD}1$
13	P10/SO0
14	P11/SI0/SB0
15	P12/SCK0
16	P13/SO1/INT1/T0HCP
17	P14/SI1/SB1/INT2/T0IN
18	P15/SCK1/INT3/T0IN/PWM0
19	P16/PWM1
20	P00/AN0/UTX1
21	P01/AN1/URX1
22	P02/AN2/DBGP0
23	P03/AN3/DBGP1
24	P04/AN4/DBGP2

System Block Diagram



Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$</td><td>-</td><td>- power supply pin</td><td>No</td></tr>
<tr><td>$V_{DD}1$</td><td>-</td><td>+ power supply pin</td><td>No</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 4 bit units
• Pull-up resistors can be turned on and off in 4 bit units.
• HOLD reset input
• Port 0 interrupt input
• Pin functions
P00: AN0 (ADC input)/UART1 transmit
P01: AN1 (ADC input)/UART1 receive
P02: AN2 (ADC input)/For On-Chip-Debugger
P03: AN3 (ADC input)/For On-Chip-Debugger
P04: AN4 (ADC input)/For On-Chip-Debugger
P05: AN5 (ADC input)/System Clock Output
P06: AN6 (ADC input)/timer 6 toggle outputs
P07: AN7 (ADC input)/timer 7 toggle outputs</td><td>Yes</td></tr>
<tr><td>Port 1
P10 to P17</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.
• Pin functions
P10: SIO0 data output
P11: SIO0 data input/bus I/O
P12: SIO0 clock I/O
P13: SIO1 data output/INT1 input/HOLD reset input/timer OH capture input
P14: SIO1 data input/bus I/O/INT2 input/ HOLD reset input/timer 0 event input/timer OL capture input
P15: SIO1 clock I/O/INT3 input (with noise filter)/timer 0 event input/timer OH capture input /PWM 0 output
P16: Timer 1 PWML output/PWM 1 output
P17: Timer 1 PWMH output/beeper output/Internal PLL filter pin
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 7
P70</td><td>I/O</td><td>• 1-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.
• Shared pins
P70: INT0 input/HOLD reset input/timer 0L capture input/watchdog timer output/AN8 (ADC input) / D- 1.5kΩ pull-up resistor connect pin
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
</table></td><td>No</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>Reset pin</td><td>No</td></tr>
<tr><td>XT1</td><td>I</td><td>Ceramic oscillator input pin/32.768kHz crystal oscillator input pin</td><td>No</td></tr>
<tr><td>XT2</td><td>I/O</td><td>Ceramic oscillator input pin/32.768kHz crystal oscillator output pin</td><td>No</td></tr>
<tr><td>D-</td><td>I/O</td><td>USB data I/O pin D-</td><td>No</td></tr>
<tr><td>D+</td><td>I/O</td><td>USB data I/O pin D+</td><td>No</td></tr>
</table>

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

Port Name	Option selected in units of	Option type	Output type	Pull-up resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
XT1	-	No	Input only	No
XT2	-	No	32.768kHz crystal oscillator output	No

Note 1: Programmable pull-up resistors for port 0 are controlled in 4 bit units (P00 to 03, P04 to 07).

USB Reference Power Option

When a voltage 4.5V to 5.5V is supplied to $V_{DD}1$ and the internal USB reference voltage circuit is activated, the H output level of the USB Port is 3.0V to 3.6V (the H output level of the ports except the USB Port is the $V_{DD}1$ voltage level, however). The active/inactive state of the reference voltage circuit can be determined by option settings.
According to the voltage to be supplied to $V_{DD}1$, make option settings as shown below.

$V_{DD}1$ voltage (V)		4.5 to 5.5			3.0 to 3.6
Option setting	USB Regulator	USE	USE	USE	NONUSE
	USB Regulator in HOLD mode	USE	NONUSE	NONUSE	NONUSE
	USB Regulator in HALT mode	USE	NONUSE	USE	NONUSE
Reference voltage circuit state	Normal state	active	active	active	inactive
	HOLD mode	active	inactive	inactive	inactive
	HALT mode	active	inactive	active	inactive
		(1)	(2)	(3)	(4)

- When the USB reference voltage circuit is made inactive, the H output level of the USB Port becomes the $V_{DD}1$ voltage level.
- Use the setting (2) or (3) to make the reference voltage circuit inactive in HOLD or HALT mode.
- When the reference voltage circuit is activated, the current drain increases by approximately 100μA compared with when the reference voltage circuit is inactive.

Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1$ = 0V

Parameter		Symbol	Pin/Remarks	Conditions		Specification			
					V_{DD}[V]	min	typ	max	unit
Maximum supply voltage		V_{DD} max	$V_{DD}1$	$V_{DD}1$		-0.3		+6.5	V
Input voltage		V_I(1)	XT1, XT2			-0.3		V_{DD}+0.3	
Input/output voltage		V_{IO}(1)	Ports 0, 1, 7			-0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1	• When CMOS output type is selected • Per 1 applicable pin		-10			mA
		IOPH(2)	PWM0, PWM1	Per 1 applicable pin		-20			
	Average output current (Note 2)	IOMH(1)	Ports 0, 1	• When CMOS output type is selected • Per 1 applicable pin		-7.5			
		IOMH(2)	PWM0, PWM1	Per 1 applicable pin		-15			
	Total output current	ΣIOAH(1)	Ports 0, 1 PWM0, PWM1 D+, D-	Total of all applicable pins		-50			
Low level output current	Peak output current	IOPL(1)	P00 to P05 Ports 1, P70 PWM0, PWM1	Per 1 applicable pin				20	
		IOPL(2)	P06, 07	Per 1 applicable pin				30	
	Average output current (Note 2)	IOML(1)	P00 to P05 Ports 1, P70 PWM0, PWM1	Per 1 applicable pin				15	
		IOML(2)	P06, 07	Per 1 applicable pin				20	
	Total output current	ΣIOAL(1)	Ports 0, 1, P70 PWM0, PWM1 D+, D-	Total of all applicable pins				75	
Allowable power Dissipation		Pd max	MFP24S	Ta=-20 to +70°C					mW
Operating ambient Temperature		Topr				-20		+70	°C
Storage ambient temperature		Tstg				-55		+125	

Note 2: The mean output current is a mean value measured over 100ms.

Allowable Operating Conditions at Ta = -20°C to +70°C, $V_{SS}1$ = 0V

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Operating supply voltage	$V_{DD}(1)$	$V_{DD}1$	0.490µs ≤ tCYC ≤ 200µs Except for onboard programming (Note 3)		2.5		5.5	V
	$V_{DD}(2)$		0.490µs ≤ tCYC ≤ 200µs internal PLL oscillation		4.5		5.5	
Memory sustaining supply voltage	VHD	$V_{DD}1$	RAM and register contents sustained in HOLD mode.		2.0		5.5	
High level input voltage	$V_{IH}(1)$	Port 1 P70 port input /interrupt side		2.5 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(2)$	Port 70 watchdog timer side		2.5 to 5.5	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(3)$	XT1, XT2, $\overline{RES}$		2.5 to 5.5	$0.75V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Port 1 P70 port input /interrupt side		4.0 to 5.5	V_{SS}		$0.1V_{DD}$ +0.4	
				2.5 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(2)$	Port 0		4.0 to 5.5	V_{SS}		$0.15V_{DD}$ +0.4	
				2.5 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(3)$	Port 70 watchdog timer side		2.5 to 5.5	V_{SS}		$0.8V_{DD}$ -1.0	
	$V_{IL}(4)$	XT1, XT2, $\overline{RES}$		2.5 to 5.5	V_{SS}		$0.25V_{DD}$	
Instruction cycle time (Note 4)	tCYC			2.5 to 5.5	0.490		200	µs
External system clock frequency	FEXCF(1)	XT1	• XT2 pin open • System clock frequency division ratio=1/1 • External system clock duty =50±5%	2.5 to 5.5	0.1		6	MHz
			• XT2 pin open • System clock frequency division ratio=1/2	2.5 to 5.5	0.1		12	
Oscillation frequency range (Note 5)	FmCF	XT1, XT2	6MHz ceramic oscillation See Fig. 1.	2.5 to 5.5		6		MHz
	FmRC		Internal RC oscillation	2.5 to 5.5	0.3	1.0	2.0	
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation See Fig. 2.	2.5 to 5.5		32.768		kHz

Note 3: V_{DD} must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

Note 4: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 5: See Tables 1 and 2 for the oscillation constants.

Electrical Characteristics at Ta = -20°C to +70°C, $V_{SS}1$ = 0V

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
High level input current	$I_{IH}(1)$	Ports 0, 1 Port 70 $\overline{RES}$	Output disabled Pull-up resistor off $V_{IN}=V_{DD}$ (Including output Tr's off leakage current)	2.5 to 5.5			1	μA
	$I_{IH}(2)$	XT1, XT2	$V_{IN}=V_{DD}$	2.5 to 5.5			1	
Low level input current	$I_{IL}(1)$	Ports 0, 1 Port 70 $\overline{RES}$	Output disabled Pull-up resistor off VIN=V_{SS} (Including output Tr's off leakage current)	2.5 to 5.5	-1			
	$I_{IL}(2)$	XT1, XT2	$V_{IN}=V_{SS}$	2.5 to 5.5	-1			
High level output voltage	$V_{OH}(1)$	Ports 0, 1	I_{OH}=-1mA	4.5 to 5.5	V_{DD}-1			V
	$V_{OH}(2)$		I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(3)$		I_{OH}=-0.2mA	2.5 to 5.5	V_{DD}-0.4			
	$V_{OH}(4)$	PWM0, PWM1 P05 (CK0 when using system clock output function)	I_{OH}=-10mA	4.5 to 5.5	V_{DD}-1.5			
	$V_{OH}(5)$		I_{OH}=-1.6mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(6)$		I_{OH}=-1mA	2.5 to 5.5	V_{DD}-0.4			
Low level output voltage	$V_{OL}(1)$	Ports 0, 1 Port 70 PWM0, PWM1	I_{OL}=10mA	4.5 to 5.5			1.5	
	$V_{OL}(2)$		I_{OL}=1.6mA	3.0 to 5.5			0.4	
	$V_{OL}(3)$		I_{OL}=1mA	2.5 to 5.5			0.4	
	$V_{OL}(4)$	P06, P07	I_{OL}=30mA	4.5 to 5.5			1.5	
	$V_{OL}(5)$		I_{OL}=5mA	3.0 to 5.5			0.4	
	$V_{OL}(6)$		I_{OL}=2.5mA	2.5 to 5.5			0.4	
Pull-up resistance	Rpu(1)	Ports 0, 1 Port 70	$V_{OH}=0.9V_{DD}$	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)			2.5 to 5.5	18	50	150	
Hysteresis voltage	VHYS	$\overline{RES}$ Port 1 Port 70		2.5 to 5.5		$0.1V_{DD}$		V
Pin capacitance	CP	All pins	For pins other than that under test: $V_{IN}=V_{SS}$ F=1MHz Ta=25°C	2.5 to 5.5		10		pF

Serial I/O Characteristics at Ta = -20°C to +70°C, $V_{SS}1$ = 0V

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin /Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	See Fig. 6.	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1a)		• Continuous data transmission/reception mode • USB is not in use simultaneous. • See Fig. 6. • (Note 4-1-2)		4			
			tSCKHA(1b)		• Continuous data transmission /reception mode • USB is in use simultaneous. • See Fig.6. • (Note 4-1-2)		7			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig.6.	2.7 to 5.5	4/3			tCYC
		Low level pulse width	tSCKL(2)				1/2			tSCK
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2a)		• Continuous data transmission /reception mode • USB is not in use simultaneous. • CMOS output selected • See Fig.6.		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC
			tSCKHA(2b)		• Continuous data transmission /reception mode • USB is in use simultaneous. • CMOS output selected • See Fig.6.		tSCKH(2) +2tCYC		tSCKH(2) +(19/3) tCYC	
Serial input	Data setup time		tsDI(1)	SB0(P11), SI0(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig.6.	2.7 to 5.5	0.03			µs
	Data hold time		thDI(1)			2.7 to 5.5	0.03			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transmission /reception mode • (Note 4-1-3)	2.7 to 5.5			(1/3)tCYC +0.05	
			tdD0(2)		• Synchronous 8-bit mode • (Note 4-1-3)	2.7 to 5.5			1tCYC +0.05	
	Output clock		tdD0(3)		(Note 4-1-3)	2.7 to 5.5			(1/3)tCYC +0.05	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SI0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig.6.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin /Remarks	CondiPtions	Specification				
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	See Fig.6.	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig.6.	2.7 to 5.5	2			tSCK
		Low level pulse width	tSCKL(4)					1/2		
		High level pulse width	tSCKH(4)					1/2		
Serial input	Data setup time		tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig.6.	2.7 to 5.5	0.03			µs
	Data hold time		thDI(2)			2.7 to 5.5	0.03			
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig.6.	2.7 to 5.5			(1/3)tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Pulse Input Conditions at Ta = -20°C to +70°C, $V_{SS}1$ = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
High/low level pulse width	tP1H(1) tP1L(1)	INT0(P70), INT1(P13), INT2(P14),	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	2.5 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P15) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.5 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P15) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.5 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P15) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.5 to 5.5	256			
	tPIL(5)	$\overline{RES}$	Resetting is enabled.	2.5 to 5.5	200			µs

AD Converter Characteristics at Ta = -20°C to +70°C, $V_{SS}1$ = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(P00) to AN7(P07), AN8(P70)		3.0 to 5.5		8		bit
Absolute accuracy	ET		(Note 6)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD		AD conversion time = 32×tCYC (when ADCR2=0) (Note 7)	4.5 to 5.5	15.68 (tCYC= 0.49µs)		97.92 (tCYC= 3.06µs)	µs
				3.0 to 5.5	31.36 (tCYC= 0.98µs)		97.92 (tCYC= 3.06µs)	
			AD conversion time = 64×tCYC (when ADCR2=1) (Note 7)	4.5 to 5.5	31.36 (tCYC= 0. 49µs)		97.92 (tCYC= 1.53µs)	
				3.0 to 5.5	31.36 (tCYC= 0. 49µs)		97.92 (tCYC= 1.53µs)	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	-1			

Note 6: The quantization error (±1/2LSB) is excluded from the absolute accuracy value.

Note 7: The conversion time refers to the interval from the time the instruction for starting the converter is issued till the time the complete digital value corresponding to the analog input value is loaded in the required register.

Consumption Current Characteristics at Ta = -20°C to +70°C, $V_{SS}1$ = 0V

Parameter	Symbol	Pin /Remarks	Conditions	V_{DD}[V]	Specification min	typ	Max	unit
Normal mode consumption current (Note 8)	IDDOP(1)	$V_{DD}1$	• FmCF=6MHz ceramic oscillation mode • System clock set to 6MHz side • Internal RC oscillation stopped • 1/1 frequency division ration	4.5 to 5.5		5.3	13	mA
	IDDOP(2)			2.5 to 4.5		3.5	9.6	
	IDDOP(3)		• FsX'tal=32.768kHz crystal oscillation mode • System clock set to PLL clock side • Internal RC oscillation stopped • 1/1 frequency division ration	4.5 to 5.5		6.7	17	
	IDDOP(4)		• FsX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • Internal PLL oscillation stopped • 1/2 frequency division ration	4.5 to 5.5		0.67	3.1	
	IDDOP(5)			2.5 to 4.5		0.43	2.3	
	IDDOP(6)		• FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped • Internal PLL oscillation stopped • 1/2 frequency division ration	4.5 to 5.5		120	380	µA
	IDDOP(7)			2.5 to 4.5		79	290	
HALT mode consumption current (Note 8)	IDDHALT(1)		• HALT mode • FmCF=6MHz ceramic scillation mode • System clock set to 6MHz side • Internal RC oscillation stopped • 1/1 frequency division ration	4.5 to 5.5		2.0	5.4	mA
	IDDHALT(2)			2.5 to 4.5		1.2	3.6	
	IDDHALT(3)		• HALT mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to PLL clock side • Internal RC oscillation stopped • 1/1 frequency division ration	4.5 to 5.5		3.6	9.6	
	IDDHALT(4)		• HALT mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • Internal PLL oscillation stopped • 1/2 frequency division ration	4.5 to 5.5		0.33	1.6	
	IDDHALT(5)			2.5 to 4.5		0.19	1.1	
	IDDHALT(6)		• HALT mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped • Internal PLL oscillation stopped • 1/2 frequency division ration	4.5 to 5.5		30	130	µA
	IDDHALT(7)			2.5 to 4.5		12	73	
HOLD mode consumption current	IDDHOLD(1)		HOLD mode • XT1=V_{DD} or open (External clock mode)	4.5 to 5.5		0.04	13	
	IDDHOLD(2)			2.5 to 4.5		0.02	9.8	
Timer HOLD mode consumption current	IDDHOLD(3)		Timer HOLD mode • FsX'tal=32.768kHz crystal oscillation mode	4.5 to 5.5		27	120	
	IDDHOLD(4)			2.5 to 4.5		9.6	66	

Note 8: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

USB Characteristics and Timing at Ta = -20°C to +70°C, $V_{SS}1$ = 0V

Parameter	Symbol	Conditions	Specification			
			min	typ	max	unit
High level output	$V_{OH(USB)}$	• 15kΩ±5% to GND	2.8		3.6	V
Low level output	V_{OL}	• 1.5kΩ±5% to 3.6V			0.3	V
Output signal crossover voltage	V_{CRS}		1.3		2.0	V
Differential input sensitivity	V_{DI}	• |(D+)-(D-)|	0.2			V
Differential input common mode range	V_{CM}		0.8		2.5	V
High level input	$V_{IH(USB)}$		2.0			V
Low level input	$V_{IL(USB)}$				0.8	V
USB data rise time	t_R		75		300	ns
USB data fall time	t_F		75		300	ns
Rise/fall time	t_{RFM}	• t_R/t_F	80		125	%

F-ROM Write Characteristics at Ta = +10°C to +55°C, $V_{SS}1$ = 0V

Parameter	Symbol	Pin	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	$V_{DD}1$	• 128-byte programming • Erasing current included	3.0 to 5.5		25	40	mA
Programming time	tFW(1)		• 128-byte programming • Erasing current included • Time for setting up 128-byte data excluded.	3.0 to 5.5		22.5	45	mS

Characteristics of a Sample External Clock Oscillation Circuit

Given below are the characteristics of a sample external clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample External Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf1 [Ω]	Rd1 [Ω]		typ [s]	max [s]	
32.768kHz	EPSON TOYOCOM	MC-306	22	22	Open	820k	2.5 to 5.5	1.3	3	Applicable CL value=12.5pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 4).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

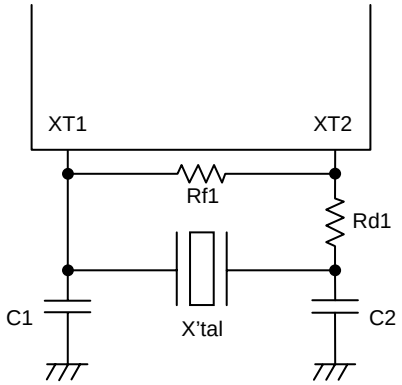


Figure 1 Crystal Oscillation Circuit

Table 2 Characteristics of a Sample External Clock Oscillator Circuit with a CF Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [ms]	max [ms]	
6MHz	MURATA	CSTCR6M00G15***-R0	(39)	(39)	Open	1k	2.5 to 5.5	0.1	0.5	Built in C3, C4

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit (see Figure 4).

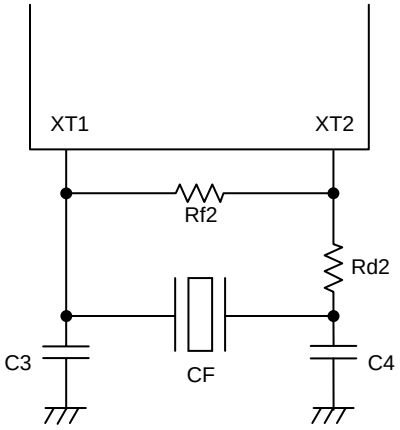


Figure 2 CF Oscillation Circuit

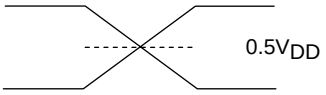
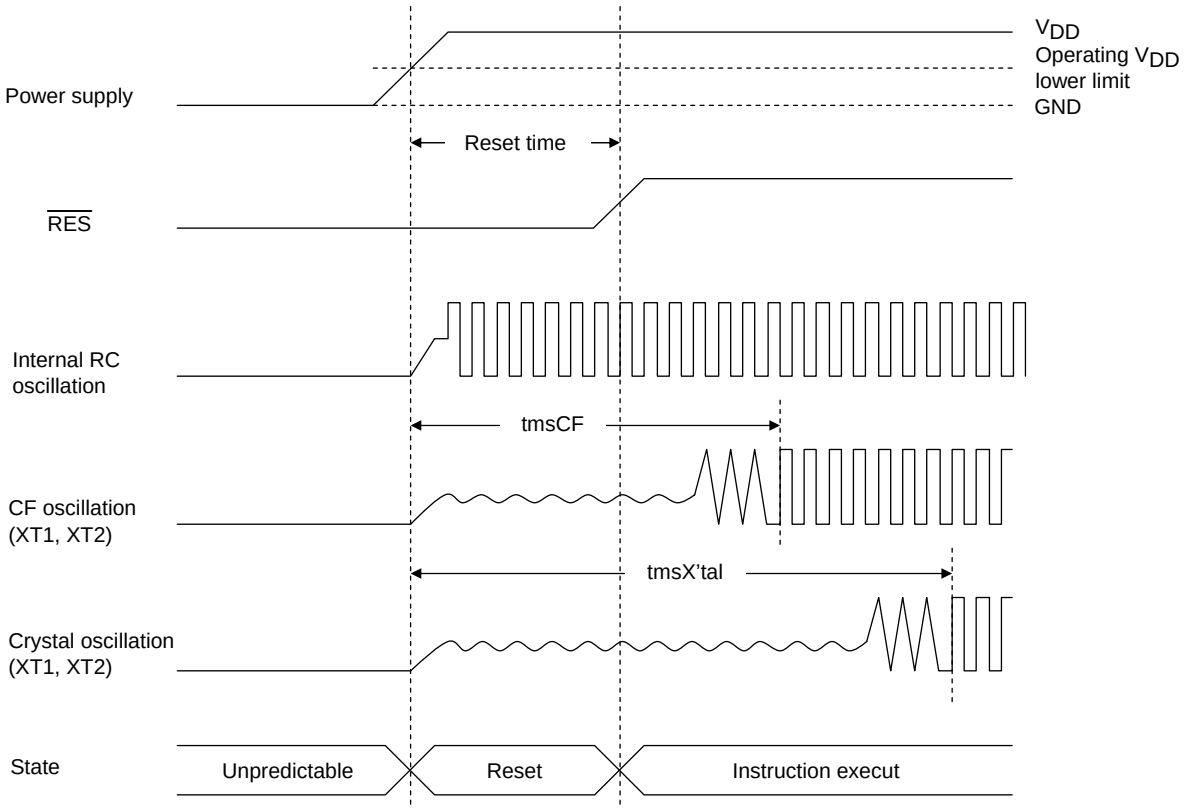
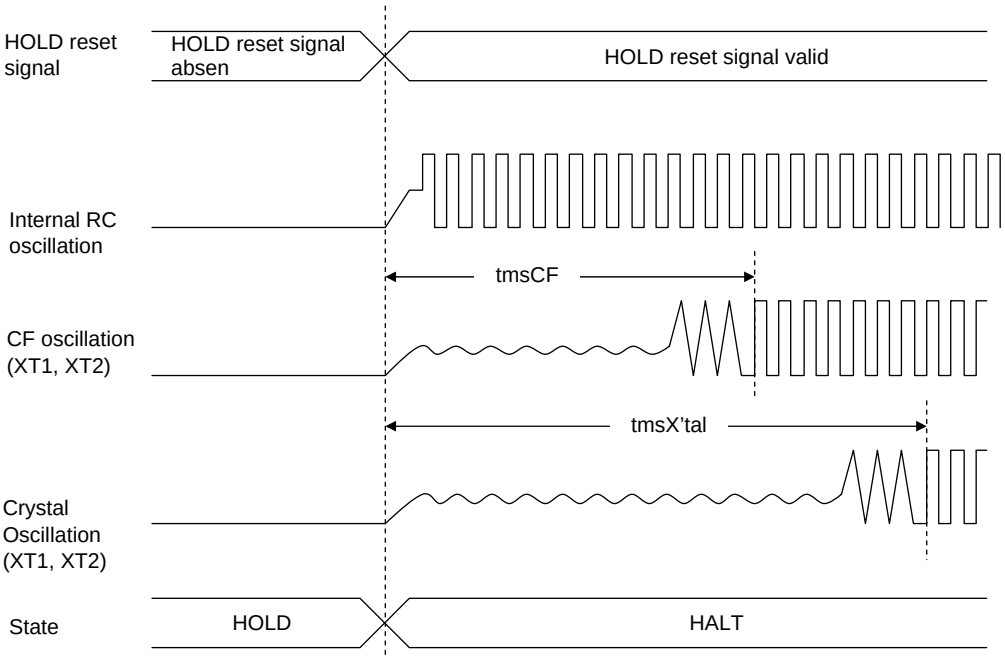


Figure 3 AC Timing Measurement Point

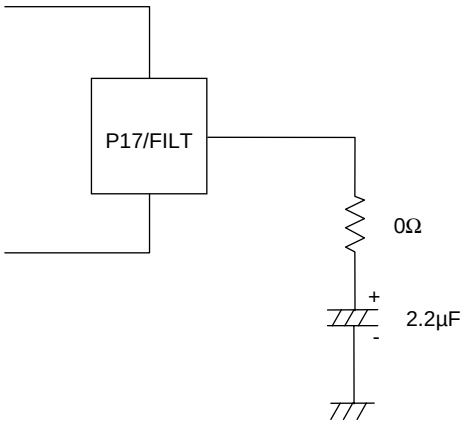


Reset Time and Oscillation Stabilization Time



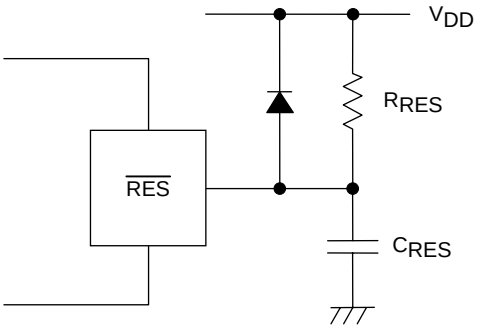
HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times



When using the internal PLL circuit to generate the 6MHz clock for USB or system clock, it is necessary to connect a filter circuit such as that shown to the left to the P17/FILT pin..

Figure 5 Filter Circuit for the Internal PLL Circuit



Note:
Determine the value of C_{RES} and R_{RES} so that the reset signal is present for a period of 200μs after the supply voltage goes beyond the lower limit of the IC's operating voltage.

Figure 6 Reset Circuit

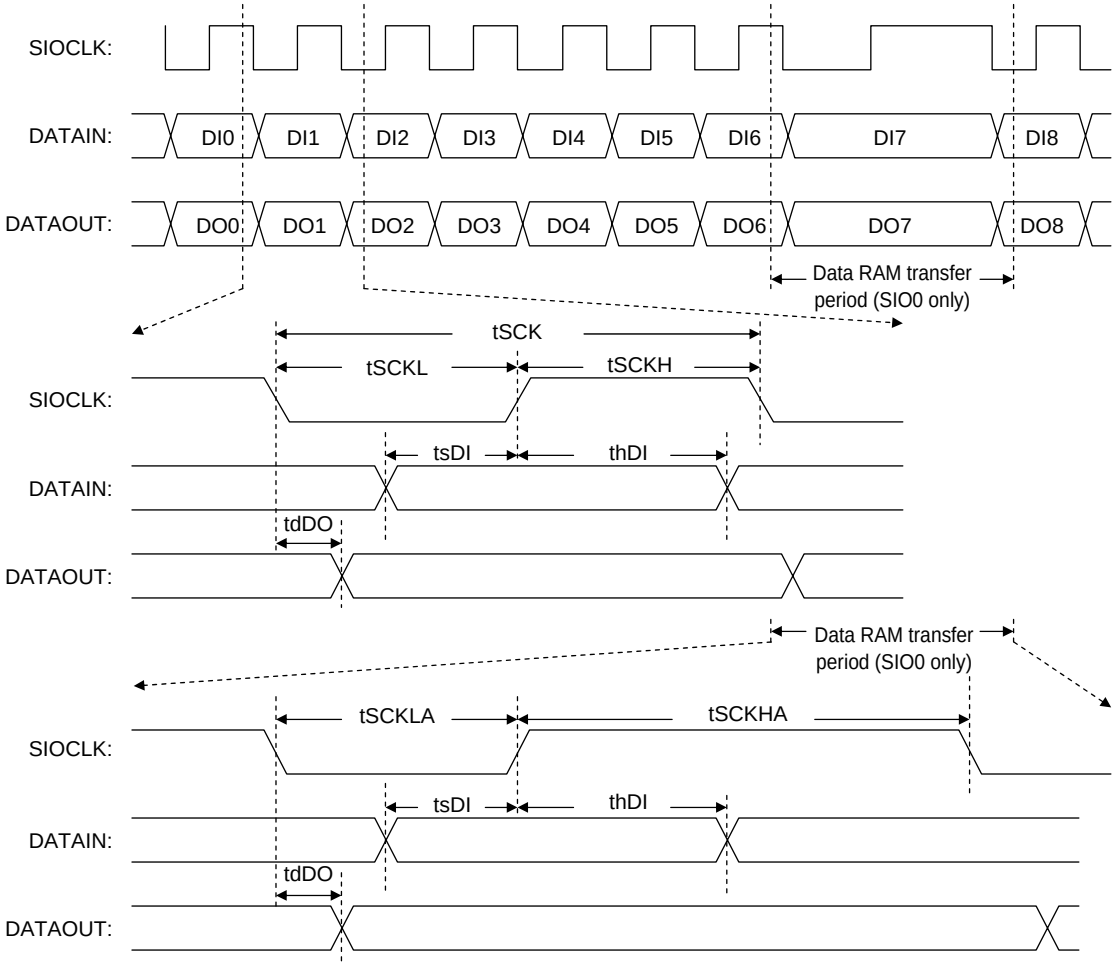


Figure 7 Serial Input/Output Waveforms

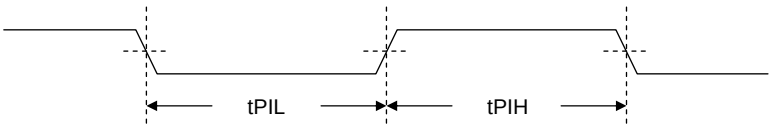


Figure 8 Pulse Input Timing Signal Waveform

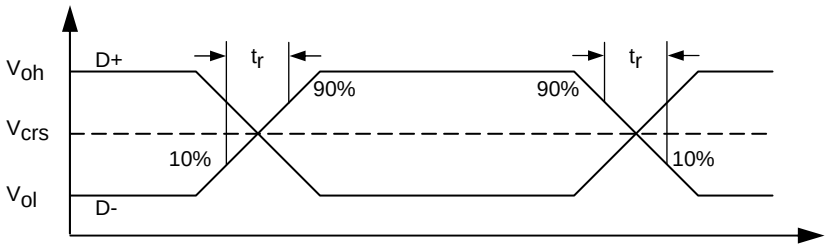


Figure 9 USB Data Signal Timing and Voltage Level