| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Package corrected to reflect a leaded chip carrier instead of a J leaded chip carrier. Corrected figure number sequence. | 93-07-13 | M. A. Frye |

| REV | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SHEET | | | | | | | | | | | | | | | | | | | |
| REV | A | A | A | A | A | A | A | A | | | | | | | | | | | |
| SHEET | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | | | | | | | | | | | |

| REV STATUS OF SHEETS | REV | A | A | A | A | A | | | A | A | A | A | A | A | A |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

PMIC N/A

**STANDARDIZED MILITARY DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
93-02-25

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

# MICROCIRCUIT, MEMORY, DIGITAL, CMOS, ELECTRICALLY ERASABLE PROGRAMMABLE LOGIC ARRAY, MONOLITHIC SILICON

| SIZE | CAGE CODE | 5962-93087 |
|---|---|---|
| A | 67268 | |

SHEET 1 OF 22

DESC FORM 193
JUL 91

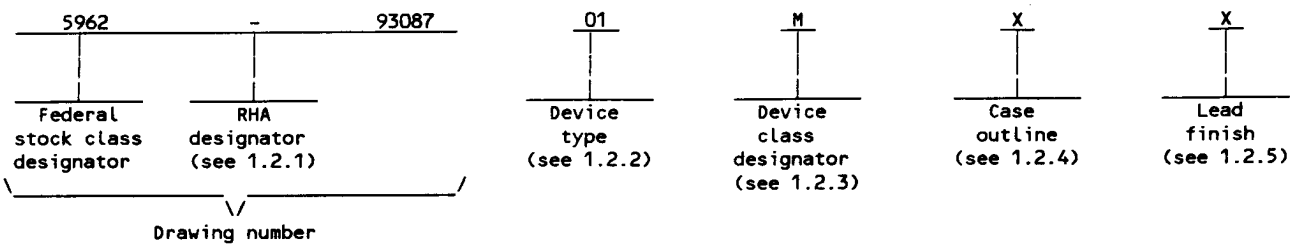
5962-E345-93

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:




1.2.1 RHA designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

| Device type | Generic number | Circuit function | Access time |
|---|---|---|---|
| 01 | 110 | EE CMOS 900-gate programmable array logic | 20 ns |

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level (see 6.6 herein) as follows:

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883 |
| B or S | Certification and qualification to MIL-M-38510 |
| Q or V | Certification and qualification to MIL-I-38535 |

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| X | see figure 1 | 44 | leaded chip carrier |

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

| | |
|---|---|
| Supply voltage range ($V_{CC}$) | -0.5 V dc to +7.0 V dc |
| Programming supply voltage range ($V_{PP}$) | -0.5 V dc to +9.50 V dc |
| DC input voltage range | -0.5 V dc to VCC +0.5 V dc |
| Power dissipation ($P_D$) | .935 W |
| Storage temperature range | -65°C to +150°C |
| Junction temperature ($T_J$) 2/ | +200°C |
| Thermal resistance, junction-to-case ($\theta_{JC}$): | |
| Case X | 20° C/W 3/ |
| DC supply current ($I_{CC}$ or $I_{SS}$) | 170 mA |
| DC output current ($I_O$) per pin | +25 mA |
| Endurance | 100 cycles (minimum) |
| Data retention | 20 years minimum |

1.4 Recommended operating conditions. 4/

| | |
|---|---|
| Supply voltage range ($V_{CC}$) | +4.5 V dc to +5.5 V dc |
| Minimum high level input voltage range ($V_{IH}$) | 2.0 V dc to $V_{CC}$ +0.5 V dc |
| Maximum low level input voltage range ($V_{IL}$) | 0.5 V dc to +0.8 V dc |
| Case operating temperature range ($T_C$) | -55°C to +125°C |
| Input rise time ($T_R$) | 50 ns maximum |
| Input fall time ($T_F$) | 50 ns maximum |
| Clock pins, rise time | 10 ns maximum |
| Clock pins, fall time | 10 ns maximum |

1.5 Digital logic testing for device classes Q and V.

| | |
|---|---|
| Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) | 5/ percent |

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARD

MILITARY

MIL-STD-480 - Configuration Control. Engineering changes, deviations & waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
3/ When a thermal resistance for this case is specified in MIL-STD-1835 that value shall supersede the value indicated herein.
4/ All voltage values in this drawing are with respect to $V_{SS}$.
5/ When a QML source exists, a value shall be provided.

BULLETIN

MILITARY

MIL-BUL-103- List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780- Standardized Military Drawings.

(Copies of the specifications, standards, and bulletin and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. This is a fully characterized military detail specification and is suitable for qualification of device classes B and S to the requirements of MIL-M-38510. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-M-38510) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M or the qualifying activity for classes B and S. The TRB will ascertain the requirements as provided by MIL-I-38535 for classes Q and V. Samples may be pulled any time after seal.

3.2.4 Block or logic diagram. The block or logic diagram shall be as specified on figure 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit will be provided when RHA product becomes available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 42 (see MIL-M-38510, appendix E).

3.11 Serialization for device classes S and V. All device class S devices shall be serialized in accordance with MIL-M-38510. Class V shall be serialized in accordance with MIL-I-38535.

3.12 Processing of EEPLDs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.12.1 Conditions of the supplied devices. Devices will be supplied in uncharged/neutral state. No provision will be made for supplying written devices.

3.12.2 Writing of EEPLDS. When specified, devices shall be written in accordance with the procedures and characteristics specified in 4.6.

3.12.3 Clearing of EEPLDs. When specified, devices shall be cleared in accordance with the procedures and characteristics specified in 4.7.

3.12.4 Verification of state of EEPLDs. When specified, devices shall be verified as either written to the specified pattern or cleared. As a minimum, verification shall consist of performing a read of the entire array to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure and the device shall be removed from the lot or sample.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the Device Manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Static burn-in for device class S (method 1015 of MIL-STD-883, test condition A).

(a) All inputs shall be connected to GND. Outputs may be open or connected to 4.5 V minimum. Resistors R1 are optional on both inputs and outputs, and required on outputs connected to $V_{CC}$ ±0.5 V. R1 = 220Ω to 47 kΩ. For static II burn-in, reverse all input connections (i.e., $V_{SS}$ to $V_{CC}$).

(b) $V_{CC}$ = 4.5 V minimum.

(c) Ambient temperature ($T_A$) shall be +125°C minimum.

(d) Test duration for the static test shall be 48 hours minimum. The 48-hour burn-in shall be broken into two sequences of 24 hours each (static I and static II) followed by interim electrical measurements.

(2) Dynamic burn-in for device classes M, B, and S (method 1015 of MIL-STD-883, test condition D) using the circuit submitted (see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

d. For classes S and B devices, post dynamic burn-in electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions<br>$4.5\ V < V_{CC} < 5.5\ V$ 1/<br>$-55°C < T_C < +125°C$<br>unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Low level output voltage | $V_{OL}$ | $I_{OL}$ = 12.0 mA, $V_{CC}$ = 4.5 V, $V_{IL}$ = 0.8 V, $V_{IH}$ = 2.0 V | 1,2,3 | 01 | | 0.5 | V |
| High level TTL output voltage | $V_{OH}$ | $I_{OL}$ = -2.0 mA, $V_{CC}$ = 4.5 V, $V_{IL}$ = 0.8 V, $V_{IH}$ = 2.0 V | 1,2,3 | 01 | 2.4 | | V |
| Input high leakage current | $I_{IH}$ | $V_I$ = 5.5 V, $V_{CC}$ = 5.5 V | 1,2,3 | 01 | | 10 | µA |
| Input low leakage current | $I_{IL}$ | $V_I$ = 0.0 V, $V_{CC}$ = 5.5. V | 1,2,3 | 01 | | -10 | µA |
| Off-state output leakage current high | $I_{OZH}$ | $V_O$ = 5.5 V, $V_{CC}$ = 5.5 V | 1,2,3 | 01 | | 40 | µA |
| Off-state output leakage current low | $I_{OZL}$ | $V_O$ = 0.0 V, $V_{CC}$ = 5.5 V | 1,2,3 | 01 | | -40 | µA |
| Output short circuit current 2/ 3/ | $I_{SC}$ | $V_{OUT}$ = 0.5 V, $V_{CC}$ = 5.0 V, $T_A$ = +25°C | 1,2,3 | 01 | -30 | -200 | mA |
| $V_{CC}$ standby current | $I_{CC2}$ | $V_{IN}$ = 0 V, $V_{CC}$ = 5.5 V, $I_{OUT}$ = 0 mA, f = 0 | 1,2,3 | 01 | | 170 | mA |
| Input capacitance 3/ | $C_{IN}$ | $V_{IN}$ = 2.0 V dc; f = 1.0 MHz<br>$T_A$ = +25°C<br>See 4.4.1e | 4 | 01 | | 8 | pF |
| Output capacitance 3/ | $C_{OUT}$ | $V_{OUT}$ = 2.0 V dc; f = 1.0 MHz<br>$T_A$ = +25°C<br>See 4.4.1e | 4 | 01 | | 9 | pF |
| Functional tests | | See 4.4.1c | 7,8A,8B | All | | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $4.5\ V < V_{CC} < 5.5\ V$ 1/ $-55°C < T_C < +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Input to nonregistered output | $t_{PD}$ | See figures 4 and 5 | 9,10,11 | 01 | | 20 | ns |
| Input to output enable 3/ | $t_{EA}$ | | 9,10,11 | 01 | | 20 | ns |
| Input to output disable 3/ | $t_{ER}$ | | 9,10,11 | 01 | | 20 | ns |
| Input setup time | $t_S$ D-type / T-type | | 9,10,11 | 01 | 13 / 15 | | ns |
| Input hold time | $t_H$ | | 9,10,11 | 01 | 0 | | ns |
| Clock width high | $t_{WH}$ | | 9,10,11 | 01 | 8 | | ns |
| Clock width low | $t_{WL}$ | | 9,10,11 | 01 | 8 | | ns |
| Clock to output delay | $t_{CO}$ | | 9,10,11 | 01 | | 12 | ns |
| Maximum frequency 4/ 5/ $1/(t_{WH} + t_{WL})$ | $f_{MAX}$ | | 9,10,11 | 01 | 62.5 | | MHz |
| Maximum external frequency $1/(t_S + tC_O)$ 6/ | $f_{EXT}$ D-type / T-type | | 9,10,11 | 01 | 40 / 37 | | MHz |
| Internal maximum frequency 7/ | $f_{INT}$ D-type / T-type | | 9,10,11 | 01 | 47.6 / 43.5 | | MHz |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $4.5\ V < V_{CC} < 5.5\ V$ 1/ $-55°C < T_C < +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Asynchronous reset width 3/ | $t_{ARW}$ | See figures 4 and 5 | 9,10,11 | 01 | 20 | | ns |
| Asynchronous reset recovery 3/ | $t_{ARR}$ | | 9,10,11 | 01 | 15 | | ns |
| Asynchronous reset to registered output | $t_{AR}$ | | 9,10,11 | 01 | | 25 | ns |
| Asynchronous preset to registered output | $t_{AP}$ | | 9,10,11 | 01 | | 25 | ns |
| Asynchronous preset width | $t_{APW}$ | | 9,10,11 | 01 | 20 | | ns |
| Asynchronous reset recovery | $t_{APR}$ | | 9,10,11 | 01 | 15 | | ns |

1/ All voltages referenced to ground $V_{SS}$.
2/ Not more than one output at a time should be shorted, and test duration should not exceed 1 second.
3/ Tested initially and after any design or process change that may affect this parameter and therefore shall be guaranteed to the limits specified in table I.
4/ $f_{MAX}$ represents the highest frequency for pipelined data.
5/ Not tested directly, but derived from testing $t_{WH}$ and $t_{WL}$.
6/ Not tested directly, but derived from testing $t_S + t_{CO}$.
7/ May not be tested directly, but shall be guaranteed to the limits specified in table I, by design.

e. An endurance test including a data retention bake, as specified in method 1033 of MIL-STD-883 prior to burn-in (e.g., may be performed at wafer sort) shall be included as part of the screening procedure, with the following condition:

(1) Cycling may be chip, block, byte or page at equipment room ambient and shall cycle all bytes a minimum of 100 cycles.

(2) After cycling, perform a high temperature unbiased storage 48 hours at +150°C minimum. The storage time may be accelerated by a higher temperature in accordance with the Arrenius relationship and with the apparent activation energy of .6 eV. The maximum storage temperature shall not exceed +200°C for assembled devices and +300°C for unassembled devices. All devices shall be programmed with a charge opposite the state that the cell would read in its equilibrium state (e.g., worst case pattern, see 3.12.2 herein).

(3) Read the data retention pattern and test using subgroups 1 and 7 (at the manufacturer's option high temperature equivalent subgroups 2, 8A, and 10 or low temperature equivalent subgroups 3, 8B, and 11 may be used in lieu of subgroups 1 and 7) after cycling and bake, but prior to burn-in. Devices having bits not in the proper state after storage shall constitute a device failure.

f. After the completion of all screening, the devices shall be erased and verified prior to delivery.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition, and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.2.3 Percent defective allowable (PDA).

a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.

b. The PDA for class B devices shall be in accordance with MIL-M-38510 for dynamic burn-in.

c. Static burn-in I and II failures shall be cumulative for determining PDA.

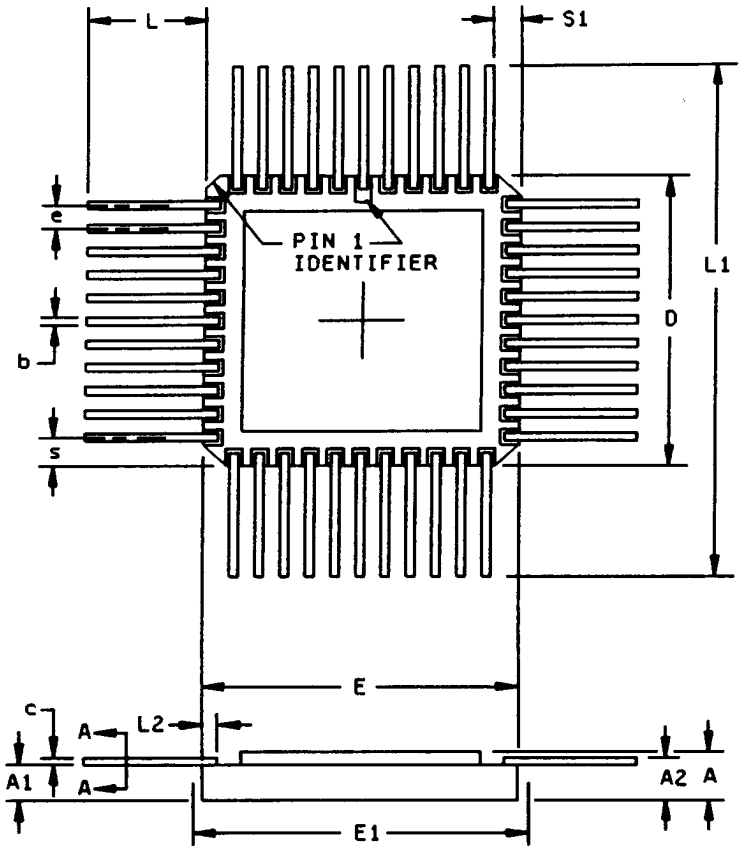
d. Those devices whose measured characteristics, after burn-in, exceed the specified delta ($\Delta$) limits or electrical parameter limits specified in table I, subgroup 1, are defective shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

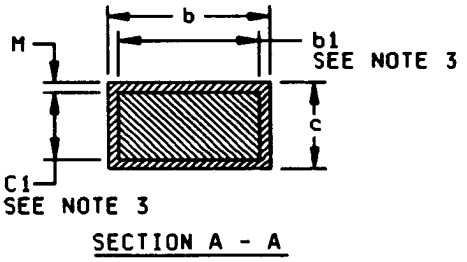
e. The PDA for device classes Q and V shall be in accordance with MIL-I-38535 for dynamic burn-in.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Qualification data for subgroups 7, 8A, and 8B shall be attributes only.

4.3.1.1 Qualification extensions for device class B and S. When authorized by the qualifying activity, if a manufacturer qualifies one device type which is identical (i.e., same die), to other device types on this specification, the slower device types may be part I qualified, upon the request of the manufacturer, without any further testing. The faster device types may be part I qualified by performing only group A qualification testing.




SECTION A - A

FIGURE 1. Case outline X.

| Symbol | Inches | | Millimeters | | Notes |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| A | .050 | .080 | 1.27 | 2.03 | |
| A1 | .044 | .064 | 1.12 | 1.63 | |
| A2 | .054 | .078 | 1.37 | 1.98 | |
| b | .013 | .023 | 1.52 | .58 | |
| b1 | .013 | .020 | 1.52 | .51 | 3 |
| c | .007 | .013 | .18 | .33 | |
| c1 | .007 | .010 | .18 | .25 | 3 |
| D | .638 | .662 | 16.21 | 16.81 | |
| E | .638 | .662 | 16.21 | 16.81 | |
| E1 | | .680 | | 17.27 | 2 |
| e | .045 | .055 | 1.14 | 1.40 | |
| L | .210 | .250 | 5.33 | 6.35 | |
| L1 | 1.062 | 1.158 | 26.97 | 29.41 | |
| L2 | .025 | | .64 | | |
| M | | .0015 | | .038 | 3 |
| S | | .085 | 2.16 | | |
| S1 | .056 | | 1.42 | | |

Notes:
1. An index mark, a notch, tab, or pin one identification mark shall be located within either of the areas shown
2. E1 allows for Ag or Cu alloy brazed overrun.
3. Dimensions b1 and c1 apply to base metal only. Dimension M applies to plating thickness.
4. All dimensions are given in inches.

FIGURE 1. Case outline X - Continued.

| Device type | 01 |
|---|---|
| Case outline | X |
| Terminal number | Terminal symbol |
| 1 | GND |
| 2 | I/O 0 |
| 3 | I/O 1 |
| 4 | I/O 2 |
| 5 | I/O 3 |
| 6 | I/O 4 |
| 7 | I/O 5 |
| 8 | I/O 6 |
| 9 | I/O 7 |
| 10 | $I_0$ |
| 11 | $I_1$ |
| 12 | GND |
| 13 | $I_2$/CKO |
| 14 | I/O 8 |
| 15 | I/O 9 |
| 16 | I/O 10 |
| 17 | I/O 11 |
| 18 | I/O 12 |
| 19 | I/O 13 |
| 20 | I/O 14 |
| 21 | I/O 15 |
| 22 | $V_{CC}$ |
| 23 | GND |
| 24 | I/O 16 |
| 25 | I/O 17 |
| 26 | I/O 18 |
| 27 | I/O 19 |
| 28 | I/O 20 |
| 29 | I/O 21 |
| 30 | I/O 22 |
| 31 | I/O 23 |
| 32 | $I_3$ |
| 33 | $I_4$ |
| 34 | GND |
| 35 | $I_5$/CK1 |
| 36 | I/O 24 |
| 37 | I/O 25 |
| 38 | I/O 26 |
| 39 | I/O 27 |
| 40 | I/O 28 |
| 41 | I/O 29 |
| 42 | I/O 30 |
| 43 | I/O 31 |
| 44 | $V_{CC}$ |

FIGURE 2. Terminal connections.

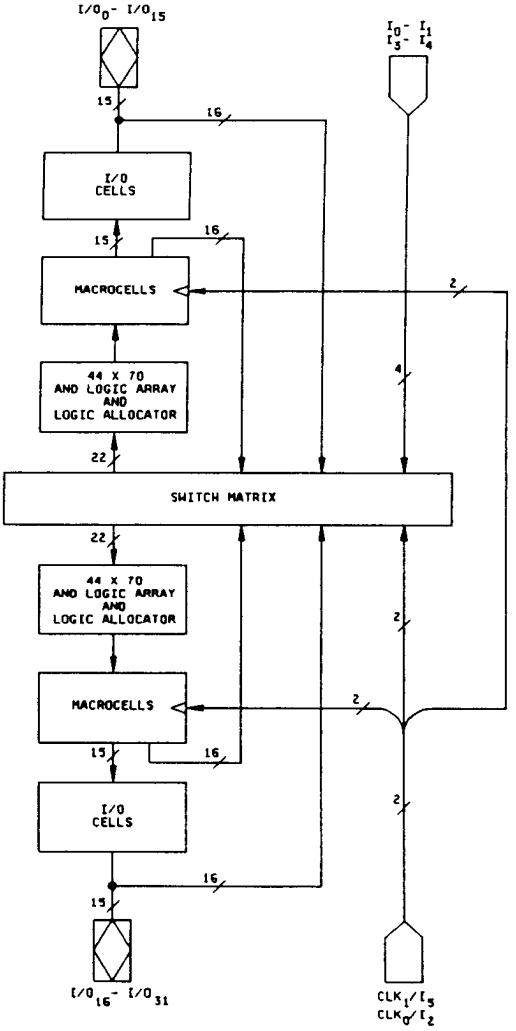
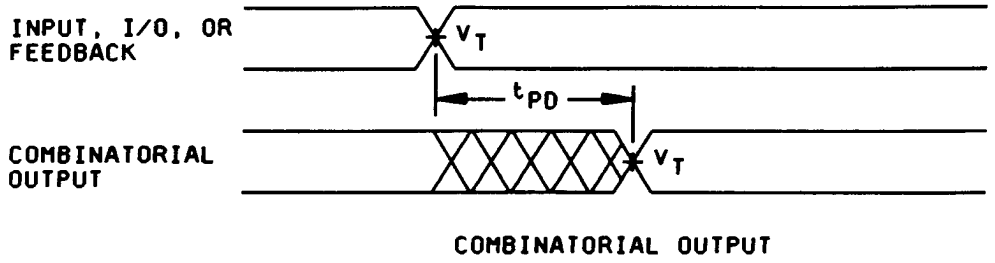
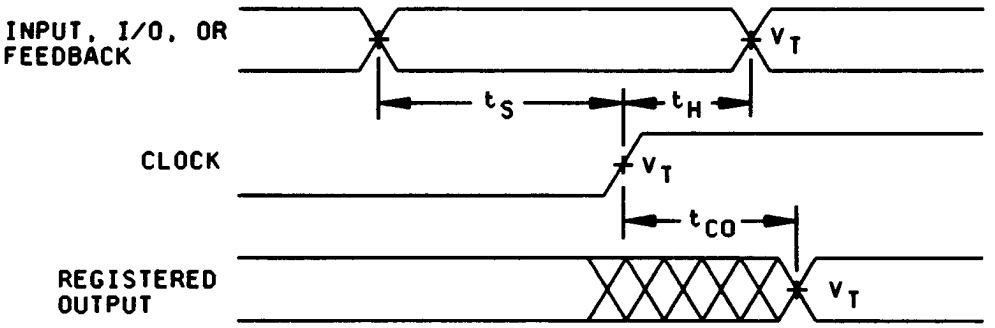



FIGURE 3. Block diagram.

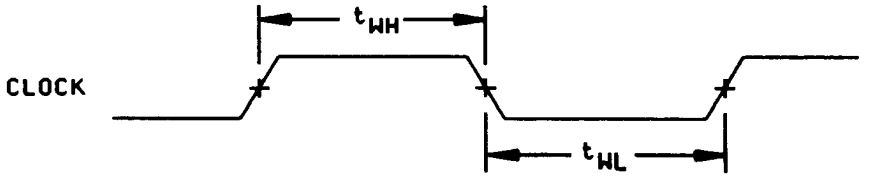
| | | | |
|---|---|---|---|
| STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444 | SIZE A | | 5962-93087 |
| | | REVISION LEVEL A | SHEET 14 |




COMBINATORIAL OUTPUT



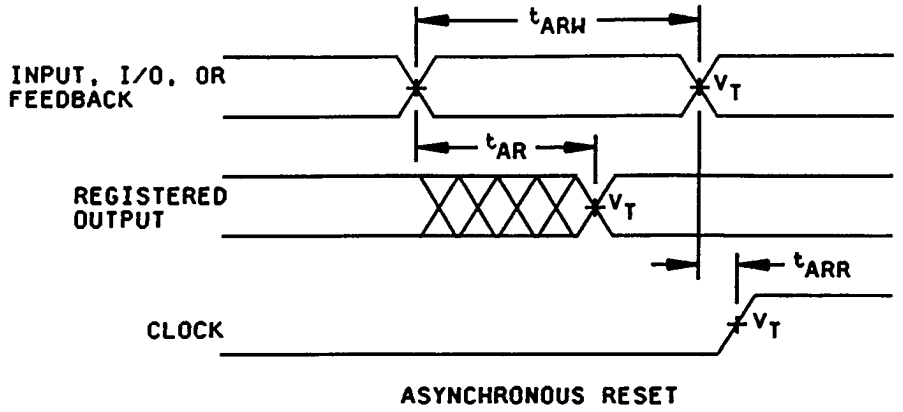

REGISTERED OUTPUT



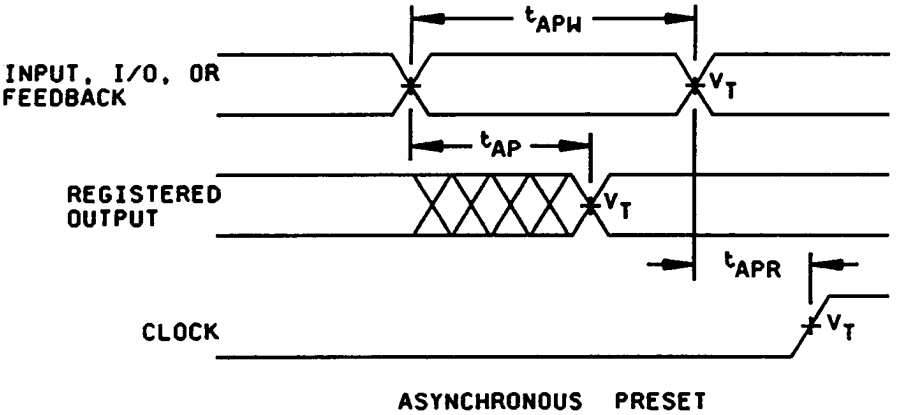

CLOCK WIDTH

NOTES:
1. $V_t$ = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2-4 ns

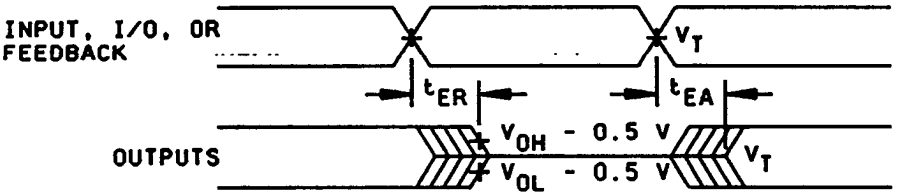
FIGURE 4. Timing waveforms.




ASYNCHRONOUS RESET



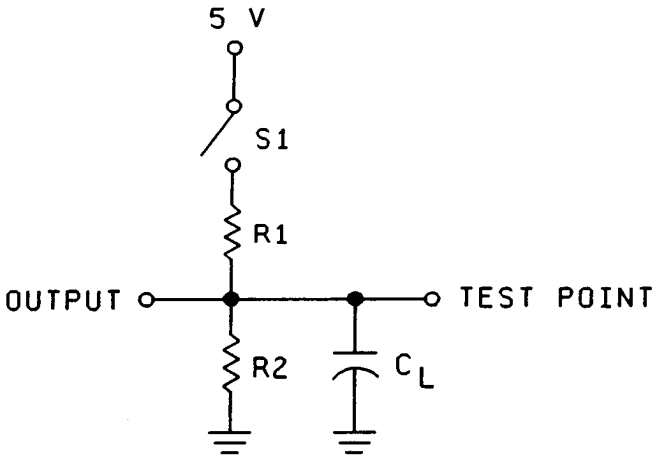

ASYNCHRONOUS PRESET




OUTPUT DISABLE/ENABLE

NOTES:
1. $V_t$ = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2-4 ns

FIGURE 4. Timing waveforms - Continued.




| Specification | $S_1$ | $C_L$ | $R_1$ | $R_2$ | Measured output value |
|---|---|---|---|---|---|
| All ac except $t_{PZX}$ and $t_{PXZ}$ | Closed | 35 pF | 390Ω | 750Ω | 1.5 V |
| $t_{PZX}$ | Z to H: open<br>Z to L: closed | 35 pF | 390Ω | 750Ω | 1.5 V |
| $t_{PXZ}$ | H to Z: open<br>L to Z: closed | 5 pF | 390Ω | 750Ω | H to Z: $V_{OH}$ - 0.5 V<br>L to Z: $V_{OL}$ + 0.5 V |

FIGURE 5. Switching test circuit.

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of Table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes B and S subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device as approved by the qualifying activity. For device classes Q and V subgroups 7 and 8 shall include verifying the functionality of the device, these tests shall have been fault graded per MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes B and S, the procedures and circuits shall be maintained under document revision control by the manufacturer and shall be made available to the qualifying activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's (TRB) in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC standard number 17 may be used for reference.

e. Subgroup 4 ($C_{IN}$ and $C_{OUT}$ measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is fifteen devices with no failures, and all input and output terminal tested.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

a. For device class S, steady-state life test shall be conducted using test condition D and the circuit described in 4.2.1b herein, or equivalent as approved by the qualifying activity.

b. For device class S only, end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 5 of group B inspections and shall consist of tests specified in table IIB herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. $T_A$ = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.4 Group D inspection. For group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device classes B, S, Q, and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.7 Erasing procedures. The erasing procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES
(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory).

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

| Line no. | Test requirements | Subgroups (in accordance with MIL-STD-883, method 5005 table I) | | | Subgroups (in accordance with MIL-I-38535, table III) | |
|---|---|---|---|---|---|---|
| | | Device class M | Device class B | Device class S | Device class Q | Device class V |
| 1 | Interim electrical parameters (see 4.2) | | 1,7,9 | 1,7,9 | 1,7,9 | 1,7,9 |
| 2 | Static burn-in I & II method 1015 | Not required | Not required | Required | Not Required | required |
| 3 | Same as line 1 | | | 1*,7* Δ | | 1*,7* Δ |
| 4 | Dynamic burn-in method | Required | Required | Required | Required | Required |
| 5 | Same as line 1 | | | 1*,7* Δ | | 1*,7* Δ |
| 6 | Final electrical parameters | 1*,2,3,7*,8A, 8B,9,10,11 | 1*,2,3,7*,8A, 8B,9,10,11 | 1*,2,3,7*,8A, 8B,9,10,11 | 1*,2,3,7*,8A, 8B,9,10,11 | 1*,2,3,7*,8A, 8B,9,10,11 |
| 7 | Group A test requirements | 1,2,3,4**,7 8A,8B,9,10,11 | 1,2,3,4**,7 8A,8B,9,10,11 | 1,2,3,4**,7 8A,8B,9,10,11 | 1,2,3,4**,7 8A,8B,9,10,11 | 1,2,3,4**,7 8A,8B,9,10,11 |
| 8 | Group B end-point electrical parameters | | | 1,2,3,7 8A,8B,9,10,11 Δ | | |
| 9 | Group C end-point electrical parameters | 2,3,7, 8A,8B | 1,2,3,7, 8A,8B Δ | | 1,2,3,7 8A,8B Δ | 1,2,3,7,8A, 8B,9,10,11 Δ |
| 10 | Group D end-point electrical parameters | 2,3, 8A,8B | 2,3, 8A,8B | 2,3, 8A,8B | 2,3, 8A,8B | 2,3, 8A,8B |
| 11 | Group E end-point electrical parameters | 1,7,9 | 1,7,9 | 1,7,9 | 1,7,9 | 1,7,9 |

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the functionality of the device.
4/ * indicates PDA applies to subgroups 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

| Test 1/ | Device types |
|---|---|
| | All |
| $I_{CC2}$, Standby | ±15 mA |
| $I_{IH}$ $I_{IL}$ | ±1 µA |
| $I_{OZH}$ $I_{OZL}$ | ±4 µA |

1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

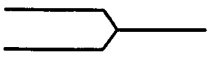
6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

$C_{IN}$ $C_{OUT}$ . . . . . Input and bidirectional output, terminal-to-GND capacitance
GND . . . . . Ground zero voltage potential
$I_{CC}$ . . . . . Supply current
$I_{IL}$ . . . . . Input current low
$I_{IH}$ . . . . . Input current high
$T_C$ . . . . . Case temperature
$T_A$ . . . . . Ambient temperature
$V_{CC}$ . . . . . Positive supply voltage
$V_{IC}$ . . . . . Positive Input Clamp Voltage
O/V . . . . . Latch-up over-voltage

6.5.1 Waveforms.

| Waveform symbol | Input | Output |
|---|---|---|
|  | MUST BE VALID | WILL BE VALID |
|  | CHANGE FROM H TO L | WILL CHANGE FROM H TO L |
|  | CHANGE FROM L TO H | WILL CHANGE FROM L TO H |
|  | DON'T CARE ANY CHANGE PERMITTED | CHANGING STATE UNKNOWN |
|  | | HIGH IMPEDANCE |

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN by establishing a one part number system covering all four documents, the OEM can procure to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

| Military document format | Example PIN under new system | Manufacturing source listing | Document Listing |
|---|---|---|---|
| New MIL-M-38510 Military Detail Specifications (in the SMD format) | 5962-XXXXXZZ(B or S)YY | QPL-38510 (Part 1 or 2) | MIL-BUL-103 |
| New MIL-H-38534 Standardized Military Drawings | 5962-XXXXXZZ(H or K)YY | QML-38534 | MIL-BUL-103 |
| New MIL-I-38535 Standardized Military Drawings | 5962-XXXXXZZ(Q or V)YY | QML-38535 | MIL-BUL-103 |
| New 1.2.1 of MIL-STD-883 Standardized Military Drawings | 5962-XXXXXZZ(M)YY | MIL-BUL-103 | MIL-BUL-103 |

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.