

# Features

- Burst Mode function
- Low startup current (4uA)
- Low operation current (1.7mA)
- Built in Leading edge blanking (LEB)
- Built in Synchronous slope compensation
- Current mode operates
- External programmable switching frequency
- Cycle by cycle Over Current Protection
- over temperature protection(OTP)
- Soft-start
- VDD over voltage protection and clamp
- under voltage lockout with hysteresis(UVLO)
- Driver Output clamped(13V)
- Soft-driver function for lower EMI
- Frequency jitter
- Constant output power limited
- Over load protection(OLP)
- Free audio noise operation

# Applications

Universal switch power supply and offline AC/DC flyback converter:

- Battery Charger
- Power Adaptor
- Set-Top Box Power Supplies

**Typical Application Circuit** 

Open-frame SMPS

# **General Description**

WS2259 which is optimized for high performance is a highly integrated current mode PWM control IC. It is applied for switch power of the small-sized and medium-sized for example the power adaptor. For lower the standby power and higher RoHS compliant, the IC has the Burst Mode function and very low startup current and working current. At the condition of no load or light load, the IC operates in extended 'burst mode' to minimize switching loss by lower the switching frequency. The low startup current and low operating current contribute to a reliable power on startup design with WS2259. A large value resistor could thus be used in the startup circuit to minimize the power consumption and improve the efficiency of the power convert.

The internal synchronous slope compensation circuit improves system large signal stability and reduces the possible subharmonic oscillation at high PWM duty cycle output. Leading-edge blanking on current sense(SENSE) input removes the signal glitch due to snubber circuit diode reverse recovery and thus greatly reduces the external component count and system cost in the design.

WS2259 offers complete protection coverage with automatic self-recovery feature including cycle by cycle over current protection (OCP), over load protection (OLP), over temperature protection (OTP), VDD Over Voltage Protection, under voltage lockout (UVLO). The gate-driven output is clamped to maximum 13V to protect the external MOSFET. Excellent EMI performance is achieved by using the frequency jitter and the soft-switching at the totem pole gate drive output. The tone energy at below 20KHZ is minimized in the design and audio noise is eliminated during operation. The IC can be used as the best alternative products of the linear power supply or the RCC-mode power to improve the whole performance of the switch power system and lower the cost. WS2259 is offered in SOT23-6, SOP-8 and DIP-8 packages.





## **Pin Definition and Device Marking**

WS2259 is offered in SOT23-6, SOP-8 and DIP-8 packages, as shown below:



## **Ordering Information**

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Package	IC Marking Information	Purchasing Device Name
8-Pin DIP8, Pb-free	WS2259DP	WS2259DP
8-Pin SOP8, Pb-free	WS2259SP	WS2259SP
6-Pin SOT23-6, Pb-free	59XXX	WS2259YP (SOT23-6)

# **Pin Function Description**

Pin Name	Pin No. DIP8/SOT23	Pin Type	Function Description
GATE	1/6	Output	Totem-pole gate drive output for the power MOSFET
VDD	2 / 5	Power	Power Supply
NC	3	Floating	Floating
SENSE	4 / 4	Current	Current sense input.
SENSE		Monitoring	
ы	5/2	Frequency	Internal oscillator frequency setting pin. A resistor which is
	575	Setting	connected between RI and GND sets the PWM frequency
NC	6	Floating	Floating
ED	7/0	Feedback	Feedback input pin. The PWM duty cycle is determined by voltage into
ГО	112	Input	this pin and the current-sense signal at Pin 4
GND	8 / 1	Ground	Ground

# **Block Diagram**

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## **Recommended Operating Condition**

Symbol	Parameter	Value	Unit
VDD	VDD Supply Voltage	10~30	V
RI	RI Resistor	100	Kohm
TA	Operating temperature	-20~85	°C

## Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Value	Unit
VDD	DC Power Supply	30	V
V <sub>FB</sub>	FB input voltage	-0.3~7	V
VSENSE	SENSE input voltage	-0.3~7	V
V <sub>RI</sub>	RI input voltage	-0.3~7	V
TJ	Operation Junction Temperature	-20~150	°C
T <sub>STG</sub>	Storage Temperature	-40~150	°C
V <sub>CV</sub>	Vcc Clamp Voltage	31	V
Icc	Vcc Clamp Continuous Current	10	mA

**Note 1**: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions section are not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

## **ESD Information**

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Symbol	Parameter	Value	Unit
Vesd-hbm	Human body model on all pins	3	KV
V <sub>ESD-MM</sub>	Machine model on all pins	300	V

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## Electrical Characteristics (T<sub>A</sub>=25°C, VCC=16V, if not otherwise noted)

Supply Voltage (VDD)							
Parameter	Symbol		Test condition	Min	Тур	Max	Unit
Operation voltage	VDD_OP					30	V
Turn on threshold Voltage	UVLO_ON			6.8	7.5	8	V
Turn-off threshold Voltage	UVLO_OFF			13.5	14.5	15.5	V
Start up current	I_VDD_ST		VDD=13V,RI=100K		4	10	uA
Operation Current			VDD=16V,RI=100K,V <sub>FB</sub> =3V		17	2.2	m۸
			GATE with 1nF to GND		1.7	2.3	ШA
	VDD_OVP				29		V
VDD Zener Clamp Voltage	VDD_Clamp		IVDD=10mA		31		V
Feedback Input Section							
V <sub>FB</sub> Open Loop Voltage	V <sub>FB</sub> Open		VDD=16V,FB open,	5.4	5.9	6.4	V
FB Pin Short Current	I <sub>FB</sub> _Short		FB Shorted to GND	0.3	0.45	5 0.6	mA
Power limiting FB Threshold	V <sub>TH</sub> _PL		VDD=16V, RI=100K	3.2	3.65	5 4.0	V
Power limiting Debounce	T <sub>D</sub> _PL		VDD=16V,FB open,RI=100KΩ	48	60	72	ms
Input Impedance	Z <sub>FB</sub> IN		VDD=16V,FB=2V/3V,CS open	11.5	14.5	5 18	kΩ
Maximum duty avala	Max Duty		VDD=16V,FB open,	72	77	02	0/
	Max_Duty		CS=0,RI=100KΩ	12		02	70
Current Sense Section							
Leading edge Blanking Time	TLEB				330		ns
OCP control delay	T <sub>D</sub> _OC		GATE with 1nF to GND		70		ns
OCP threshold T <sub>TH</sub> OC			FB=3.2V	0.68	0.78	0.78	V
Oscillator Section							
Frequency	Fosc	\	VDD=16V,RI=100K,,FB=3.2V	60	65	70	khz
	Jitter period	F	For 65K		4		ms
	Jitter range				±5		%
Burst mode frequency	Fosc_BM	``	VDD=9.5V,RI=100K, FB=1V		22		khz
Frequency variation versus temp. Deviation	∆f_temp	-	TEMP = -20 to 85℃		5		%
Frequency variation versus VDD	∆f_VDD	\	VDD = 12 to 25V		5		%
RI Section							
RI voltage	V <sub>RI</sub>	\	VDD=16V,RI=100KΩ,CS=1V	1.94	2	2.06	V
Thermal protection							
Thermal shutdown temperature	T_shutdown				150		°C
GATE Output Section							
Output voltage Low	VOL	VE	DD = 16V, lo = -20mA			0.8	V
Output voltage high	VOH	VD	DD = 16V, lo = 20mA	9			V
Output clamp voltage	VClamp	VE	DD = 20V	11	13	14.5	V
Rising time	Tr	VE	DD = 16V, GATE with 1nF to GND		250		ns
Falling time	Tf	VD	DD = 16V, GATE with 1nF to GND		75		ns

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# Typical Operating Characteristics

IVDD vs VDD

IVDD\_startup vs VDD



Temperature(°C)

Temperature('C)

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## **Function Description**

WS2259 is a highly integrated current mode PWM control IC which is optimized for high performance. It is applied for switch power of the small-sized and medium-sized for example the power adaptor. The low startup current, operation current and burst mode function at the condition of no load and low load can decrease the standby power of the system, and improve the power convert efficiency. The internal synchronous slope compensation, the leading edge blanking function of the Sense pin not only decrease the component number, but also improve the stability of the system and avoid the harmonics generation. WS2259 also have multiform general recovery protection mode. The main function is described as below.

#### Startup Current and Startup Control

Startup current of WS2259 is designed to be very low (4uA) so that VDD could be charged up above UVLO threshold level and starts up quickly. A large value startup resistor can therefore be used to minimize the power loss, predigest the design of startup circuit and provides reliable startup in application. For the design of AC/DC adaptor with universal input range, a startup resistor of 2 M $\Omega$ , 1/8 W could be used together with a VDD capacitor to provide a fast startup and low power dissipation solution.

#### **Operating Current**

The operating current of WS2259 is very low .Good efficiency is achieved with low operating current together with extended burst mode control circuit which can easy the design of VDD capacitor.

### Soft-start

As soon as VDD reaches UVLO(on), the soft-start function operates, the peak current is then gradually increased from zero. Every restart attempt is followed by 4ms soft-start.

#### **Burst Mode**

At very light load or no load condition, the IC operates in Burst Mode. In this condition, the voltage at FB is below burst mode threshold level, thus system goes into burst mode. The gate dive output switches only when VCC voltage drops below a preset level or FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss thus reduce the standby power consumption. The standby current of WS2259 is low as 800uA, Thus the standby of WS2259 can be low than 100mW. The frequency control also eliminates the audio noise at any loading conditions.

#### **Oscillator Operation**

A resistor connected between RI and GND sets the charge/discharge time of the constant current source to the internal cap and thus the PWM oscillator frequency is determined. The relationship between RI and switching frequency follows the below equation:

$$F_{OSC} = \frac{6500}{RI(Kohm)} (Khz)$$

If RI floating, the frequency will be internal set at 50 KHz

### **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in WS2259. The switch current is detected by a sense resistor into the SENSE pin. The internal Leading-edge blanking chops off the sense voltage spike at initial MOSFET on state due to snubber diode circuit reverse recovery and thus reduce the external RC filter circuit. The current limit comparator is disabled and cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by voltage level into SENSE pin and FB pin.

#### Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds slope voltage onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

## **Gate Driver**

GATE pin of WS2259 is connected to the gate of an external power switch. The gate drive strength which is too weak leads to over switch loss of MOSFET while too strong gate drive output compromises in the over EMI. A good tradeoff between output strength and dead time control is achieved through the design of the built-in totem pole gate in WS2259. The low standby dissipation and good EMI system design is easier to achieve through this dedicated devise. For MOSFET gate protection, an internal 13V clamp is added at higher than expected VCC input.

## **Protection Controls**

Good power supply system reliability is achieved with auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP), Under Voltage Lockout on VDD (UVLO), Over Temperature Protection (OTP), and VDD Over Voltage Protection & VDD clamp.

Internal line voltage compensation of OCP help to achieve constant output power limit over the universal input voltage range.



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# SOT23-6 Package Dimension



Symbol	Dimensions I	n Millimeters	Dimensions In Inches		
Symbol	Min	Мах	Min	Мах	
А	1.050	1.250	0.041	0.049	
A1	0.000	0.100	0.000	0.004	
A2	1.050	1.150	0.041	0.045	
d	0.300	0.400	0.012	0.016	
c	0.100	0.200	0.004	0.008	
D	2.820	3.020	0.111	0.119	
Е	1.500	1.700	0.059	0.067	
E1	2.650	2.950	0.104	0.116	
e	0.950	0.950TYP		7TYP	
e1	1.800	2.000	0.071	0.079	
L	0.700REF		0.028REF		
L1	0.300	0.600	0.012	0.024	
θ	0°	8°	0°	8°	



# **DIP-8 Package Dimension**



Ormhal	Dimensions I	n Millimeters	Dimensions In Inches		
Symbol	Min	Max	Min	Max	
А	3.710	4.310	0.146	0.170	
A1	0.510		0.020		
A2	3.200	3.600	0.126	0.142	
В	0.360	0.560	0.014	0.022	
B1	1.52	4(TYP)	0.060(TYP)		
С	0.204	0.360	0.008	0.014	
D	9.000	9.400	0.354	0.370	
E	6.200	6.600	0.244	0.260	
E1	7.620(TYP)		0.300(TYP)		
е	2.540(TYP)		0.100(TYP)		
L	3.000	3.600	0.118	0.142	
E2	8.200	9.400	0.323	0.370	

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# **SOP-8 Package Dimension**

