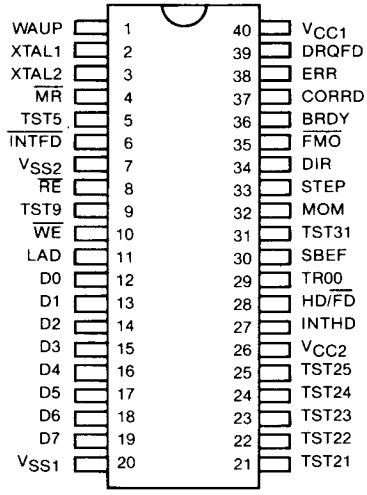
WD1015 Buffer Manager Control Processor

FEATURES

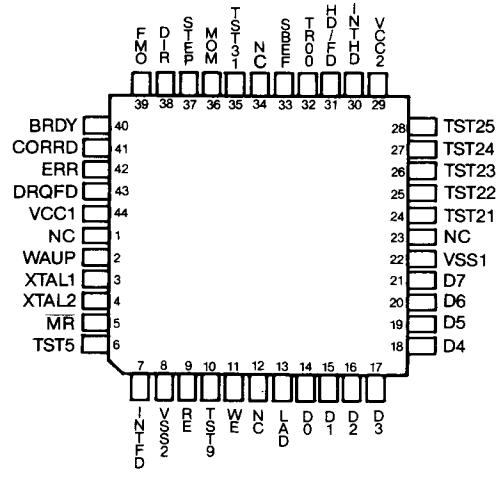
- SINGLE +5V POWER SUPPLY
- COMPLETE BUFFER MANAGER
- PROGRAMMABLE SECTOR SIZES - 128, 256, 512, or 1024 BYTES
- ECC BURST ERROR CORRECTION UP TO 5 BITS ON HARD DISK DATA
- 8-BIT MULTIPLEXED ADDRESS/DATA I/O BUS
- FLOPPY DISK COMMAND TRANSLATION
- SUPPORTS MOTOR ON OR HEAD LOAD DRIVES
- SUPPORTS 250 OR 500 KBS FLOPPIES
- BUFFERED SEEKS WITH FLOPPIES AND WINCHESTERS
- 16 POPULAR STEPPING RATES AVAILABLE
- AUTOMATIC RETRIES ON ALL ERRORS WITH SIMULATED COMPLETION
- POWER-ON DIAGNOSTICS INCLUDED
- 10 MHZ CLOCK RATE
- 40 PIN DIP PACKAGE
- 44 PIN QSM PACKAGE

DESCRIPTION

The WD1015 is a complete Control Processor (CP) that is used to handle all aspects of buffer management, in conjunction with the EDS (WD1014) device, for the Winchester/Floppy Controller board (WD1002-05). It executes all of the commands used by the WD1002-05 and does all of the control required except for real time processing, which is done by the WD1014. Throughout this specification this device will be referred to as the WD1015, or BMAC (buffer manager and controller), or simply as the CP (control processor). The WD1015 is programmed to control the transfer of information within the WFC and it maintains the necessary copies of the task files (TSF) found on both drives. Host access to the WFC causes the CP to access task file information in the TSF after a command is issued. Depending on the command, the CP will make the buffer accessible to the host or the WD1010 or 2797 controllers. The CP also controls the operation of the Error Correcting logic. During the transfer of data from the Host to the WD1010, the EDS monitors the data bus, if so enabled, to compute a 4 byte ECC which is appended to the data transferred to the WD1010 and recorded on the disk. During data transfers from the WD1010 to the host the CP uses the ECC to validate the data. If data is corrupted the CP envokes recovery techniques such as retries and correction. A maximum of 8 retries are attempted if two consecutive syndroms do not match. Correction is attempted only if two consecutive syndromes match. If the error is uncorrectable, the operation is terminated. The CP is also used to handle data transfers from or to the SF for the



PIN DESIGNATION



QSM DESIGNATION

floppy disk controller, which only uses CRC check bytes for its data fields. Two commands, RESTORE and SEEK, are directly executed by the CP rather than the WD2797 floppy disk controller. During status reads by the Host, the CP consolidates the normal completion status from the WD1010, the WD2797 and the current EDS status into a form consistant with established WD1010 error reporting. This consolidated status is then presented to the Host. The WD1015 is fabricated using HMOS technology and is available in a 40 pin DIP package and 44 pin QSM package.

PIN DESCRIPTION

PIN NUMBER	SIGNAL NAME	MNEMONIC	FUNCTION
1	WAKEUP	WAUP	This input is used by the BMAC to poll a command from the Host. The BUSY status bit is set immeditately execpt in case of a WRITE/FORMAT command. In that case, WAUP and BUSY, are set only after the sector buffer has been filled by the Host. WAUP is reset when the command has been executed.
2	CRYSTAL 1	XTAL1	One side of crystal input for internal oscillator. Also input for external source.
3	CRYSTAL 2	XTAL2	Other side of crystal/external source input. Frequency should be 10 MHz.
4	$\overline{\text{MASTER RESET}}$	$\overline{\text{MR}}$	This input is used to initialize the internal logic of the processor.
5	TEST 5	TST5	This input is to be left open by the user. Internal pull-up 300K ohm.
6	$\overline{\text{FLOPPY DISK INTERRUPT}}$	$\overline{\text{INTFD}}$	Initiates an interrupt if interrupt is enabled; disabled on reset.
7	V_{SS2}	V_{SS2}	This input is to be left open by the user. Internal pull-up 10M ohm.
8	READ ENABALE	$\overline{\text{RE}}$	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device.
9	$\overline{\text{TEST 9}}$	$\overline{\text{TST9}}$	This output is left open by the user.
10	$\overline{\text{WRITE}}$	$\overline{\text{WE}}$	Output strobe during a BUS write. Used as write strobe to an external device. Signifies that valid data has been put on the BUS.
11	ADDRESS LATCH	LAD	This output signal occurs once during each instruction cycle. The negative edge of LAD strobes address into an external latch, used to communicate to the WD1010, WD2797, and the WD1014 chips.
12-19	DATA BUS	D7-D0	True I/O bi-directional BUS which can be written to or read synchronously using $\overline{\text{RE}}$, $\overline{\text{WE}}$, strobes. Also contains the address and data during an external access to or from port devices, under control of LAD, $\overline{\text{RE}}$, and $\overline{\text{WE}}$.
20	GROUND	V_{SS1}	Ground.
21-25	TEST 21-25	TST21-25	Unused pins to be left open by the user.
26	V_{CC2}	V_{CC2}	+5V during operation.
27	HARD DISK INTERRUPT	INTHD	This input is polled to sense an interrupt from the WD1010, indicating completion of command issued to it by the BMAC.
28	$\overline{\text{HARD DISK/FLOPPY DISK}}$	HD/$\overline{\text{FD}}$	This input is used to sense hard disk operation when high, and floppy disk operation when low.
29	TRACK 00	TR00	This input indicates that the R/$\overline{\text{W}}$ heads of the selected floppy drive are positioned over the outermost cylinder.
30	SECTOR BUFFER EMPTY/FULL	SBEF	This input to the BMAC is set high whenever a sector of data has been written to or read from the Sector Buffer.
31	TEST 31	TST31	Normally left open by the user.

PIN DESCRIPTION (cont.)

PIN NUMBER	SIGNAL NAME	MNEMONIC	FUNCTION
32	MOTOR MODE	MOM	Input used to select motor-on or head load timings for floppies. This line should be left open for motor-on type drives such as the mini floppies. A delay of 1 second will be observed before $\overline{FMO}$ is activated. For head load type drives like the standard floppies, this input should be grounded. A delay of 40 mS, will be observed before $\overline{FMO}$ is activated, thereby improving the overall performance when accessing the floppies.
33	STEP	STEP	The STEP output is pulsed once for each cylinder to be stepped on the floppies. The step pulse period is normally determined by the stepping rate selected. On a RESTORE for the floppies, however, a stepping rate of 8 mS, is used if the specified stepping rate is faster than 8 mS.
34	DIRECTION	DIR	This output is used by the floppy drive to determine the direction of a seek operation. A low defines direction as out and a high specifies direction as in.
35	$\overline{FLOPPY\ MOTOR\text{-}ON}$	$\overline{FMO}$	This output is used to turn the motor on, on all floppy drives supported by the WD1002 WFC board. The drives must be configured such that the heads are loaded when this signal is activated. When the floppies are being accessed for the first time, a delay as determined by MOM, is observed before activating $\overline{FMO}$. Motor on is turned off after - 3 seconds, if no further floppy accesses are made.
36	BUFFER READY	BRDY	This output signal indicates the sector buffer is ready to be accessed by an external device such as the WD1010.
37	CORRECTED DATA	CORRD	This output status indicates to the Host that the BMAC has successfully corrected a data error in the data buffer, at least once. To determine if more than one correction has taken place during a multisector read, each sector specified must be reread by the Host on an individual basis.
38	ERROR	ERR	Output status bit indicates that the BMAC encountered an error during the execution of a command.The error reg, on the WFC board must be read by the Host to determine the type of error that occurred.
39	DATA REQUEST	DRQFD	This input indicates to the BMAC that the WD2797 has a byte of data available to be read from the disk, or requires a byte of data to be written to the floppy disk.
40	V_{CC1}	V_{CC1}	Main power supply. +5V ±5%