WINSEMI ®
MICROELECTRONICS

Logic Level
Bi-Directional Triode Thyristor

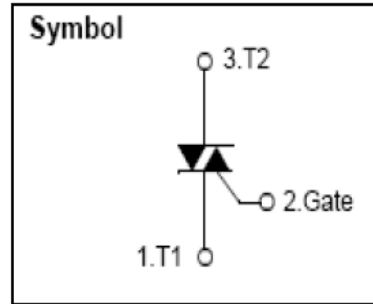## Features

■ Repetitive Peak off-State Voltage: 800V

■ R.M.S On-State Current($I_{T(RMS)}$)=1A

■ Low on-state voltage: V_{TM}=1.2(typ.)@ I_{TM}

■ Low reverse and forward blocking current:
  I_{DRM}=500uA@TC=125℃

■ Low holding current: I_H=4mA (typ.)

■ High Commutation dV/dt.

Symbol

General Description

General purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers,logic integrated circuits and other low power gate trigger circuits such as fan speed and temperature modulation control, lighting control and static switching relay.

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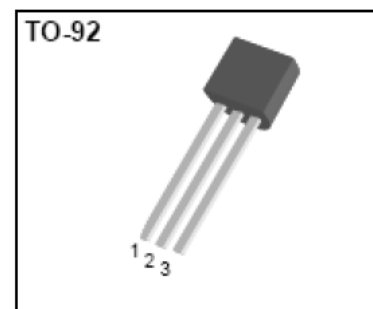
Absolute Maximum Ratings (T$_J$=25℃ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DRM}	Peak Repetitive Forward Blocking Voltage(gate open) (Note 1)	800	V
$T_{(RMS)}$	Forward Current RMS (All Conduction Angles, TL=50℃)	1	A
I_{TSM}	Peak Forward Surge Current, (full Cycle, Sine Wave, 50/60 Hz)	9.1/10	A
I^2t	Circuit Fusing Considerations (tp= 10 ms)	0.41	A^2s
P_{GM}	Peak Gate Power — Forward, (Tc = 58°C,Pulse with≤1.0us)	5	W
$P_{G(AV)}$	Average Gate Power — Forward, (Over any 20ms period)	0.1	W
dI/dt	Critical rate of rise of on-state current ITM = 1.5A; IG = 200mA; dIG/dt = 200mA/ms T$_J$=125℃	50	A/μs
I_{FGM}	Peak Gate Current — Forward, Tj = 125°C (20 μs, 120 PPS)	0.5	A
V_{RGM}	Peak Gate Voltage — Reverse, Tj = 125°C (20 μs, 120 PPS)	6	V
T_J,	Junction Temperature	-40 ~ 125	℃
T_{stg}	Storage Temperature	-40~150	℃
	mass	2	g

Note1: .Although not recommended, off-state voltages up to 800V may be applied without damage, but the TRIAC may
switch to the on-state. The rate of rise of current should not exceed 3A/us.

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
R_{QJC}	Thermal Resistance, Junction-to-Case	-	-	60	℃/W
R_{QJA}	ThermalResistance,Junction-to-Ambient	-	-	120	℃/W

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Electrical Characteristics (T$_J$ = 25°C unless otherwise specified)

Symbol	Characteristics		Min	Typ.	Max	Unit
I$_{DRM}$	Peak Forward or Reverse Blocking Current (V$_D$= V$_{DRM}$/V$_{RRM}$,gate open)	T$_J$=25℃	-	-	5	μA
		T$_J$=125℃	-	-	500	
V$_{TM}$	Forward "On" Voltage (ITM = 1.5 A) (Note2)		-	1.2	1.5	V
I$_{GT}$	Gate Trigger Current (Continuous dc) (V$_D$ = 12 Vdc, R$_L$ = 33 Ω)	T2+G+	-	0.4	5	mA
		T2+G-	-	1.3	5	
		T2-G-	-	1.4	5	
		T2-G+	-	3.8	7	
V$_{GT}$	Gate Trigger Voltage (Continuous dc) (V$_D$ =12 Vdc, R$_L$ = 33 Ω)	T2+G+	-	-	1.2	V
		T2+G-	-	-	1.2	
		T2- G-	-	-	1.2	
		T2-G+	-	-	1.5	
V$_{GD}$	Gate threshold voltage(T$_J$=125℃ , V$_D$=V$_{DRM}$,R$_L$=3.3KΩ)		0.2	-	-	V
dV/dt	Critical rate of rise of commutation Voltage (V$_D$=0.67V$_{DRM}$,gate open)		10	20	-	V/μs
I$_H$	Holding Current (V$_D$ =12 V, I$_{GT}$ = 100 mA)		-	1.3	5	mA
I$_L$	latching current (V$_D$ = 12 V; I$_{GT}$ = 100 mA)	T2+G+	-	1.2	5	mA
		T2+G-	-	4.0	8	
		T2-G-	-	1.0	5	
		T2-G+	-	2.5	8	
R$_d$	Dynamic resistance (T$_J$=125℃)		-	-	420	mΩ

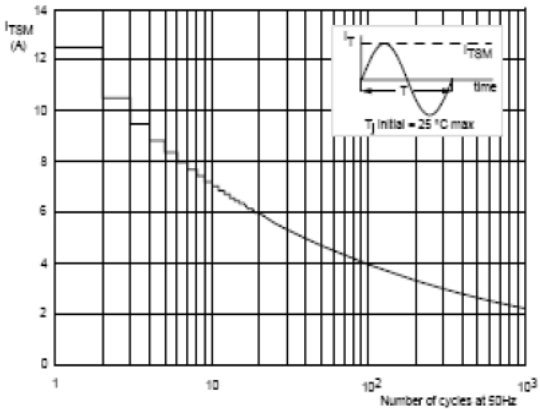Note 2. Forward current applied for 1 ms maximum duration, duty cycle

Fig.1 Maximum permissible non-repetitive
Peak on-state current I_{TSM} versus number of
Cycles,for sinusoidal currents,f=50Hz.

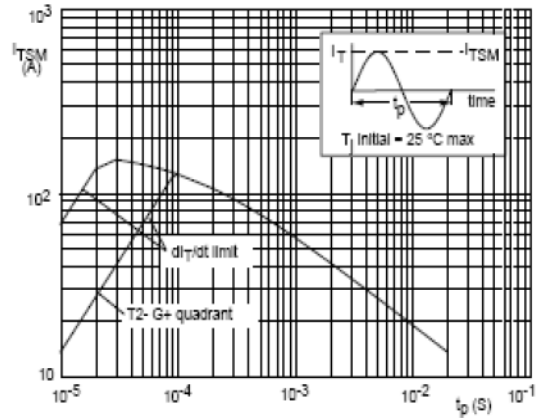Fig.2 Maximum permissible non-repetitive
Peak on-state current I_{TSM},versus pulse
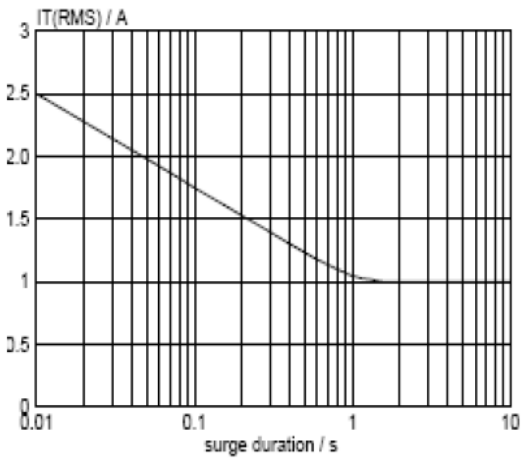width t_p for sinusoidal currents,$t_p{\leq}20ms$

Fig.3 Maximum permissible repetitive rms
On-state current $I_{T(RMS)}$,versus surge duration,
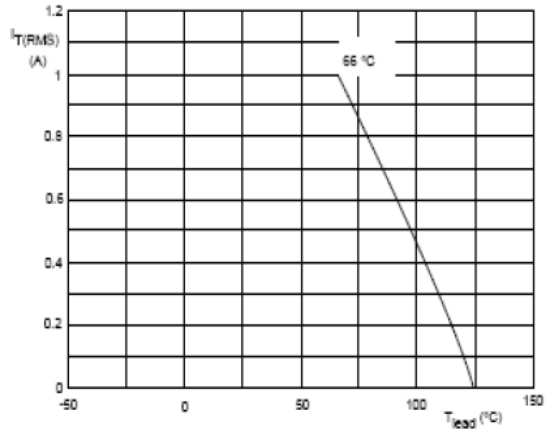For sinusoidal currents,f=50HZ;Tlead${\leq}66℃$

Fig.4 Maximum permissible rms current
$I_{T(RMS)}$, versus lead temperature T_{lead}
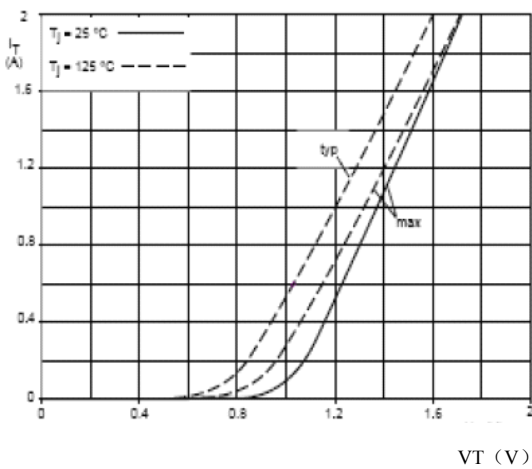
Fig.5 Typical and maximum on-state
characteristic

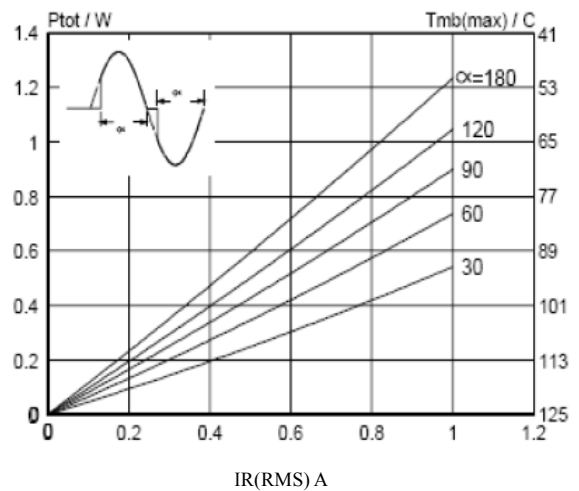Fig.6 Maximum on-state dissipation,P_{tot}
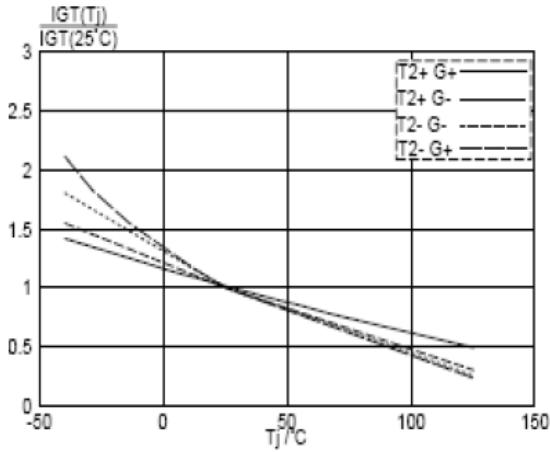versus rms on-state current,$I_{T(RMS)}$where
α=conduction angle.

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Fig.7 Normalised gate trigger current $I_{GT}(T_j)$/$I_{GT}(25°C)$,versus junction temperature T_j.
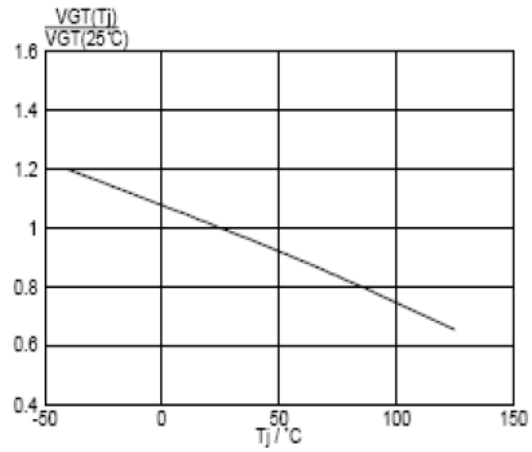

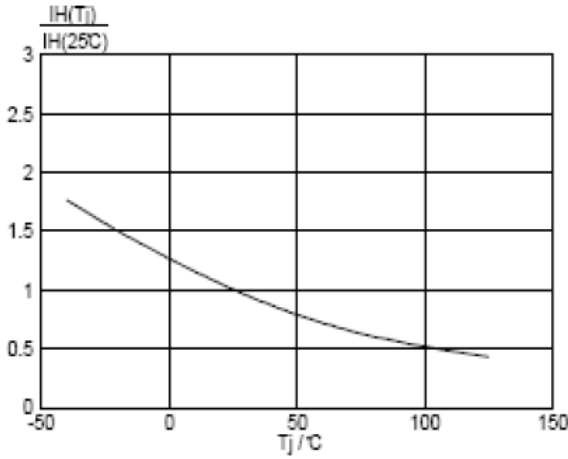Fig.8 Normalised gate trigger voltage $V_{GT}(T_j)$/$V_{GT}(25°C)$,versus junction temperature Tj-

Fig.9 Normalised holding current $I_H(Tj)$/$I_H(25°C)$
Versus junction temperature T_j.

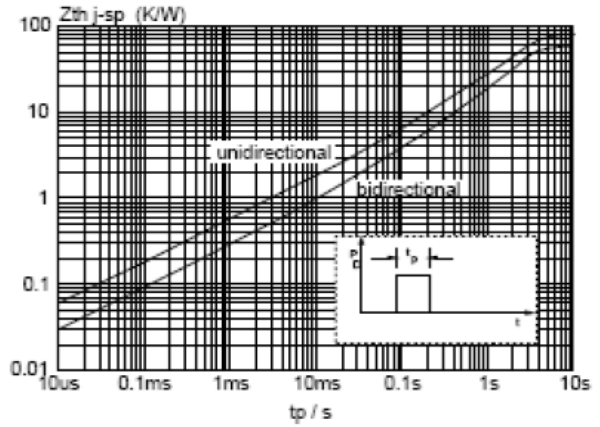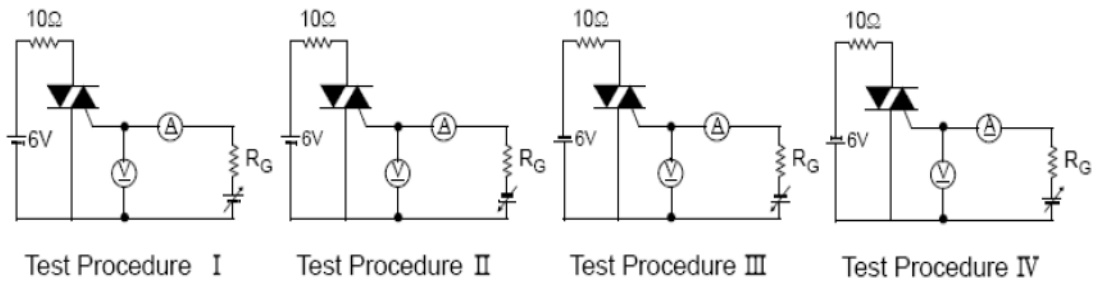Fig.10 Transient thermal impedance Z_{th}
$_{j-lead}$,versus pulse width t_p.

Test Procedure Ⅰ   Test Procedure Ⅱ   Test Procedure Ⅲ   Test Procedure Ⅳ

Fig.11 Gate Trigger Characteristics Test Circuit

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TO-92 Package Dimension