Description

The RM5631A is a monolithic, IC filter now available for use in the band separation filtering of low speed (300 baud) originate/answer modem applications.

The device contains two 10-pole switched-capacitor bandpass filters fabricated in NMOS technology and it is packaged in a single 16-pin dip. The pinout configuration for this device is shown in Figure 1, and the package dimensions are shown in Figure 9.

This transmit and receive filter is compatible with CCITT V.21 modems. Switching the filter between originate and answer modes is accomplished by a TTL-compatible input pin.

Included on the chip is a receive gain control stage externally adjustable from 0 to 30 dB, a separate limiter for use with the receive output, a TTL-compatible input for self-test mode and an on-chip oscillator. The block diagram is shown in Figure 2.

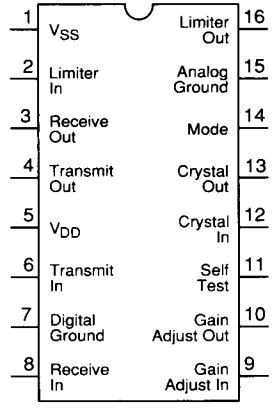

Figure 1. Pinout Configuration

Device Operation

The modem filters are self-contained. They require only plus and minus supplies and either an external 1 MHz input clock (CMOS) or a 1 MHz crystal with two capacitors and a resistor (as shown in Figure 3). With accurate clocking, center frequency

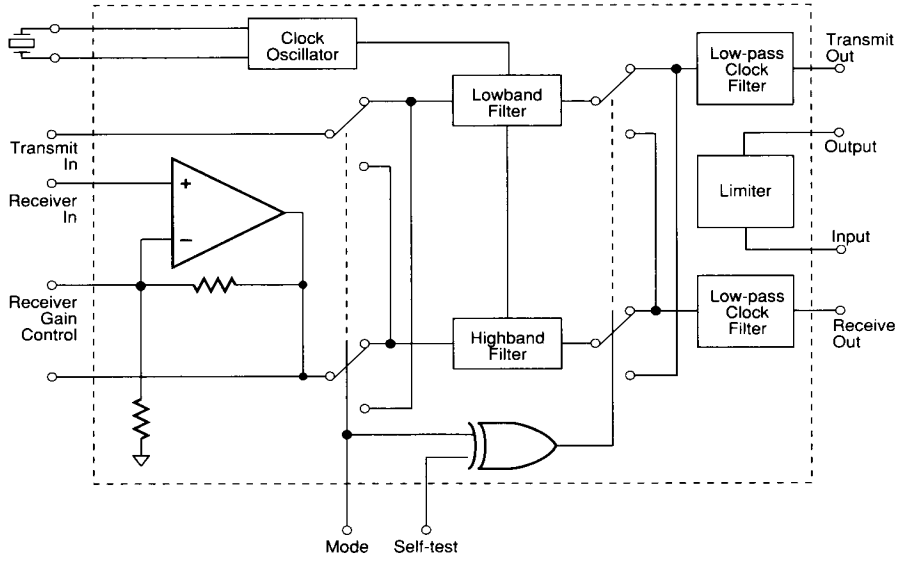

Figure 2. 300 Baud Modem Filter Chip Block Diagram

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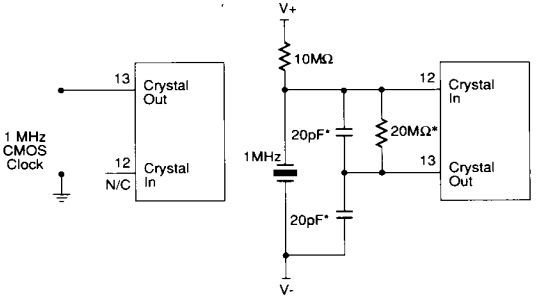
shifts of the filters are less than ±1%. For either the highband or lowband filter, maximum S/N is obtained when the input, after the mode switches, is $5V_{p-p}$ for ±5V only ($10V_{p-p}$ for ±10V supplies). For optimum receive performance at minimum S/N (≤10 dB), the circuitry of Figure 4 is recommended; then low-level signals will be limited by the Output Noise specification.

Gain Adjust

For tight control of receive gain, it is recommended that an attenuation network, such as a resistor divider, be placed ahead of the receive input. The device currently has a receive gain of 18.5 dB ±1 dB. Note that gain control, pins 9 and 10, is also accomplished by the parallel resistor technique; however, device-to-device variation restricts tight gain control from these pins unless resistor values are selectable or a trimpot is used. Refer to Figure 8 for further information.



* Component values may vary with parasitic capacitances

Figure 3. Clocking Circuits

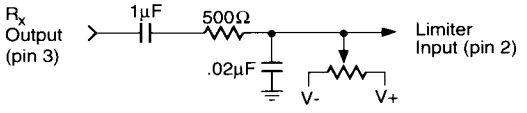


Figure 4. Interface Circuitry to Limiter

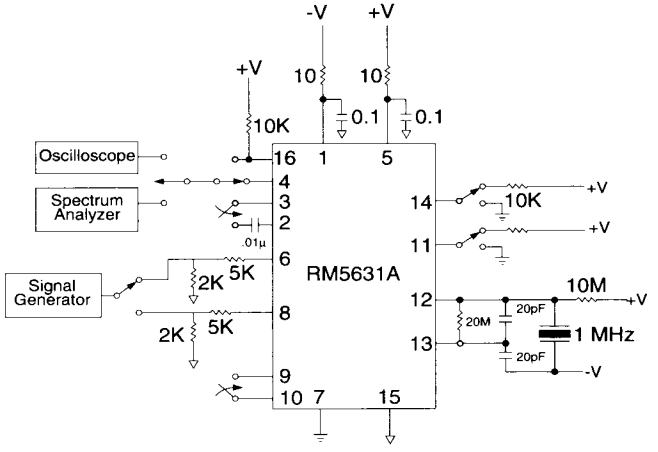


Figure 5. Test Circuit

Limiter Operation

It is recommended that an AC-coupled low-pass filter be placed between the Rx Output and the Limiter Input (see Figure 4). Component values are chosen based on the limiter input impedance. In this way, the filter DC offset is blocked and limiter operation is constrained to the signal bandwidth. The bandwidth consideration is important; typically 5-20 mV_{p-p} of clock feedthrough (from oscillator or sampling frequencies) is inherent in SCFs. Note also the potentiometer for compensation of the Limiter Offset Voltage. The component value can be chosen between 100KΩ and 1MΩ. Either offsets or clock feedthrough raise the apparent output noise and reduce the dynamic range.

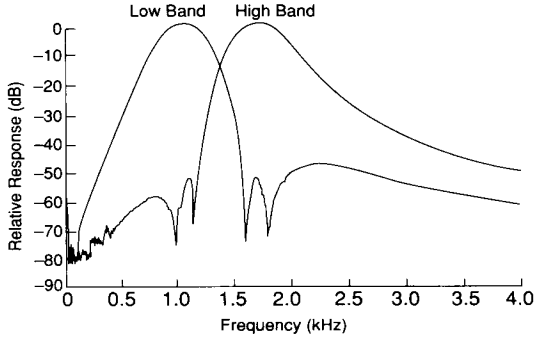


Figure 6. Typical Frequency Response, 200/300 Baud Modem Filter

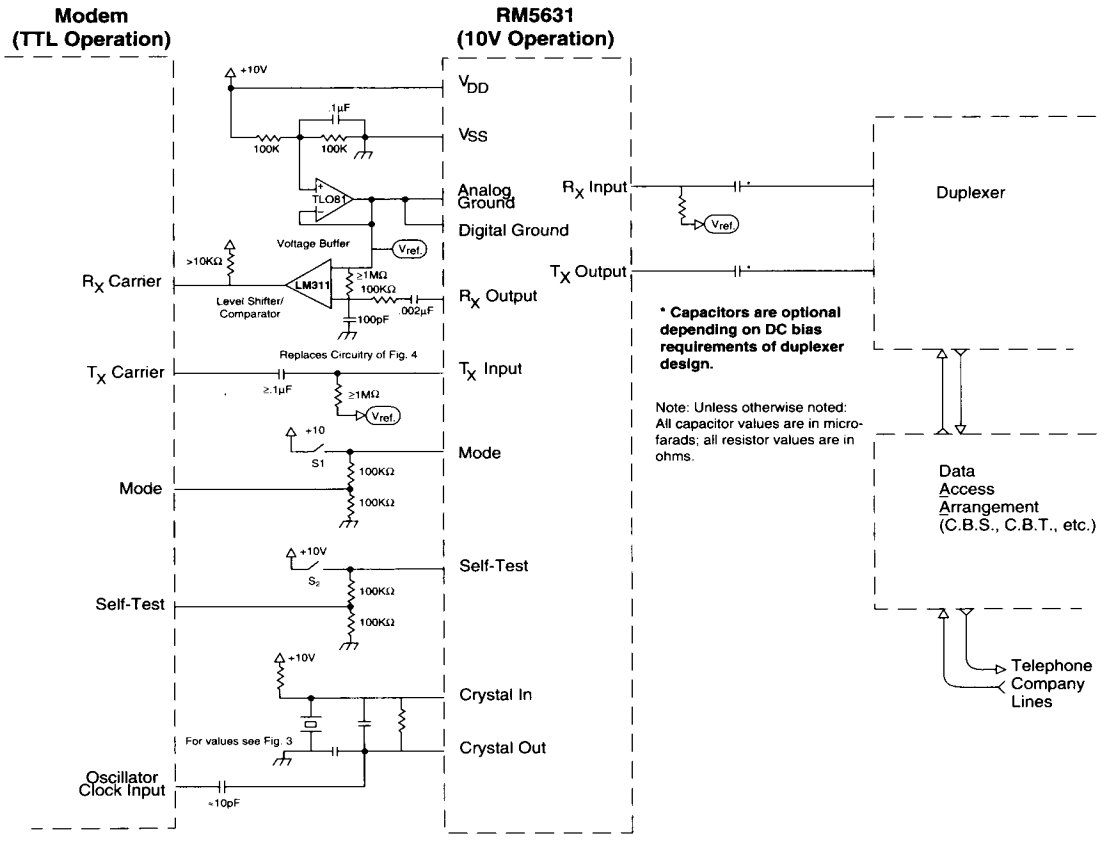


Figure 7. Single Supply Operation

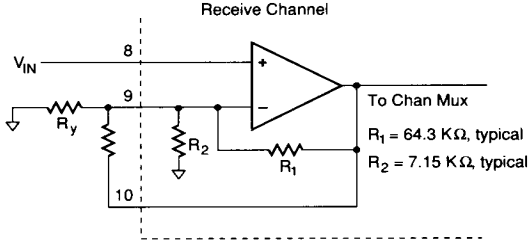


Figure 8. Gain Adjust Schematic

Note: Both R1 and R_2 are implemented as polysilicon resistors. For the "worst-case" calculations, variance of their value ought to be set at ±40%. If the parallel combination of R_1 and R_x (R_1//R_x) is represented by R_f, and R_2 and R_y(R_2//R_y) by R_s, then the gain equation is simplified:

$$20 \log (1+R_f/R_s) = \text{Gain (dB)}$$

From this a gain tolerance can be evaluated. Note that the value of R_1 and R_2 change form typical by the same percentage, plus or minus. For example, when R_y is 6.8KΩ and R_x is 18KΩ, the gain is 12 dB ±1 dB.

Gains to 30 dB are possible if loading of the on-chip op-amp does not fall below 10KΩ.

Table 1. Absolute Minimum/Maximum Ratings

	Min	Max	Units
Input voltage - any terminal with respect to substrate, pin 1 (V_{SS})	-0.4	21	V
Output short-circuit duration — any terminal	Indefinite		
Operating temperature	0	70	°C
Storage temperature	-55	125	°C
Lead temperature (soldering, 10 sec.)		300	°C

Caution: Observe MOS handling and operating procedures

Note: This table shows stress ratings *exclusively*. Functional operation of this product under any conditions beyond those listed under standard operating conditions is not suggested by the table. Permanent damage may result if the device is subject to stresses beyond these absolute min/max values. Moreover, reliability may be diminished if the device is run for protracted periods at absolute maximum values.

Although devices are internally gate-protected to minimize the possibility of static damage, MOS handling precautions should be observed. Do not apply instantaneous supply voltages to the device or insert or remove device from socket while under power. Use decoupling networks to suppress power supply turn-off/ on switching transients and ripple. Applying AC signals or clock to device with power off may exceed negative limit.

Table 2. Device Characteristics and Operating Range Limits [1]

Parameter	Conditions & Comments		Sym	Min	Typ	Max	Units
Supply voltages			V_{DD}	+5		+10	V
			V_{SS}	-5		-10	V
Quiescent current [2]	No load		I_{QDD}		12	20	mA
			I_{QSS}		13	20	mA
Clock frequency	$f_c = 4xf_s$		f_c		1		MHz
Clock pulse width	External clock		T_{cp}	200		$10^9/f_c$-200	nsec
Digital input levels			V_{IL}	V_{SS}		0.8	V
(mode, self-test, clock)			V_{IH}	2.0		V_{DD}	V
Center frequency Highband	f_{OH}			1750			Hz
	Lowband		f_{OL}		1080		Hz
Output signal		R_L=600Ω	V_o-T_x	2.2			V_{p-p}
		R_L≥27KΩ	V_o-T_x,R_x	4.8	5.5		V_{p-p}
	V_i=6V_{p-p}	R_L=gnd	I_o-T_x			10	mA
		R_L=gnd	I_o-R_x			2	mA
	Input≥+15mV	R_{LIM}≥2.7KΩ	V_{LIM}-Low	0.4	0.6	0.8	V
Input impedance(s)			R_i	10			MΩ
			C_i			10	pF
	Limiter only		R_i		3		KΩ
	Limiter only		C_i		100		pF
Load impedance(s)			R_L-T_x	0.6	27		KΩ
			R_L-R_x	10	27		KΩ
			R_L-Lim.Out	2.7	10		KΩ
			C_L-T_x			5000	pF
			C_L-R_x			1000	pF
Output impedance	Small-signal		R_o-T_x		2	10	Ω
	Small-signal		R_o-R_x		10	100	Ω
Output offset voltages	Tx and Rx		V_{off}		20-50	200	mV
Limiter offset voltage	Input				5		mV
Input bias current			I_B		.001-.01	10	nA

Notes:

[1] V_{DD} = +5V,V_{SS} = -5V, f_s = 250 kHz (f_c = 1 MHz), T = 25°C

[2] Increases 15% for operation at 0°C; increases 30% for operation at ±10V

Table 3. Performance Standards [4]

Parameter	Conditions & Comments	Sym	Min	Typ	Max	Units
Total harmonic distortion [2]						
V_{in} = $5V_{p-p}$ @ 1 kHz	THD lowband				1.5	%
	THD highband			1.0	2.0	%
Output noise [1]				1.0	2.0	mV_{rms}
Crosstalk				-60	-58	dB
Insertion loss [5]			0.5	1	3	dB
Ripple				1	2	dB
Dynamic range [2]		DR	66	72		
3dB bandwidth (both bands)		BW	330	350	370	Hz
Adjacent channel rejection			50	53		dB
Group delay variation [3]		GD		100	200	µsec

Notes:

1 15 kHz bandwidth

2 5 V_{p-p} input (DR = peak-to-peak output divided by rms noise).

3 GD = - $\Delta\phi/\Delta w$; GD variation = $|GD_{mark} - GD_{space}|$, where GD_{mark} = Group delay at the mark frequency and GD_{space} = Group delay at the space frequency. Δf = Mark to space frequencies, $\Delta\phi$ = relative phase shift in radians between mark and space frequencies.

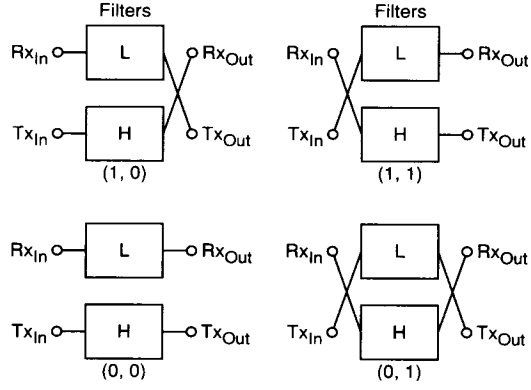
4 V_{DD} = +5V, V_{SS} = -5V, f_c = 1MHz,25°C, f_s = 250 kHz, R_L>27KΩ

5 For Rx_{in}, this gain applies when pin 9 is connected to pin 10.

Table 4. Operational Programming

Self Test	Mode	Rx_{In}	Rx_{Out}	Tx_{In}	Tx_{Out}
0	0	L	L	H	H
0	1	H	H	L	L
1	0	L	H	H	L
1	1	H	L	L	H

L = Lowband Filter
H = Highband Filter



16-Pin Plastic

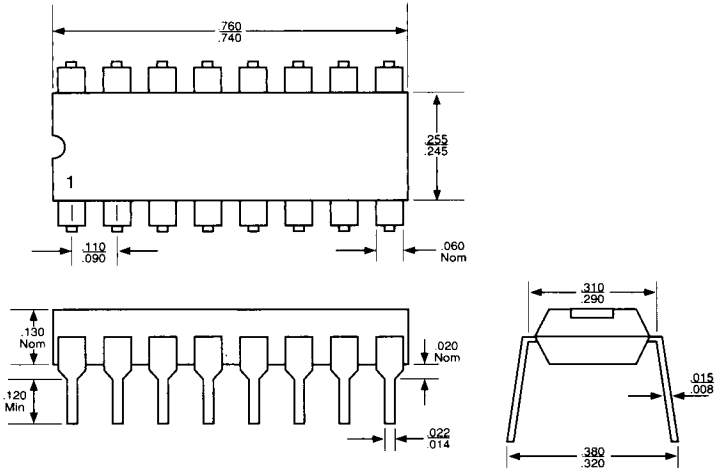


Figure 9. Package Dimensions

Ordering Information

Part Number	Description
RM5631ANP-011	200/300 Baud, modem filter combination, full-duplex, CCITT V.21 compatible