

Advance Information

MC92460EC/D
Rev. 1.0, 7/2002

MC92460 HDLC Controller
Hardware Specifications



NCSD Applications

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MC92460 Multichannel HDLC Controller.

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Features

Figure 1 shows a block diagram of the MC92460.

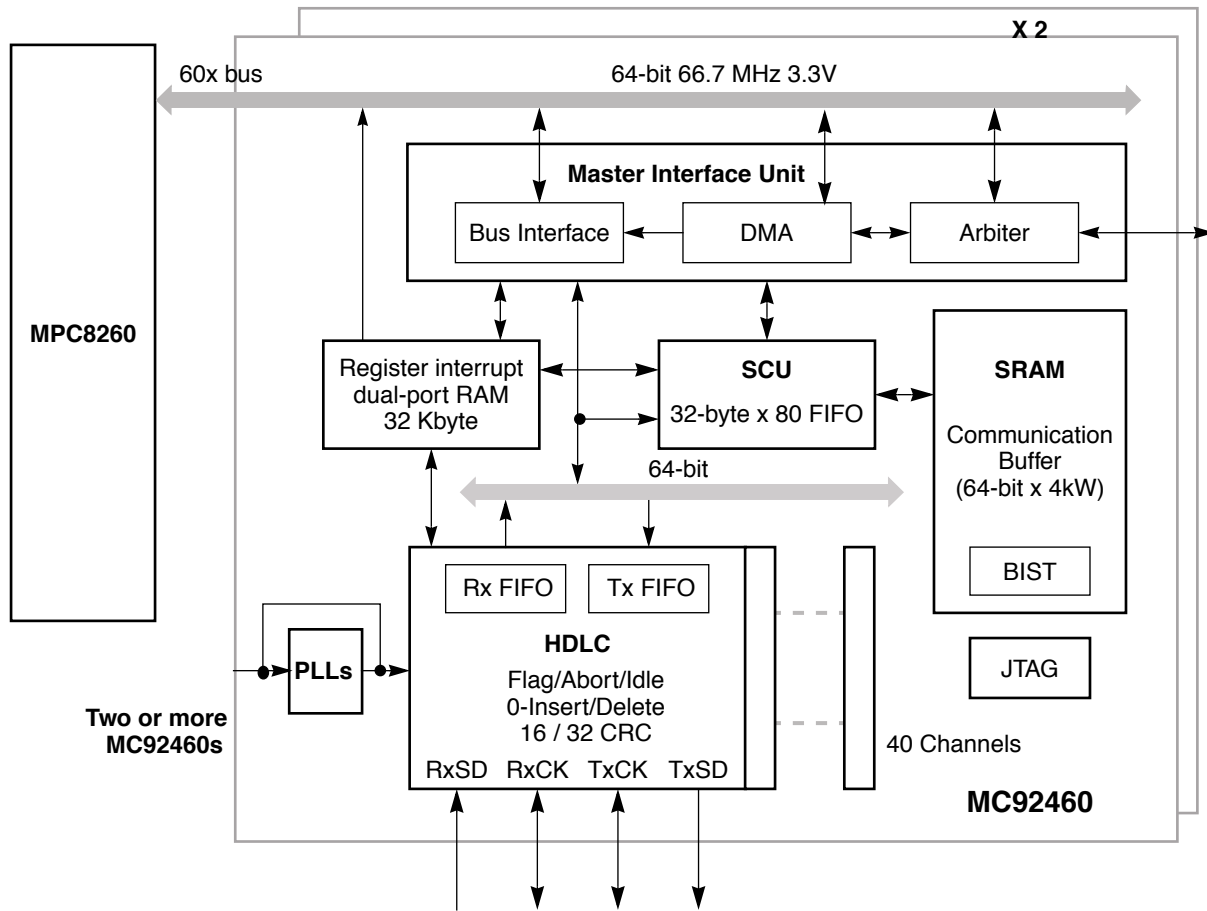


Figure 1. MC92460 Block Diagram

1.1 Features

The following is an overview of the MC92460 feature set:

- Channels
 - 40 full-duplex HDLC channels
 - Programmable channel assignment (any logical channel to any signal)
 - Each channel has a default of 64 buffer descriptors (Rx and Tx) but the number of buffer descriptors per channel is configurable
- Controllers
 - Maximum throughput of 1919 Mbps; individual controllers operate up to 66.7 Mbps
 - All communication controllers operate asynchronously
 - Programmable frame size (maximum 65,535 bytes)
 - Transparent memory access with internal memory controller
- 60x Bus
 - MC92460 directly connects with a 64-bit data and 32-bit address 60x bus
 - Supports 66.7 MHz 60x bus speed, with aggregate bandwidth of up to 1919 Mbps depending

- on the type of main memory used
- Up to four MC92460's may be connected in parallel on the 60x bus
- Bus supports multiple master design
- Communication Buffers
 - Data Buffer
 - 256 Kbits on-chip memory for data buffers
 - 256 Kbit communication buffer can store up to 819 bytes per frame.
 - 80 channel virtual DMA functionality executes between off-chip memory and the communication buffer
 - BD Buffer
 - 32 Kbyte on-chip dual-port RAM for buffer descriptors
 - A total of 4096 buffer descriptors (2048 TxBD and 2048 RxBD)
- JTAG Support
 - Supports the IEEE1149.1 JTAG controller standard
- Power and Clocks
 - Supports single-beat and burst accesses
 - On-chip PLL for baud rate generator (maximum of 66.7 MHz)
 - Separate power supplies for core internal logic (1.8V) and for I/O (3.3V)
- Package
 - 480 pin TPGA, 1.27 mm pitch

1.2 Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the MC92460.

1.2.1 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MC92460. Table 1 shows the maximum electrical ratings.

Table 1. Maximum Temperatures and Voltages

Rating	Symbol	Value Name	Unit
Core supply voltage	VDD	-0.3 – 2.5	V
I/O supply voltage	VDDH	-0.3 – 3.6	V
Input voltage	VIN	GND-0.3 – 3.6	V
Junction temperature	T _J	120	°C
Storage temperature range	T _{STG}	-55 – 150	°C
Ambient temperature	T _A	-40 – 85	°C

Table 2 lists recommended operational voltage conditions.

Table 2. Recommended Operating Conditions

Rating	Symbol	Value	Unit
Core supply voltage	VDD	1.65 – 1.95	V
I/O supply voltage	VDDH	3.15 – 3.465	V
Input voltage	VIN	GND -0.3 – 3.6	V
Junction temperature	T _J	105	°C

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

Table 3 shows DC electrical characteristics.

Table 3. DC Electrical Characteristics

TA=0 to 85°C; VDD=2.0±5% Vdc; VDDH=3.3±5% Vdc; GND=0Vdc; Load Capacitance < 10pF

Characteristics	Conditions	Symbol	Min	Max	Unit
Input high voltage		V _{IH}	2.0	3.465	V
Input low voltage		V _{IL}	GND	0.8	V
Input leakage current	V _{IN} =VDDH	I _{IN}	–	10	µA
HI-Z leakage current	V _{IN} =VDDH, GND	I _{OZ}	–10	+10	µA
Signal low input current	V _{IL} =0.8V	I _{IL}	–	60	µA
Signal high input current	V _{IH} =2.0V	I _{IH}	–	60	µA
Output high voltage	I _{OH} =-7.0mA	V _{OH}	2.4	-	V

Table 3. DC Electrical Characteristics (continued)

TA=0 to 85°C; VDD=2.0±5% Vdc; VDDH=3.3±5% Vdc; GND=0Vdc; Load Capacitance < 10pF

Output low voltage <ul style="list-style-type: none"> • BR • BG • ABB • TS • A[0-31] • AP[0-3] • APE • TT[0-4] • TBST • TSIZ[0-2] • GBL • CI • WT • LBCLAIM • BTO • INT • TC[0-1] • AACK • ARTRY • DBG • DBWO • DBB • DH[0-31],DL[0-31] • DP[0-7] • DPE • DBDIS • TA • DRTRY • TEA 	$I_{OL}=7.0\text{mA}$	V_{OL}		0.4	V
Output low voltage <ul style="list-style-type: none"> • Rx CLK[0-39] • Tx CLK[0-39] • Tx SD[0-39] • TDO • SBG • SDBG • SBR • SIRQ • CS0 • CS1 • CS2 	$I_{OL}=5.0\text{mA}$	V_{OL}		0.4	V

1.2.2 Thermal Characteristics

Table 4 describes thermal characteristics.

Table 4. Maximum Temperatures and Voltages

Characteristics	Symbol	Thermal Resistance Value	Unit	Air Flow
Thermal resistance for 480 TBGA	θ_{JA}	10.48	°C/W	0 LFM
		8.61	°C/W	100 LFM
		7.78	°C/W	200 LFM
		6.89	°C/W	400 LFM
		5.52	°C/W	800 LFM

LFM = Linear Feet per Minute

1.2.3 Power Considerations

The average chip-junction temperature, T_J , can be obtained from the following:

$$T_J = T_A + (P_D \cdot \theta_{JA})$$

where

θ_{JA} = package thermal resistance, junction to ambient, °C/W

T_A = ambient temperature, °C

Power equations are the following:

$P_D = P_{VDD} + P_{VDDH} =$ chip total power dissipation, W

$P_{VDD} = I_{VDD} \times VDD =$ chip core power, W

$P_{VDDH} = I_{VDDH} \times VDDH$

= user-determined power dissipation on input/output pins, W

1.2.4 Power Dissipation

Table 5 describes maximum chip core power dissipation.

Table 5. Maximum Core Power Dissipation (PVDD)

VDD(V)	SYSClk Frequency (MHz)	I _{VDD} (mA)	P _{VDD} (mW)	P _{VDDH} (mW)
1.95	66.7	650	980	920

1.2.5 AC Specifications

These AC specifications are target specifications.

1.2.5.1 SYSCLK Timing

Table 6 shows the system clock timing.

Table 6. Clock Timing

Characteristics	Symbol	Min	Max	Unit
Operation Frequency	f	60.0	66.7	MHz
Clock period		15.0	16.7	nS
Clock pulse width	t_{CL}, t_{CH}	7	8	nS
SYSCLK input high voltage	V_{IHC}	2.4	3.465	V
SYSCLK input low voltage	V_{ILC}	GND	0.4	V
SYSCLK Jitter			± 200	pS

Figure 2 shows the SYSCLK.

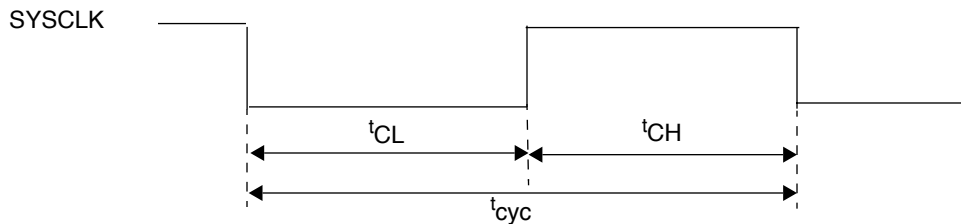


Figure 2. SYSCLK

1.2.5.2 EXCLK Timing

Table 7 shows the external clock timing.

Table 7. Clock Timing

Characteristics	Symbol	Min	Max	Unit
Operation Frequency	f	14.0	16.0	MHz
Clock duty		40	60	%
Clock Pulse width	t_{CL}, t_{CH}	25	42.8	nS
EXCLK input high voltage	V_{IHC}	2.4	3.465	V
EXCLK input low voltage	V_{ILC}	GND	0.4	V
EXCLK Jitter			± 200	pS

Figure 3 shows the EXCLK.

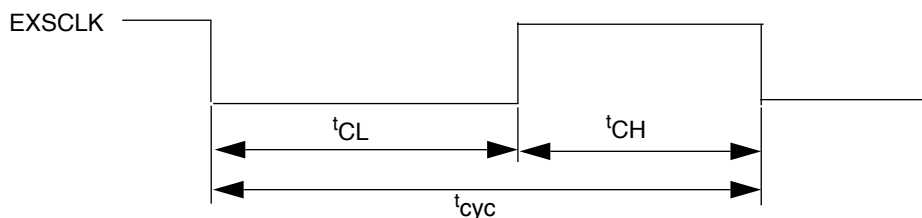


Figure 3. EXCLK

1.2.5.3 AC Timing

Figure 4 shows the HDLC external clock with polarity not inverted. All time specifications were measured at expected load capacitance $C_L=8pF$.

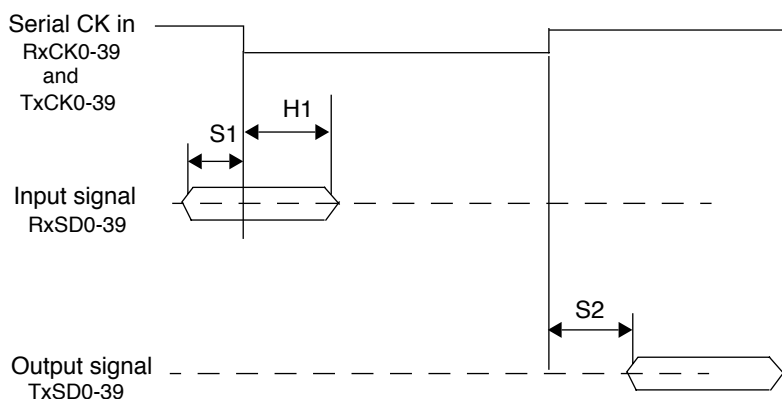


Figure 4. HDLC External Clock

Figure 5 shows an HDLC internal clock (TxCK/RxCK output mode) whose polarity is not inverted.

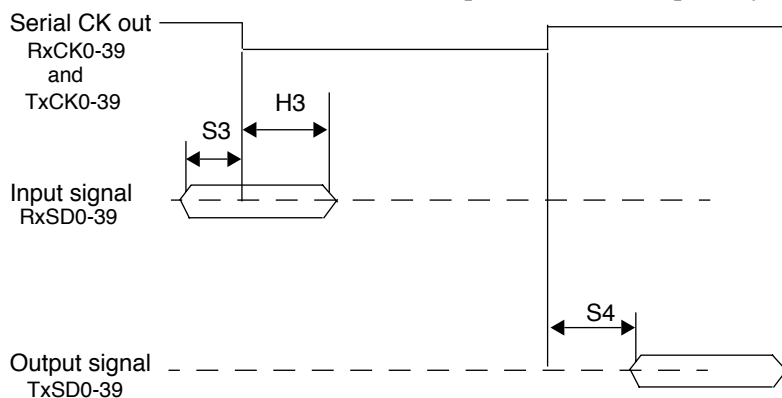


Figure 5. HDLC Internal Clock

Table 8 shows the AC electrical characteristics. The frequency is 20 MHz.

Table 8. AC Electrical Characteristics

Spec Num	Characteristic	Min	Max	Unit
S1	HDLC input- external clock setup time	2		nS

Table 8. AC Electrical Characteristics

H1	HDLC input -external clock hold time	1		nS
S2	HDLC output- external clock setup time		14	nS
S3	HDLC input- internal clock setup time	12		nS
H3	HDLC input- internal clock hold time	0		nS
S4	HDLC output- internal clock setup time		4	nS

Figure 6 shows the interaction of several bus signals.

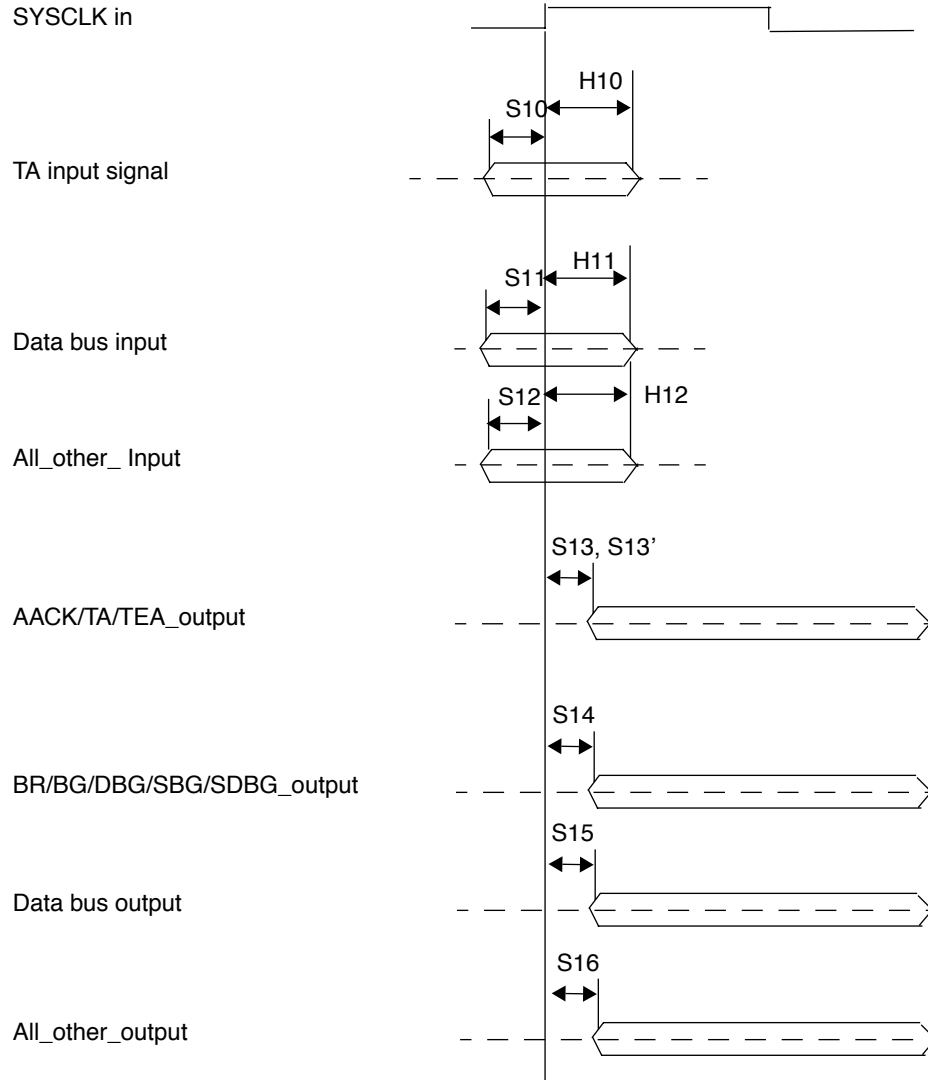


Figure 6. Bus Signals

Freescale Semiconductor, Inc.
Electrical and Thermal Characteristics

Table 9 shows the bus signal I/O characteristics. The frequency is 20 MHz.

Table 9. Bus Input/Output Characteristics

Spec Num	Characteristic	Min	Max	Unit
S10	TA/TEA input	6		nS
H10	TA/TEA input		1	nS
S11	Data bus input signals	7		nS
H11	Data bus input signals		1	nS
S12	All other input signals	7		nS
H12	All other input signals		1	nS
S13	AACK/TEA output	1	7	nS
S13'	TA output	1	8.5	nS
S14	BR/BG/DBG/SBG/SDBG output	1	7	nS
S15	Data bus output signals	1	8.5	nS
S16	All other output signals	1	7	nS

1.3 Pinout

Table 10. Pin Assignments

	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ball	
A	RwV656	RwV658	RwV658	scan_out_e	RwV623	CoreV623	RwV624	D9	CoreV623	D57	D32	D42	D11	D55	D59	CoreV617	D28	D52	D21	D45	D61	D30	D62	D23	D38	D31	D94	RwV659	RwV657	RwV656	
B	RwV657	RwV655	TEST0	scan_out_k	CoreV615	CS1	scan_out_h	D1	D25	CoreV616	D10	RwV627	D3	RwV628	CoreV617	D20	RwV630	D60	DP7	RwV632	D6	D30	D62	D23	D38	D31	D94	RwV659	RwV657	RwV656	
C	RwV655	TEST2	RwV654	RwV622	scan_out_j	CoreV615	scan_out_g	D56	RwV625	D49	CoreV616	D4	D56	CoreV624	RwV629	D4	D56	D5	D29	D53	D14	CoreV625	RwV634	CoreV625	D47	D8	RwV655	DP1	RwV650		
D	SEI	FPK	SMDD0	RwV623	scan_out_j	CSA2	scan_out_l	D48	D17	D41	D2	D26	CoreV624	D27	D43	D40	D44	CoreV631	CoreV618	CoreV618	D22	D46	D15	RwV635	D0	RwV652	DP0	DP2	DP3		
E	CSA5	CSA3	TEST3	SMODE1	RwV622	CS2	CS0	D24	D16	D33	RwV626	D18	D50	D19	D51	D12	scan_out_j	D13	D37	DP6	D38	D7	CoreV619	D63	RwV651	TR	TS20	RwV640	CoreV640		
F	CSA1	RwV621	DPW0	scan_out_d	AMODE																				TEST	TS21	DEG	TS	CoreV650		
G	PCMD	TEST1	DPD0	CoreV614	CoreV614																				TS22	CTD0	ABB	XACK	XNTYP		
H	TCK	TRST	TDI	FPRESET	CSA0																				ERG	RwV641	TT0	DPE	TT2		
J	FLLD0	ACoreV642	ERCLK	TDO	TMS																				TT1	TT3	TT4	SBCEI	RwV642		
K	scan_out_c	RwV638	CoreV613	RwV639	ACoreV622																				DBE	A0	CoreV641	A1	SEB		
L	RwV639	RwV638	TS509	CoreV613	TRCK08																				A2	A3	CoreV651	A4	RwV643		
M	RwV637	RwV637	TS4D8	RwV620	TRCK08																				A5	A6	ERR	A7	AI		
N	TRCK08	RwV636	RwV636	TRCK07	TRCK07																				A9	RwV644	A10	A11	SEB		
P	CoreV612	TS5D6	TRCK35	RwV635	RwV635																				A13	A14	RwV645	A12	A15		
R	TRSD35	CoreV612	scan_out_b	RwV634	RwV634																				CoreV620	A16	A17	CoreV642	CoreV642		
T	TRCK4	RwV633	TS4D4	RwV619	RwV633																				A20	RwV646	A19	A21	A18		
U	TRCK33	TS5D33	RwV632	TRCK32	TRCK32																				RwV647	A24	A23	CoreV620	A22		
V	TRSD32	RwV631	RwV631	TRCK31	TRCK31																				TEA	A28	A27	A26	A25		
W	RwV630	scan_out_a	RwV630	CoreV611	TRCK30																				CoreV648	A31	RwV648	A30	A29		
Y	CoreV611	TS5D00	RwV618	RwV629	TRCK29																				DPRTY	DECDUM	SREQ	CoreV63	INT		
AA	RwV629	TS5D29	RwV628	RwV628	RwV627																				AP3	RwV649	AP0	CSA6	B10		
AB	TRCK28	TS5D28	RwV627	TRCK27	scan_in_k																				CI	WT	ZPE	AP2	AP1		
AC	TRSD27	RwV626	RwV626	CoreV610	CoreV610																				TC0	DE	MODE	RwV640	CSA4		
AD	TRCK26	RwV617	TS5D26	TRCK25	TRCK24																				FLLD0	TRCK0	CoreV64	TC1	CSA7		
AE	RwV625	TS5D25	TRSD24	TRSD24	RwV615																				RwV648	RwV648	ACoreV61	SYSLK	CoreV644		
AF	RwV624	RwV624	RwV616	RwV616	RwV616																				RwV648	RwV648	RwV648	ACoreV61	TSX00		
AG	RwV634	RwV633	RwV617	TS5D23	TRSD23																					RwV648	RwV648	RwV648	TSX01	RwV631	
AH	RwV621	RwV618	TRCK23	TRCK22	TRCK22																					RwV648	RwV648	RwV648	TRCK1	RwV611	RwV613
AJ	RwV619	RwV620	RwV633	scan_in_j	RwV633																						RwV648	RwV648	RwV648	RwV612	
29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ball		

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