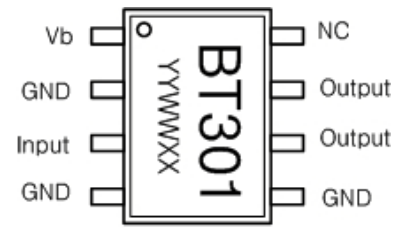


500-4000 MHz High Power Amplifier

Device Features

- 49dBm Output IP3 at 16dBm/tone at 1900MHz
- 18.5dB Gain at 900MHz
- 30.3dBm P1dB at 1900MHz
- Highly Reliable InGaP/GaAs HBT Technology
- Lead-free/Green/RoHS compliant SOIC8 package
- Patented Over Voltage Protection Circuit
- Application:
commercial, space, military wireless system



YY=Year, WW=Work week
XX=Wafer Number

Electrical Specifications ($T_a = 25^\circ\text{C}$, $V_s = 5.0\text{V}$)

Parameters	Test Conditions	Min	Typ	Max	Unit
Frequency Range		500		4000	MHz
Gain	900MHz	17.5	18.5		dB
	1900MHz	11.5	12.5		
	2140MHz	10.5	11.5		
	2450MHz	9.5	10.5		
S11	900MHz		-15.0		dB
	1900MHz		-18.0		
	2140MHz		-18.0		
	2450MHz		-12.0		
S22	900MHz		-7.0		dB
	1900MHz		-12.0		
	2140MHz		-12.0		
	2450MHz		-11.0		
OIP3	900MHz	46	49		dBm
	1900MHz	46	49		
	2140MHz	45	47		
	2450MHz	46	49		
P1dB	900MHz	28.5	29.5		dBm
	1900MHz	29.0	30.3		
	2140MHz	29.0	30.3		
	2450MHz	29.0	30.3		
IS-95 CH Power @ -50dBc ACPR	900MHz		22.5		dBm
	1900MHz		22.5		
WCDMA CH Power @ -50 dBc ACLR	2140MHz		25.0		dBm
	2450MHz		25.0		
NF	900MHz		8.5		dB
	1900MHz		8.6		
	2140MHz		7.5		
	2450MHz		7.5		
Ic	$V_c = 5.0\text{V}$	310	350	390	mA
Vc			5.0		V
Rth	Thermal Resistance		19.6		$^\circ\text{C/W}$

Test conditions unless otherwise noted.

1. $T = 25^\circ\text{C}$, $V_{\text{device}} = 5.0$, 50 ohm system.
2. OIP3 is measured on an eval-board with two tones separated by 1 MHz.
3. ACPR Test set-up: IS-95 CDMA, 9 Ch. Fwd, +885 KHz offset.
4. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5MHz offset,.

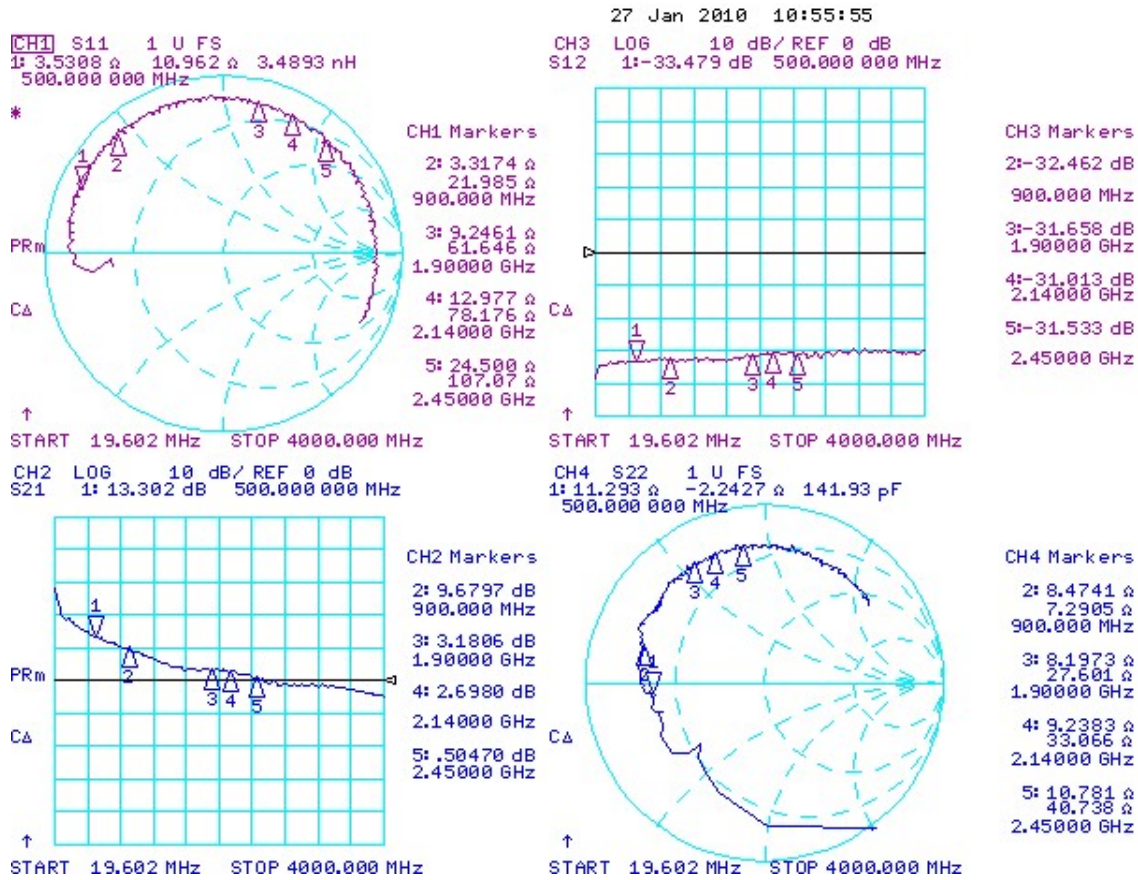
Absolute Maximum Ratings

Parameters	Rating
Operating Case temperature	-40 to +85°C
Storage Temperature	-55 to +155°C
Junction Temperature	+220°C
Supply Voltage	6.0V
Max. Device Current	600mA
Input RF Power	28dBm above input P1dB

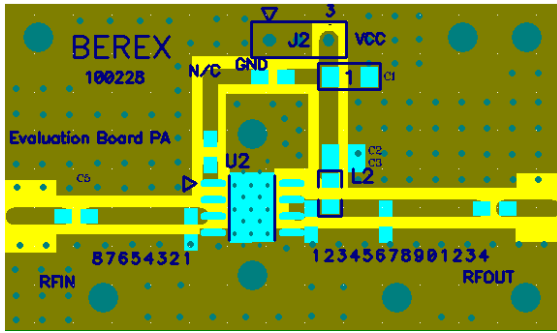
Operation of this device above any of these parameters may result in permanent damage.

Typical Device Data

S-parameters (Vc=5V, Ic=340mA, T=25°C)

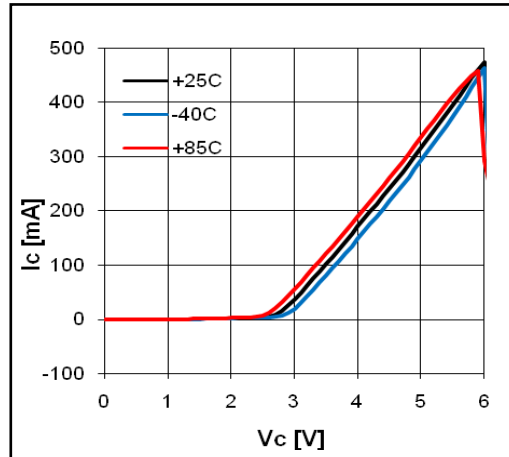


[Generic SOIC8 Evaluation Board]



- *Dielectric constant is 4.2
- *RF pattern width 52mil
- *31mil thick FR4 PCB

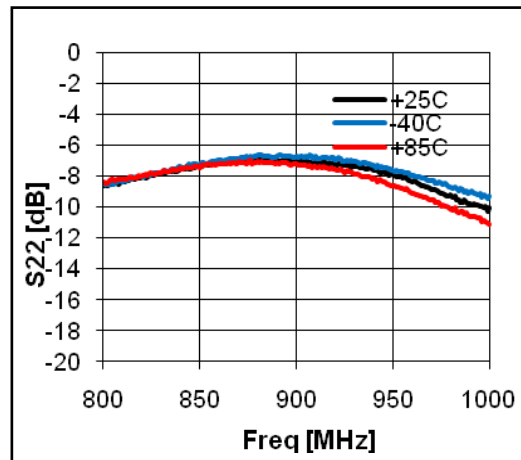
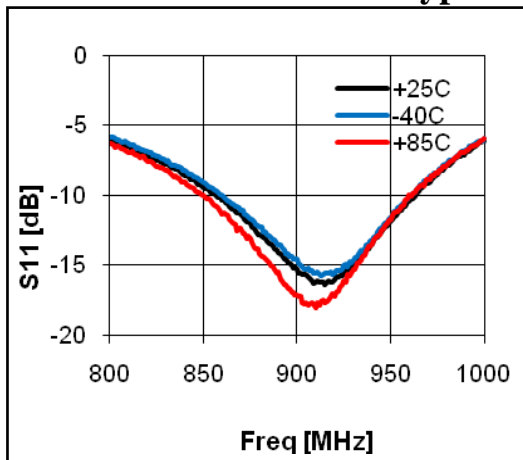
[I-V Characteristics]

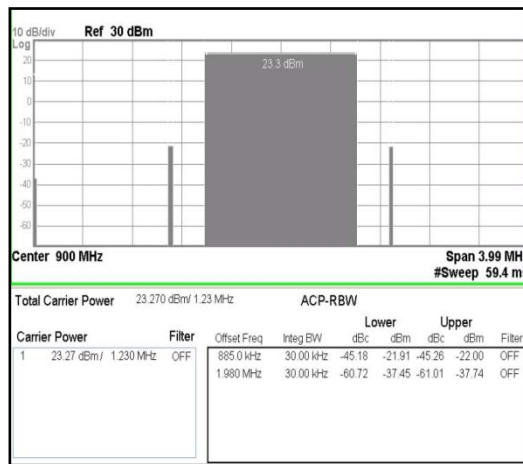
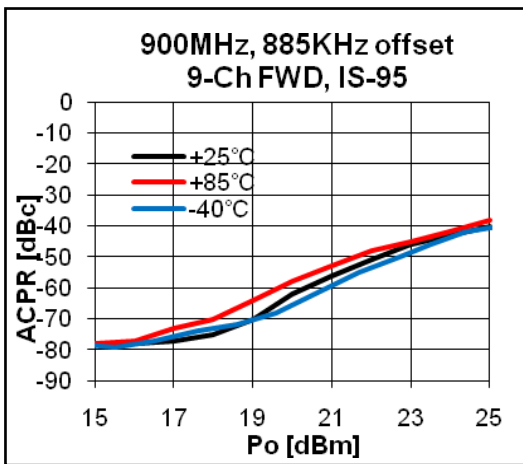
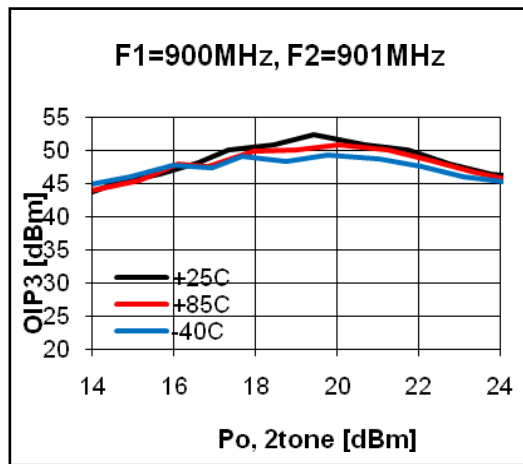
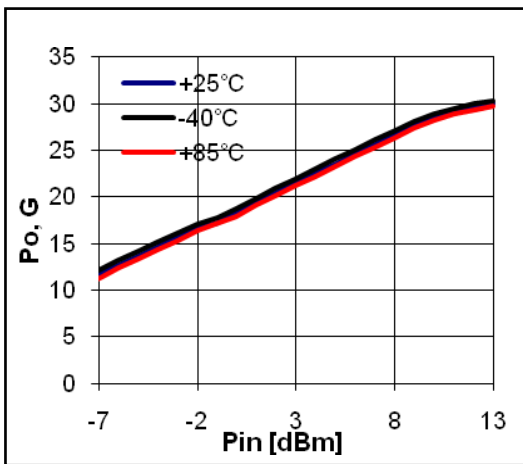
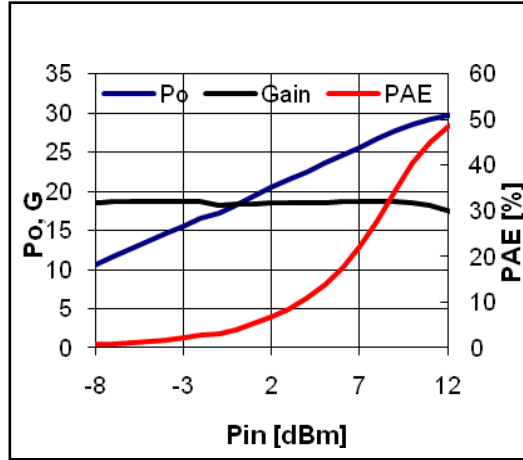
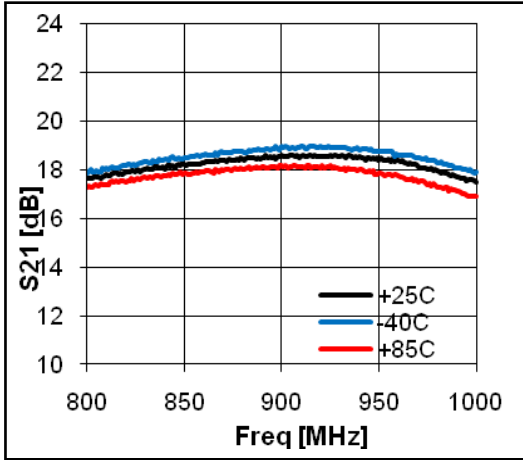


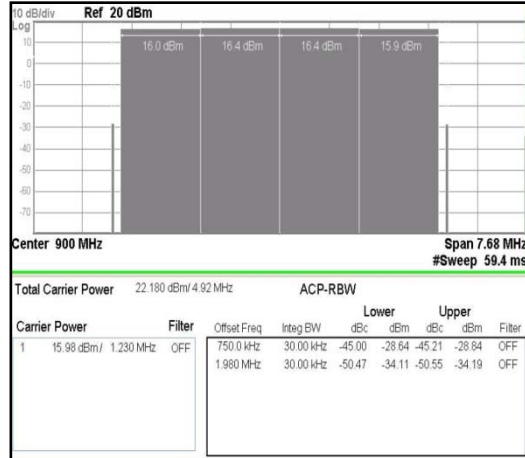
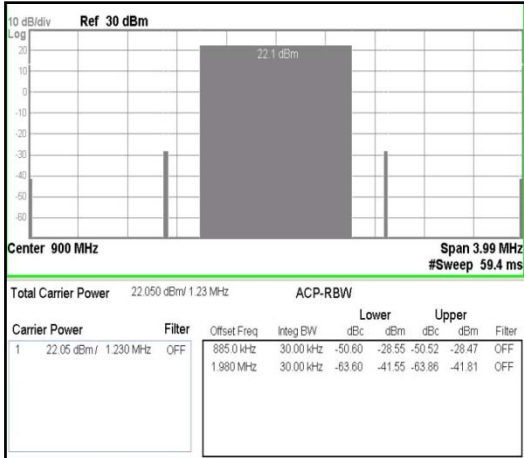
Application Circuit: 900 MHz

Schematic Diagram	BOM	Tolerance	
	C1	10uF	±20%
	C2	1.0nF	±5%
	C3	100pF	±5%
	C4	3,0pF	±5%
	C5	100pF	±5%
	C6	4.7pF	±5%
	C7	5.0pF	±5%
	C8	2.7pF	±5%
	C9	100pF	±5%
	R1	12ohm	±5%
L1	56nH	±5%	
L2	4.7nH	±5%	

Typical Performance



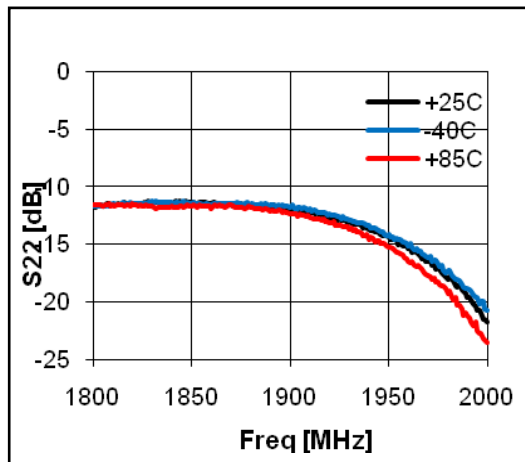
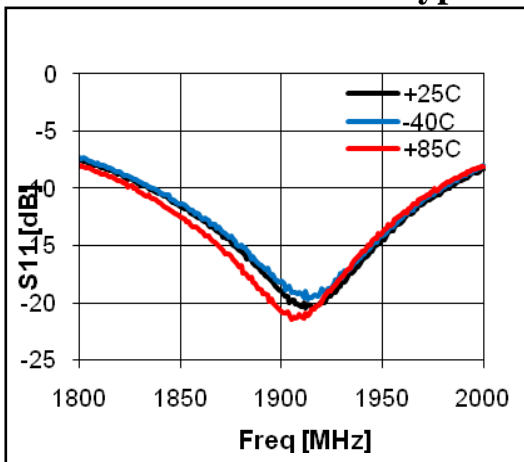


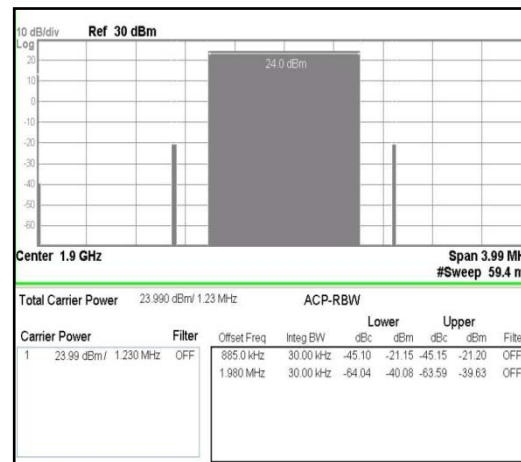
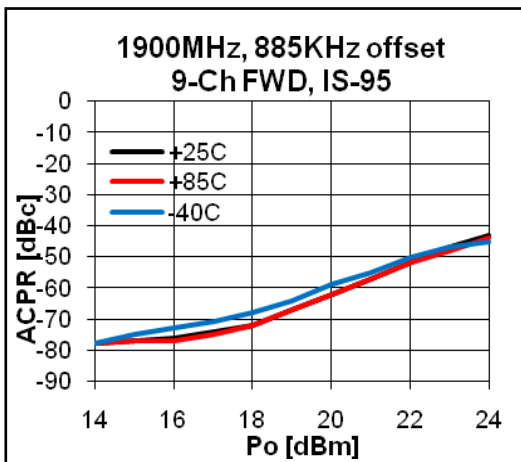
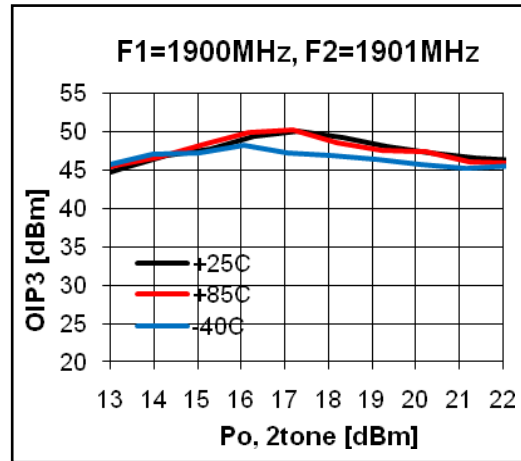
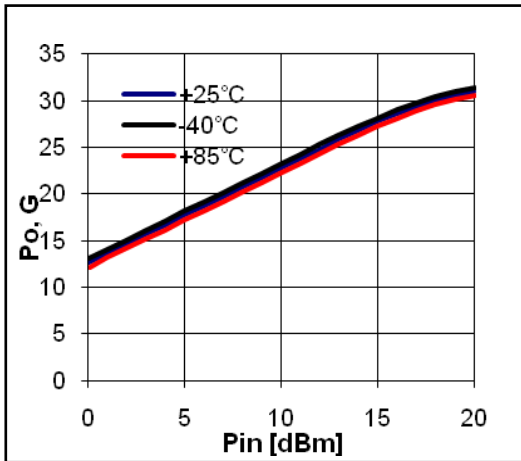
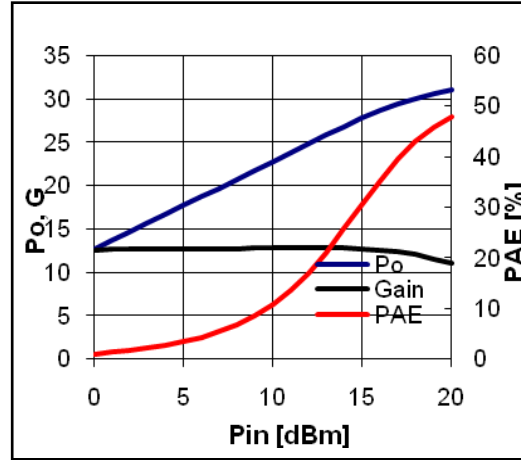
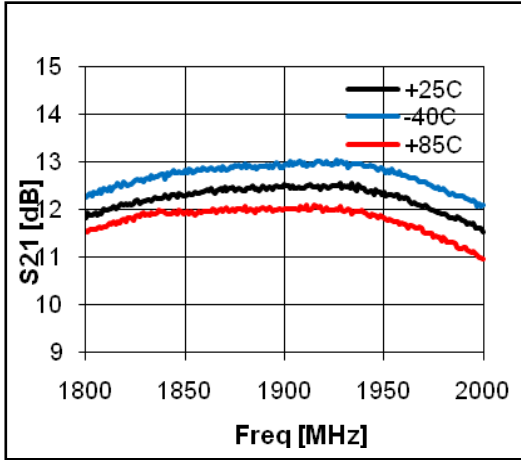


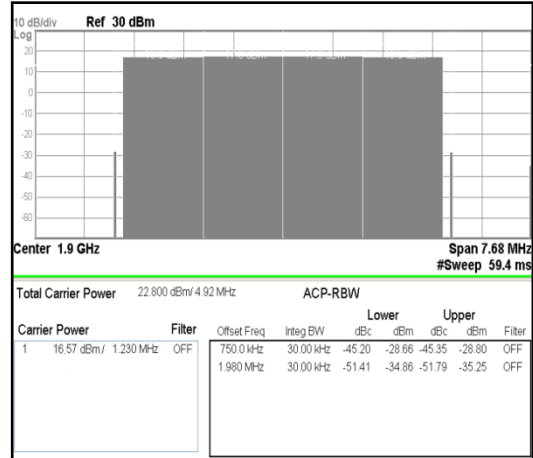
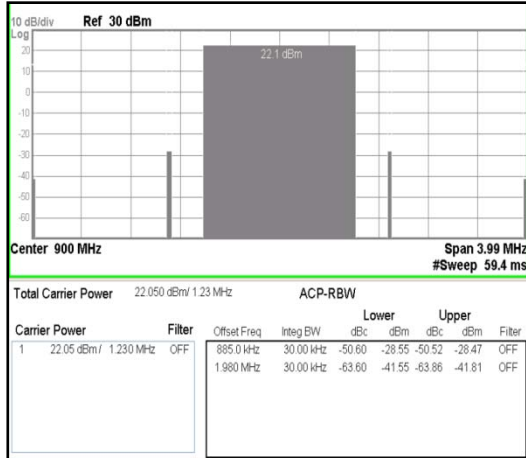
Application Circuit: 1900 MHz

Schematic Diagram	BOM	Tolerance	
	C1	10uF	±20%
	C2	1.0nF	±5%
	C3	100pF	±5%
	C4	100pF	±5%
	C5	100pF	±5%
	C6	2.7pF	±5%
	C7	2.5pF	±5%
	C8	2.5pF	±5%
	C9	100pF	±5%
	R1	12 ohm	±5%
L1	56 nH	±5%	
L2	6.8nH	±5%	

Typical Performance



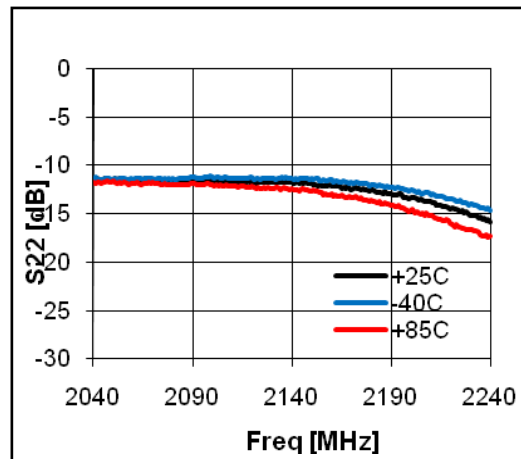
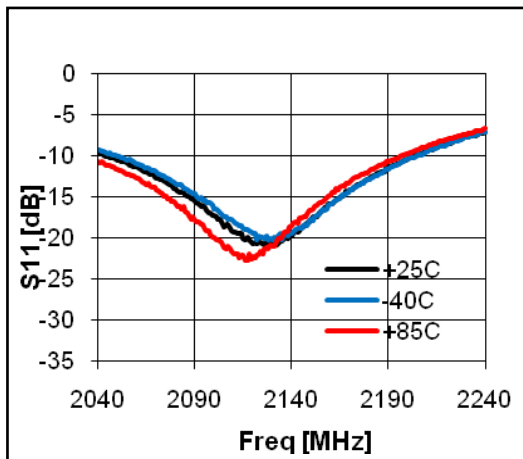


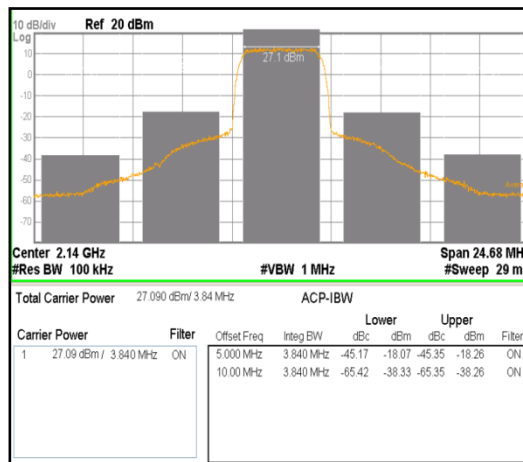
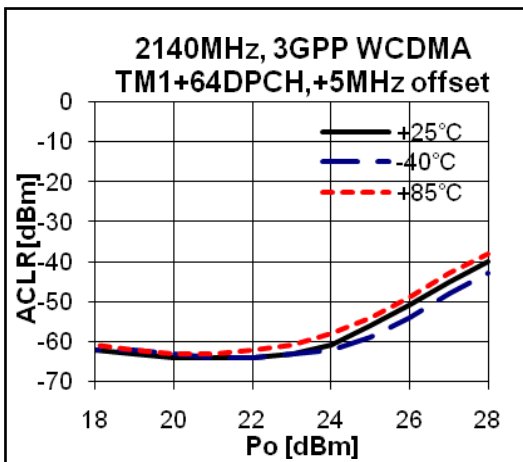
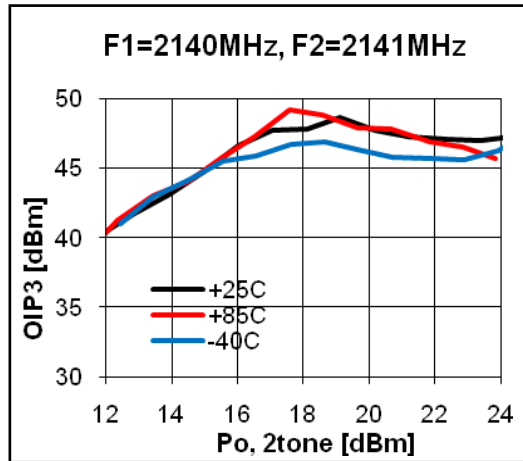
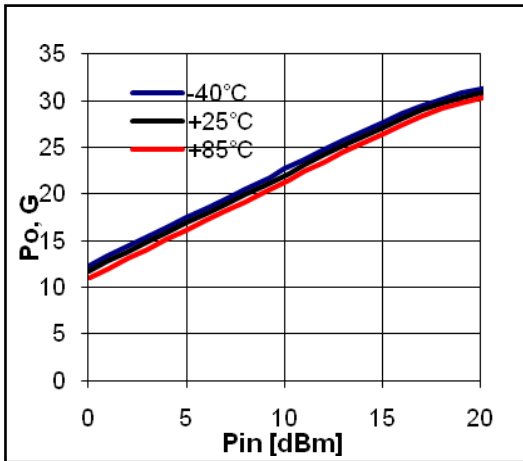
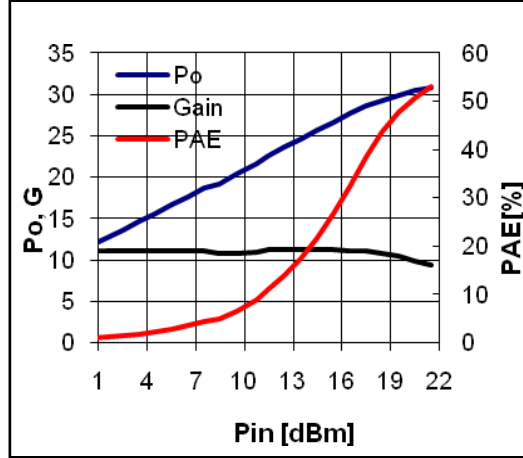
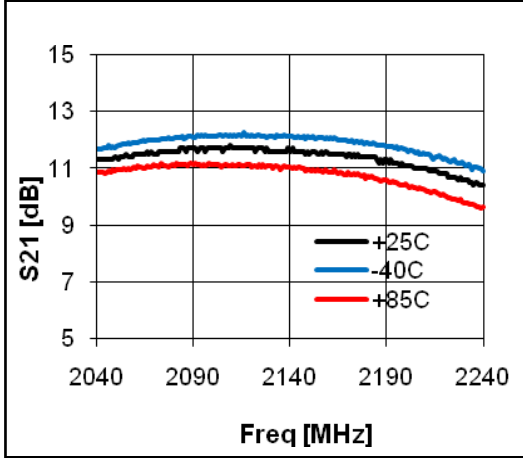


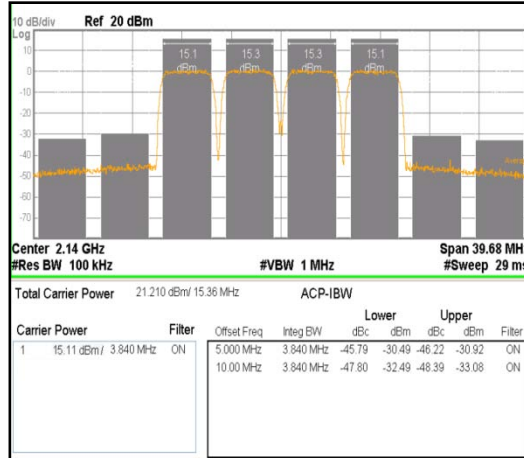
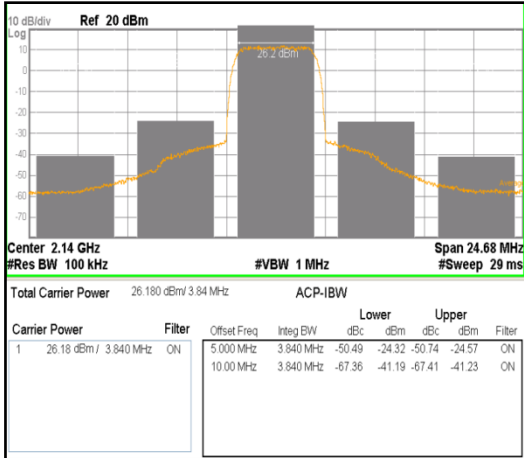
Application Circuit: 2140 MHz

Schematic Diagram	BOM	Tolerance	
	C1	10uF	±20%
	C2	1.0nF	±5%
	C3	100pF	±5%
	C4	100pF	±5%
	C5	100pF	±5%
	C6	2.2pF	±5%
	C7	1.8pF	±5%
	C8	2.0pF	±5%
	C9	5.0pF	±5%
	R1	12 ohm	±5%
L1	56 nH	±5%	
L2	4.7nH	±5%	
L3	100nH	±5%	

Typical Performance



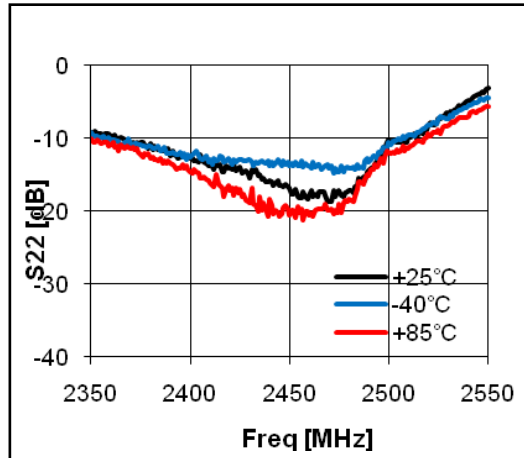
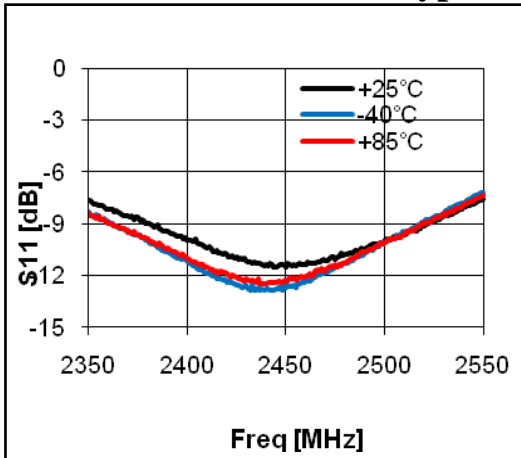


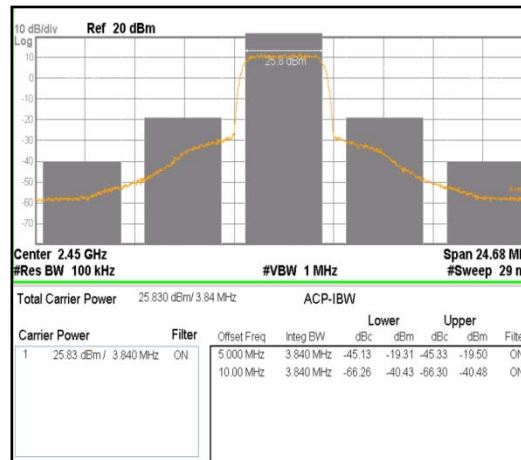
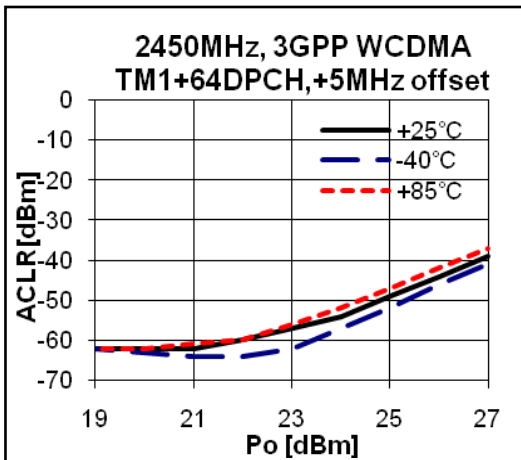
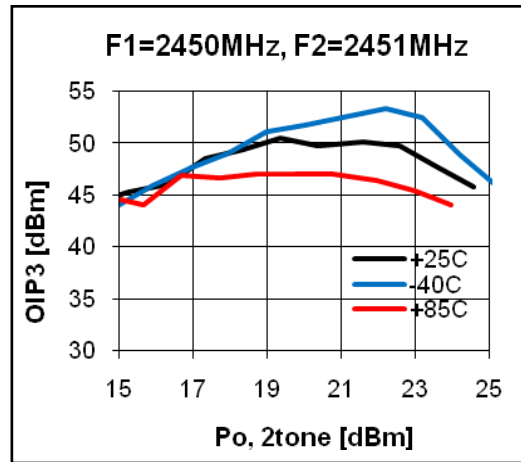
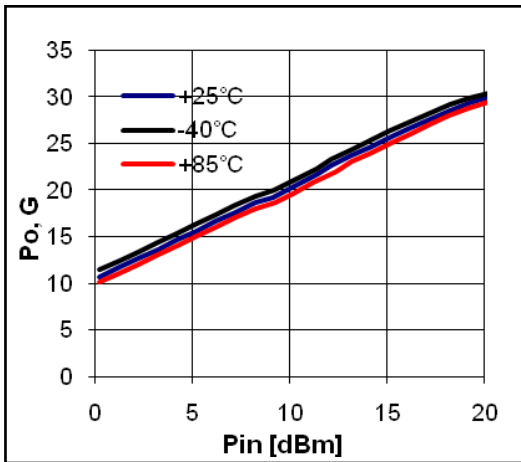
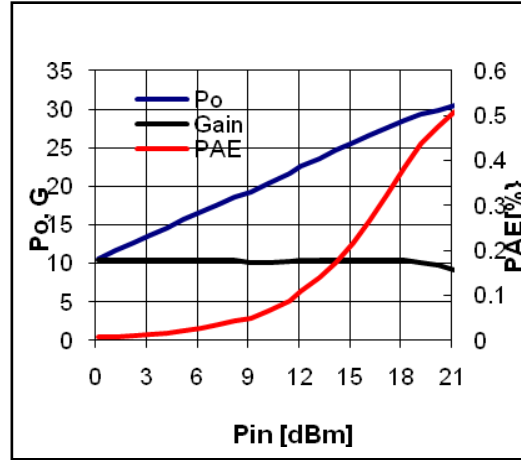
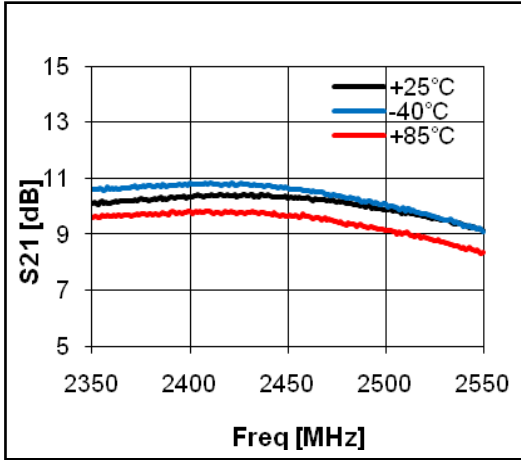


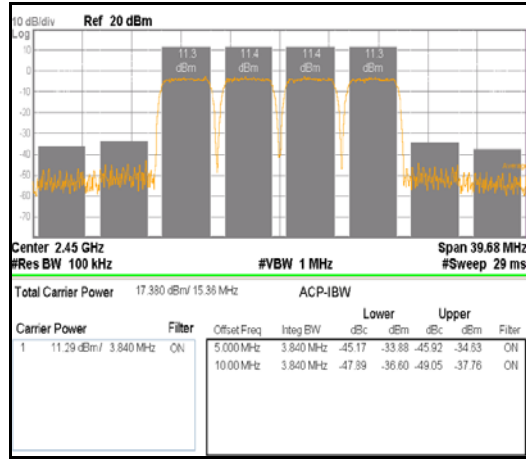
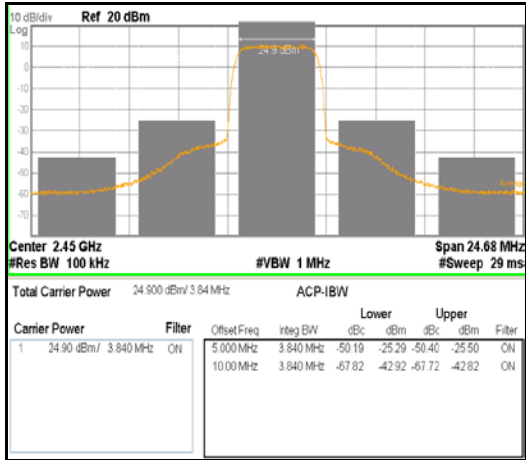
Application Circuit: 2450MHz

Schematic Diagram	BOM	Tolerance	
	C1	10uF	±20%
	C2	1.0nF	±5%
	C3	100pF	±5%
	C4	100pF	±5%
	C5	100pF	±5%
	C6	1.5pF	±5%
	C7	1.5pF	±5%
	C8	1.2pF	±5%
	C9	2.5 ohm	±5%
	R1	12 ohm	±5%
	L1	56 nH	±5%
	L2	4.7nH	±5%

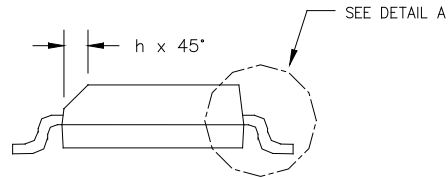
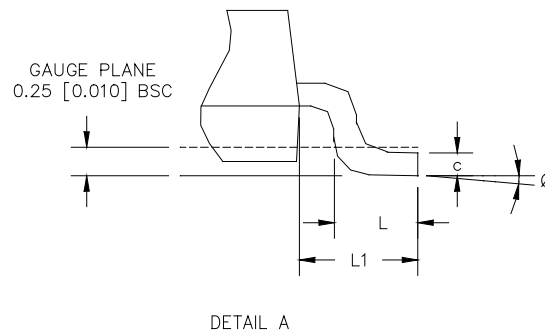
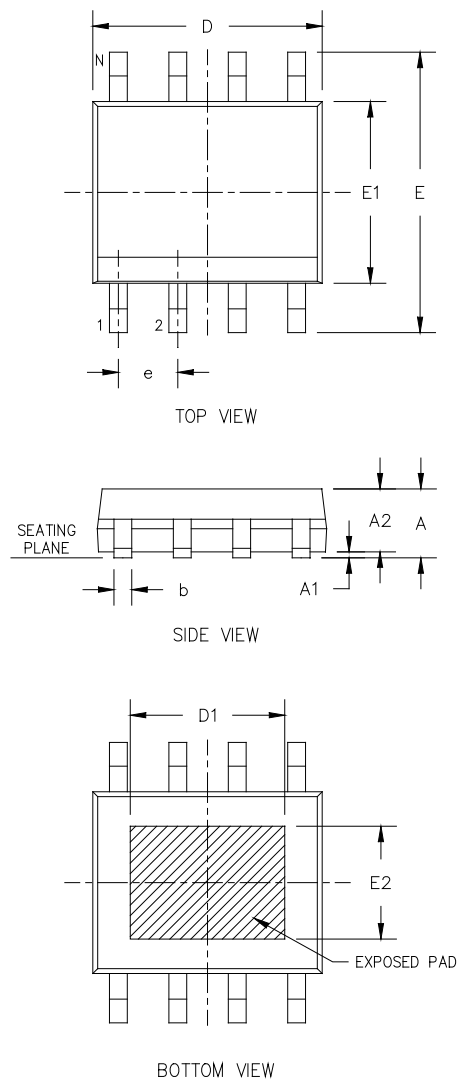
Typical Performance







Package Outline Drawing

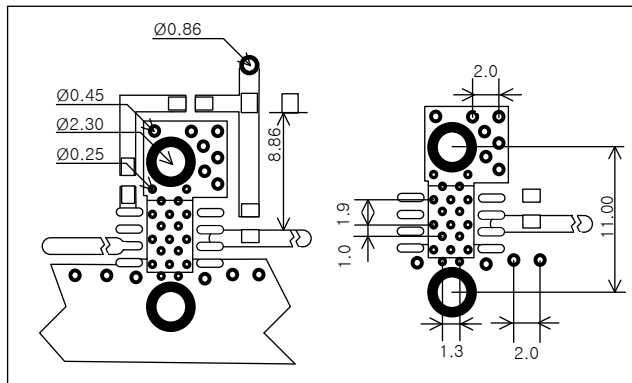


SYM	DIMENSION IN INCHES			DIMENSION IN MM		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.056	0.058	0.061	1.42	1.47	1.55
A1	0.001	0.004	0.005	0.025	0.102	0.127
A2	0.051	0.054	0.057	1.30	1.37	1.45
b	0.014	0.016	0.020	0.36	0.41	0.51
c	0.007	0.008	0.010	0.18	0.20	0.25
D	0.191	0.193	0.195	4.85	4.90	4.95
E1	0.151	0.153	0.155	3.84	3.89	3.94
E	0.234	0.240	0.244	5.94	6.10	6.20
e	0.050			1.27		
L	0.020	0.027	0.032	0.51	0.69	0.81
L1	0.042	0.044	0.046	1.07	1.12	1.17
Ø	0*	-	8*	0*	-	8*
h	0.011	0.015	0.019	0.28	0.38	0.48
D1	0.120	-	0.130	3.05	-	3.30
E2	0.085	-	0.095	2.16	-	2.41

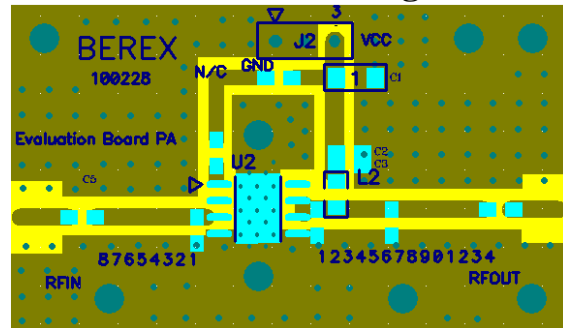
- NOTES:
1. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
 2. COPLANARITY APPLIES TO THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.003" [0.08 mm].
 3. BASED FROM JEDEC MS-012 VARIATION AA.

Suggested PCB Land Pattern and PAD Layout

PCB Land Pattern



PCB Mounting



Each CAD layout in the datasheet makes reference to the CAD file on BeRex website. (Visit <http://www.berex.com> for PCB layout)

Lead plating finish

100% Tin Matte finish.

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns)

MSL / ESD Rating

ESD Rating Value	Class 1C
Test Standard	Passes <2000V Human Body Model (HBM) JEDEC Standard JESD22-A114B
MSL Rating Standard	Level 3 at +265°C convection reflow JEDEC Standard J-STD-020

NATO CAGE code:

2	N	9	6	F
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NOTICE

BeRex Corporation reserves the right to make changes of product specification or to discontinue product at any time without notice.