# NCV8460

# Self Protected High Side Driver with Temperature Shutdown and Current Limit

The NCV8460 is a fully protected High−Side driver that can be used to switch a wide variety of loads, such as bulbs, solenoids and other acuators. The device is internally protected from an overload condition by an active current limit and thermal shutdown.

A diagnostic output reports ON and OFF state open load conditions as well as thermal shutdown.

## Features

- Short Circuit Protection
- Thermal Shutdown with Automatic Restart
- CMOS (3.3 V / 5 V) compatible control input
- Open Load Detection in On and Off State
- Diagnostic Output
- Undervoltage and Overvoltage Shutdown
- Loss of Ground Protection
- ESD protection
- Slew Rate Control for Low EMI Switching
- Very Low Standby Current
- NCV Prefix for Automotive and Other Applications Requiring AEC−Q100 Qualified Site and Change Controls
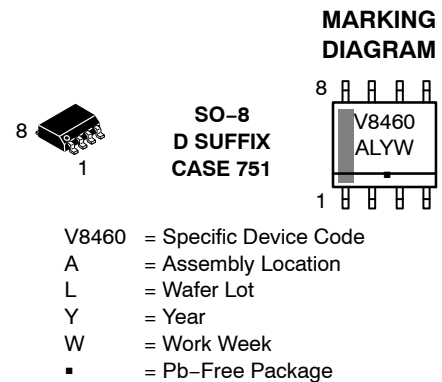- These are Pb−Free Devices

## Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
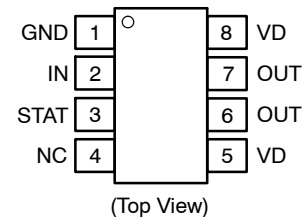- Automotive / Industrial

## ON Semiconductor®

http://onsemi.com

### MARKING DIAGRAM

SO−8
D SUFFIX
CASE 751

```
V8460
ALYW
```

V8460 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
■ = Pb−Free Package

### PIN CONNECTIONS

| | |
|---|---|
| GND 1 | 8 VD |
| IN 2 | 7 OUT |
| STAT 3 | 6 OUT |
| NC 4 | 5 VD |

(Top View)

### ORDERING INFORMATION

| Device | Package | Shipping[†] |
|---|---|---|
| NCV8460DR2G | SOIC−8 (Pb−Free) | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
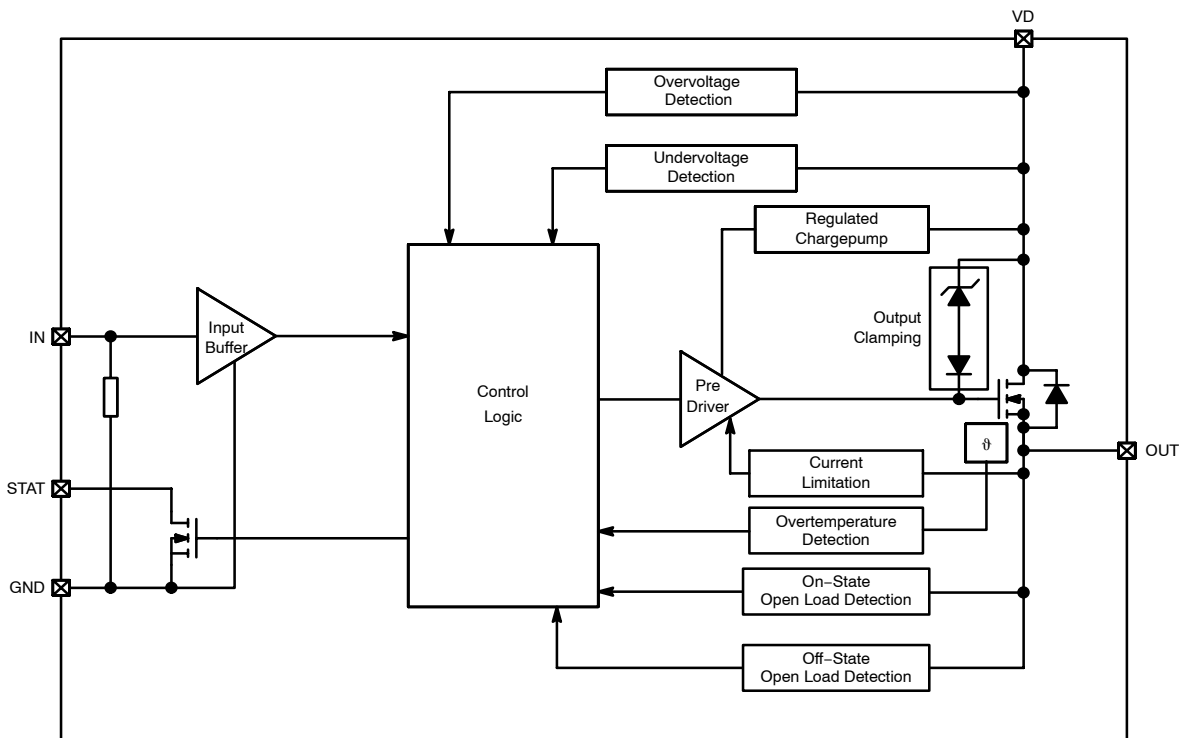
# NCV8460



**Figure 1. Block Diagram**

## PIN DESCRIPTION

| Pin # | Symbol | Description |
|-------|--------|-------------|
| 1 | GND | Ground |
| 2 | IN | Logic Level Input |
| 3 | STAT | Status Output |
| 4 | N/C | No Connection |
| 5 | $V_D$ | Supply Voltage |
| 6 | OUT | Output |
| 7 | OUT | Output |
| 8 | $V_D$ | Supply Voltage |

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## MAXIMUM RATINGS

| Rating | Symbol | Value Min | Value Max | Unit |
|---|---|---|---|---|
| DC Supply Voltage | $V_D$ | −16 | 42 | V |
| Peak Transient Input Voltage (Load Dump 51.5 V, $V_D$ = 13.5 V, ISO7637−2 pulse 5) | $V_{peak}$ | | 65 | V |
| Input Voltage | $V_{in}$ | −8 | 8 | V |
| Input Current | $I_{in}$ | −5 | 5 | mA |
| Output Current (Note 2) | $I_{out}$ | −6 | Internally Limited | A |
| Negative Ground Current | $-I_{gnd}$ | −200 | – | mA |
| Status Current | $I_{status}$ | −5 | 5 | mA |
| Power Dissipation Tc = 25°C | $P_{tot}$ | 1.183 | | W |
| Electrostatic Discharge (HBM Model 100 pF / 1500 Ω) Input Status Output $V_D$ | | 4 3.5 5 5 | | DC kV kV kV kV |
| Single Pulse Inductive Load Switching Energy (Note 1) (L = 1.8 mH, $V_{bat}$ = 13.5 V; $I_L$ = 9 A, $T_{Jstart}$ = 150°C | $E_{AS}$ | 100 | | mJ |
| Operating Junction Temperature | $T_J$ | −40 | +150 | °C |
| Storage Temperature | $T_{storage}$ | −55 | +150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1.  Not subjected to production testing
2.  Reverse Output current has to be limited by the load to stay within absolute maximum ratings and thermal performance.


## THERMAL RESISTANCE RATINGS

| Parameter | Symbol | Max Value | Unit |
|---|---|---|---|
| Thermal Resistance Junction−to−Lead Junction−to−Ambient (min. Pad) Junction−to−Ambient (1" square pad size, FR−4, 1 oz Cu) | $R_{\theta JL}$ $R_{\theta JA}$ $R_{\theta JA}$ | 72 110.8 105.6 | °C/W °C/W °C/W |

**ELECTRICAL CHARACTERISTICS** ($8 \leq V_D \leq 36$ V; $-40°C < T_J < 150°C$ unless otherwise specified)

| Rating | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | **Value** | | |
| | | | Min | Typ | Max | Unit |
| Operating Supply Voltage | $V_D$ | | 6 | – | 36 | V |
| Undervoltage Shutdown | $V_{UV}$ | | 3 | 4 | 5.5 | V |
| Undervoltage | $V_{UV\_Rst}$ | | | | 6 | V |
| Overvoltage Shutdown | $V_{OV}$ | | 36 | | | V |
| On Resistance | $R_{ON}$ | $I_{out} = 2$ A; $T_J = 25°C$, $V_D > 6$ V<br>$I_{out} = 2$ A, $V_D > 6$ V | | | 60<br>120 | mΩ |
| Standby Current | $I_D$ | Off State, $V_{in} = V_{out} = 0$ V, $V_D = 13.5$ V<br>On State; $V_{in} = 5$ V, $V_D = 13.5$ V, $I_{out} = 0$ A | | 10<br>1.5 | 20<br>3.5 | μA<br>μA |
| Output Leakage Current | $I_L$ | $V_{in} = V_{out} = 0$ V<br>$V_{in} = 0$ V, $V_{out} = 3.5$ V<br>$V_{in} = V_{out} = 0$ V, $V_D = 13.5$ V | −20 | | 50<br>10<br>3 | μA |

**INPUT CHARACTERISTICS**

| Rating | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Voltage – Low | $V_{in\_low}$ | | | | 1.25 | V |
| Input Current – Low | $I_{in\_low}$ | $V_{in} = 1.25$ V | 1 | | | μA |
| Input Voltage – High | $V_{in\_high}$ | | 3.25 | | | V |
| Input Current – High | $I_{in\_high}$ | $V_{in} = 3.25$ V | | | 10 | μA |
| Input Hysteresis Voltage | $V_{hyst}$ | | 0.25 | | | V |
| Input Clamp Voltage | $V_{in\_cl}$ | $I_{in} = 1$ mA<br>$I_{in} = -1$ mA | 11<br>−13 | 12<br>−12 | 13<br>−11 | V |

**SWITCHING CHARACTERISTICS**

| Rating | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Turn–On Delay Time | $t_{d\_on}$ | to 10% $V_{out}$, $V_D = 13.5$ V, $R_L = 6.5$ Ω | | 40 | | μs |
| Turn–Off Delay Time | $t_{d\_off}$ | to 90% $V_{out}$, $V_D = 13.5$ V, $R_L = 6.5$ Ω | | 30 | | μs |
| Slew Rate On | $dV_{out} / dt_{on}$ | 10% to 80% $V_{out}$, $V_D = 13.5$ V, $R_L = 6.5$ Ω | | 0.9 | | V / μs |
| Slew Rate Off | $dV_{out} / dt_{off}$ | 90% to 10% $V_{out}$, $V_D = 13.5$ V, $R_L = 6.5$ Ω | | 0.7 | | V / μs |

**OUTPUT DIODE CHARACTERISTICS** (Note 3)

| Rating | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Forward Voltage | $V_F$ | $I_{out} = -1.3$ A, $T_J = 150°C$ | | | 0.6 | V |

**STATUS PIN CHARACTERISTICS**

| Rating | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Status Output Voltage Low | $V_{stat\_low}$ | $I_{stat} = 1.6$ mA | | 0.2 | 0.5 | V |
| Status Leakage Current | $I_{stat\_leakage}$ | $V_{stat} = 5$ V | | 1 | 10 | μA |
| Status Pin Input Capacitance | $C_{stat}$ | $V_{stat} = 5$ V (Note 3) | | | 100 | pF |
| Status Clamp Voltage | $V_{stat\_cl}$ | $I_{stat} = 1$ mA<br>$I_{stat} = -1$ mA | 10<br>−2.2 | 11<br>−1.2 | 12<br>−0.6 | V |

**PROTECTION FUNCTIONS** (Note 4)

| Rating | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Temperature Shutdown (Note 3) | $T_{SD}$ | | 150 | 175 | 200 | °C |
| Temperature Shutdown Hysteresis (Note 3) | $T_{SD\_hyst}$ | | 7 | 15 | | °C |
| Output Current Limit | $I_{lim}$ | $8$ V $< V_D < 36$ V | 6 | 9 | 15 | A |
| | | $6$ V $< V_D < 36$ V | 5 | | 15 | A |
| Status Delay in Overload | $t_{d\_stat}$ | | | | 20 | μs |

3. Not subjected to production testing
4. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper hardware/software strategy. If the devices operates under abnormal conditions this hardware/software solutions must limit the duration and number of activation cycles.
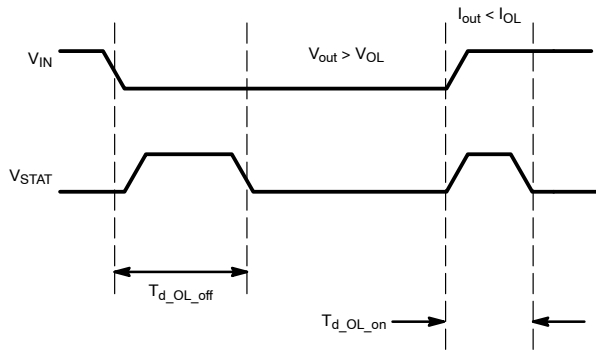
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## ELECTRICAL CHARACTERISTICS ($8 \leq V_D \leq 36$ V; $-40°C < T_J < 150°C$ unless otherwise specified)

| Rating | Symbol | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **PROTECTION FUNCTIONS** (Note 4) | | | | | | |
| Switch Off Output Clamp Voltage | $V_{clamp}$ | $I_{out} = 2$ A, $V_{in} = 0$ V, $L = 6$ mH | $V_D - 41$ | $V_D - 45$ | $V_D - 55$ | V |
| **DIAGNOSTICS CHARACTERISTICS** | | | | | | |
| Openload On State Detection Threshold | $I_{OL}$ | $V_{in} = 5$ V | 30 | | 300 | mA |
| Openload On State Detection Delay | $t_{d\_OL\_on}$ | $I_{out} = 0$ A | | | 200 | µs |
| Openload Off State Detection Threshold | $V_{OL}$ | $V_{in} = 0$ V | 1.5 | – | 3.5 | V |
| Openload Detection Delay at Turn Off | $t_{d\_OL\_off}$ | | | | 1000 | µs |

3. Not subjected to production testing
4. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper hardware/software strategy. If the devices operates under abnormal conditions this hardware/software solutions must limit the duration and number of activation cycles.



**Figure 2. Open Load Status Timing (with external pull−up)**
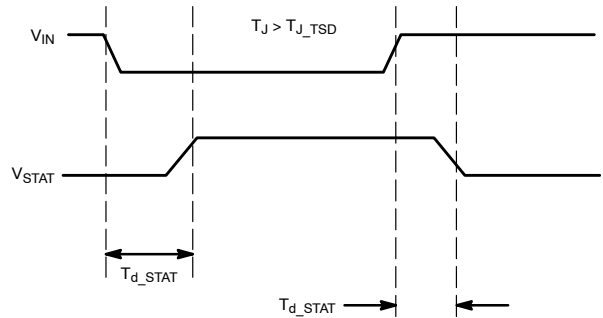


**Figure 3. Overtemperature Status Timing**
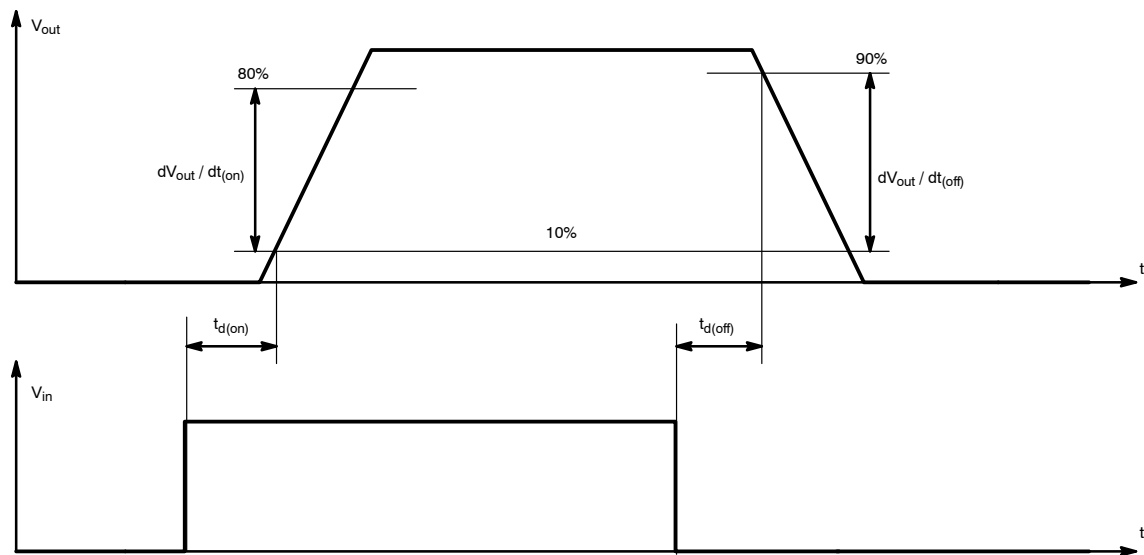


**Figure 4. Switching Timing Diagram**

**STATUS PIN TRUTH TABLE**

| Conditions | Input | Output | Status |
|---|---|---|---|
| Normal Operation | L<br>H | L<br>H | H<br>H |
| Undervoltage | L<br>H | L<br>L | X<br>X |
| Overvoltage | L<br>H | L<br>L | H<br>H |
| Current Limitation | L<br>H<br>H | L<br>X<br>X | H<br>$(T_J < T_{SD})$ H<br>$(T_J > T_{SD})$ L |
| Overtemperature | L<br>H | L<br>L | H<br>L |
| Output Voltage > $V_{OL}$ | L<br>H | H<br>H | L<br>H |
| Output Current < $I_{OL}$ | L<br>H | L<br>H | H<br>L |

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## TYPICAL CHARACTERISTICS CURVES
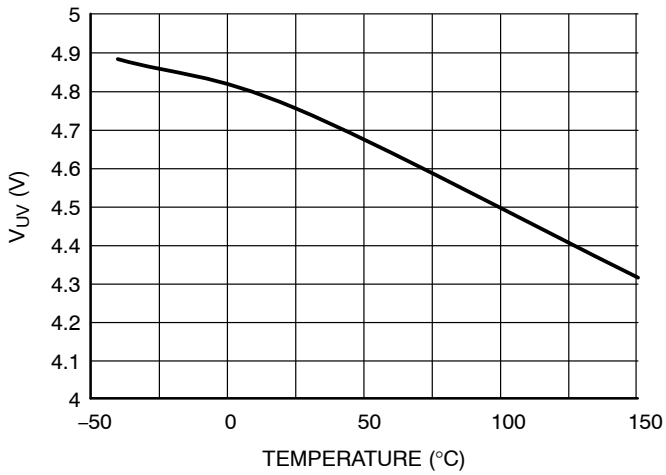
**Figure 5. Undervoltage Shutdown vs. Temperature**
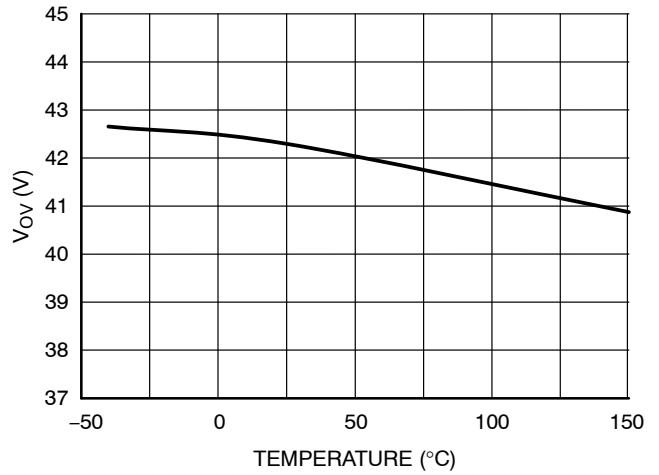
**Figure 6. Overvoltage Shutdown vs. Temperature**
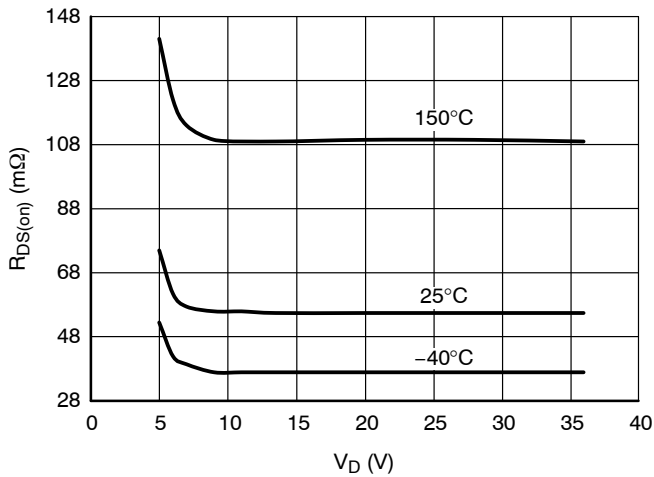
**Figure 7. R$_{DS(on)}$ vs. V$_D$**
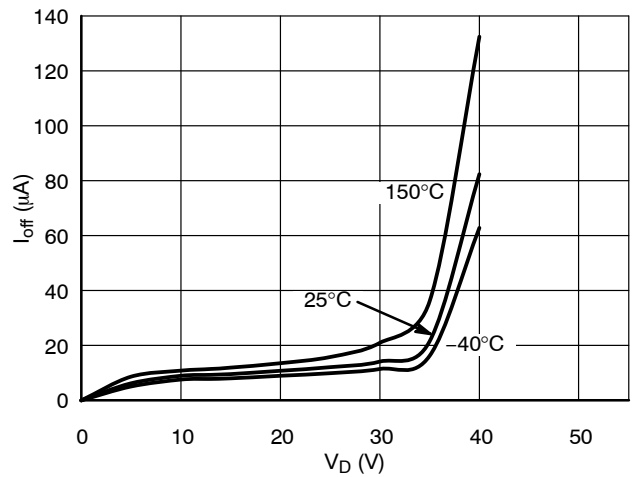
**Figure 8. OFF State Standby Current vs. V$_D$**
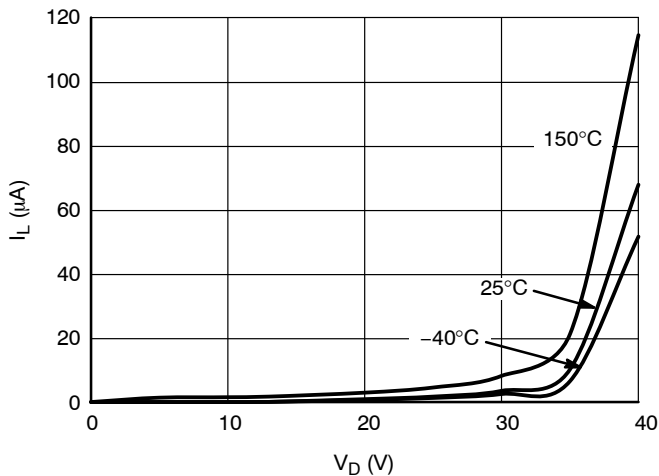
**Figure 9. Output Leakage vs. V$_D$ V$_{out}$ = 0 V**
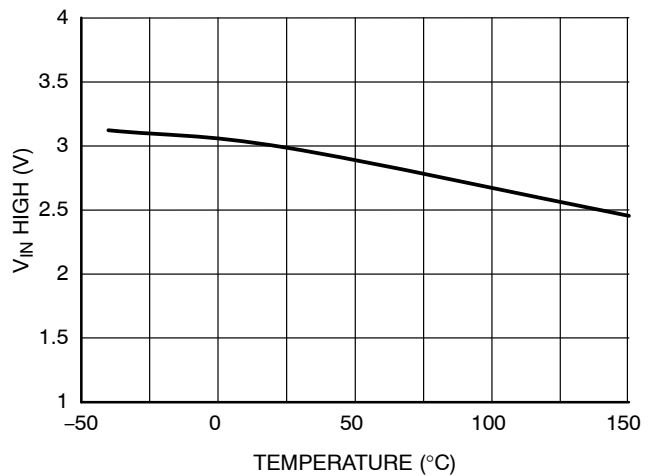
**Figure 10. V$_{in}$ Threshold High vs. Temperature**

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## TYPICAL CHARACTERISTICS CURVES



**Figure 11. V$_{in}$ Threshold Low vs. Temperature**
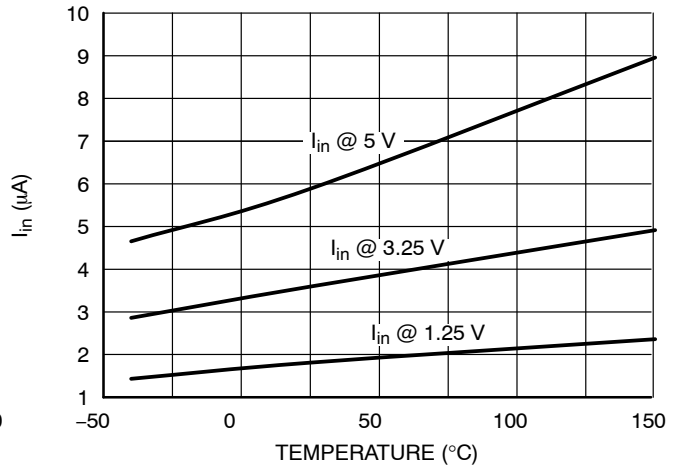


**Figure 12. Input Current vs. Temperature**
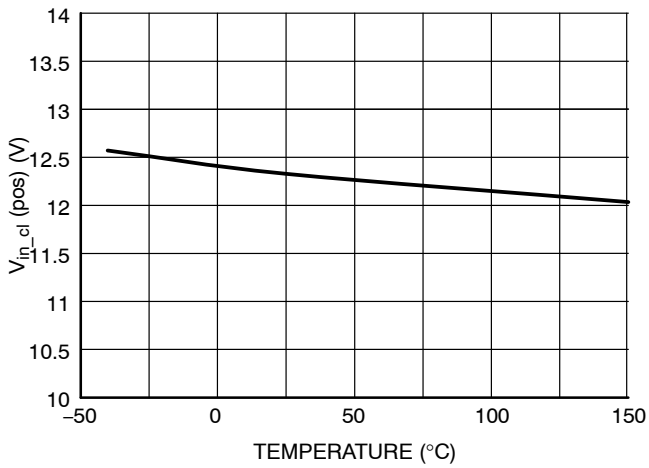


**Figure 13. Input Clamp Voltage (Positive) vs. Temperature**
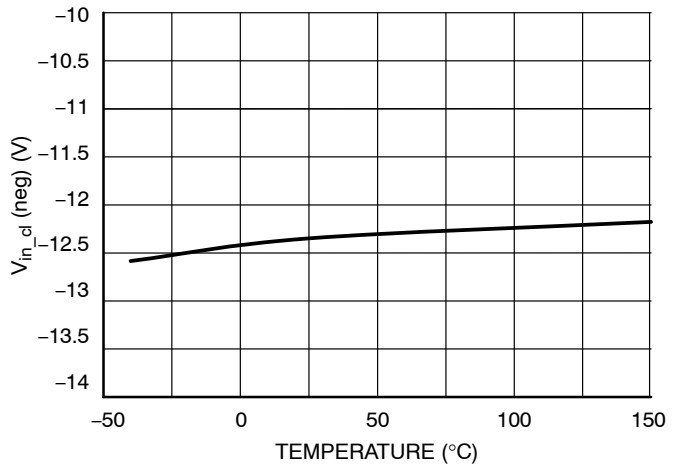


**Figure 14. Input Clamp Voltage (Negative) vs. Temperature**
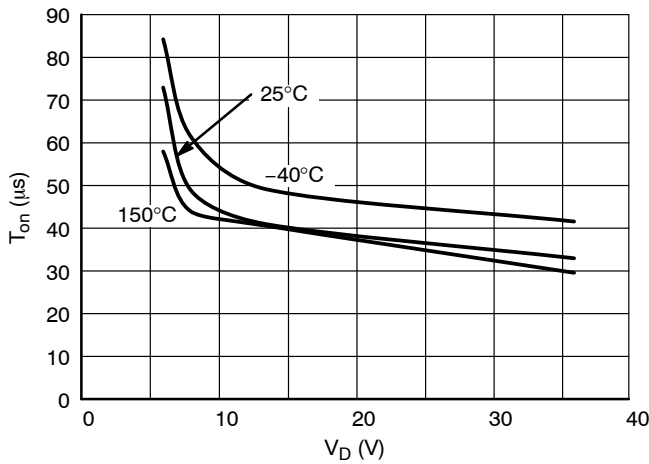


**Figure 15. Turn On Time vs. V$_D$**
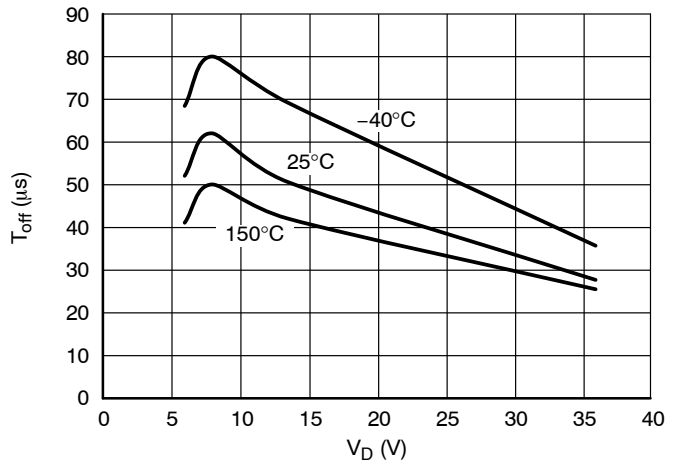


**Figure 16. Turn Off Time vs. V$_D$**

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## TYPICAL CHARACTERISTICS CURVES
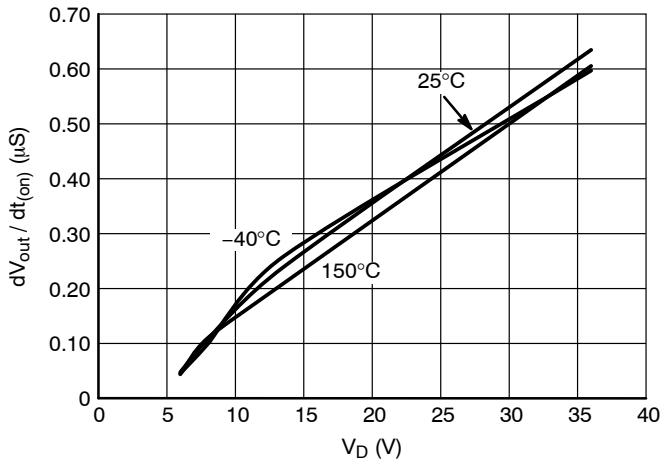


**Figure 17. Slew Rate ON vs. $V_D$**
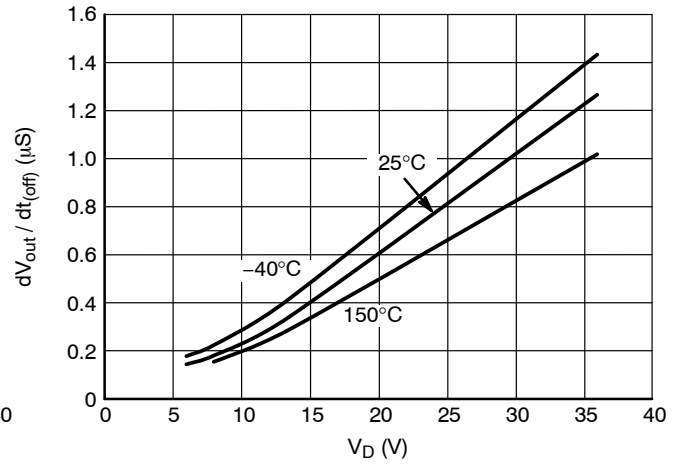


**Figure 18. Slew Rate OFF vs. $V_D$**
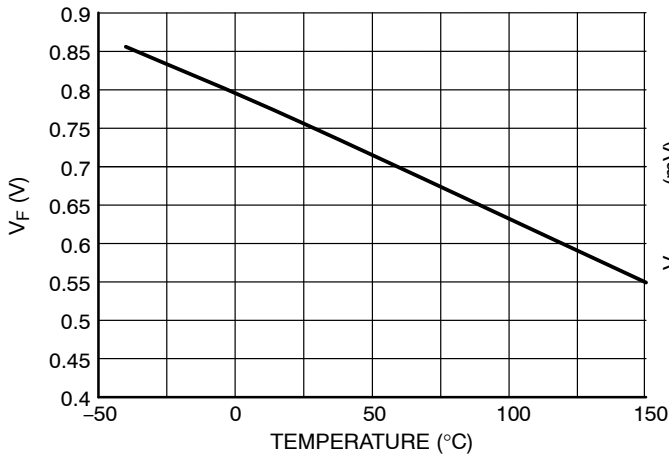


**Figure 19. Forward Voltage (@ −1.3 A) vs. Temperature**
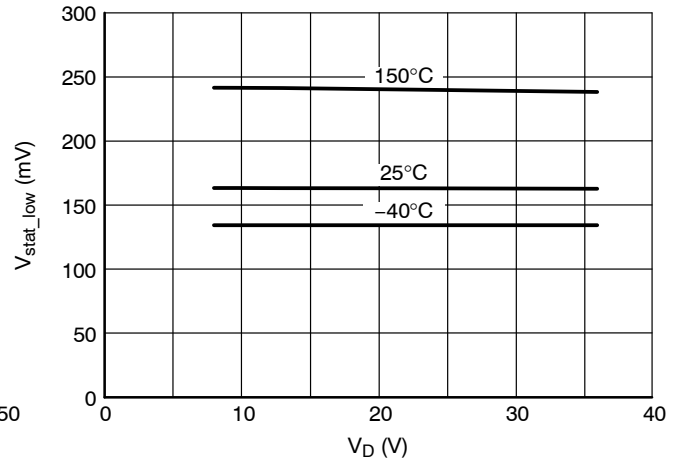


**Figure 20. STAT Low Voltage vs. $V_D$**
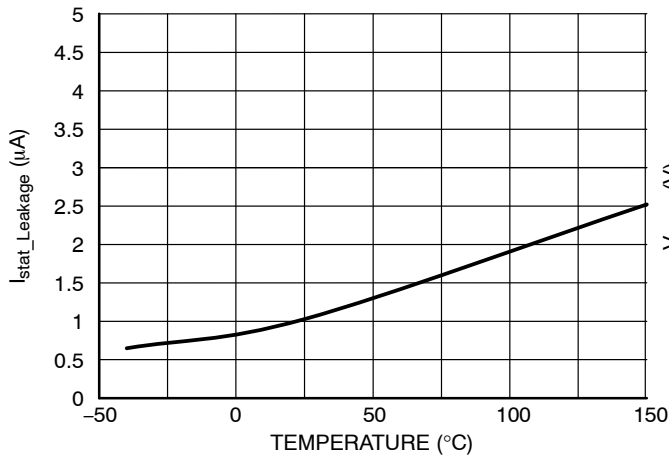


**Figure 21. Status Leakage Current vs. Temperature**
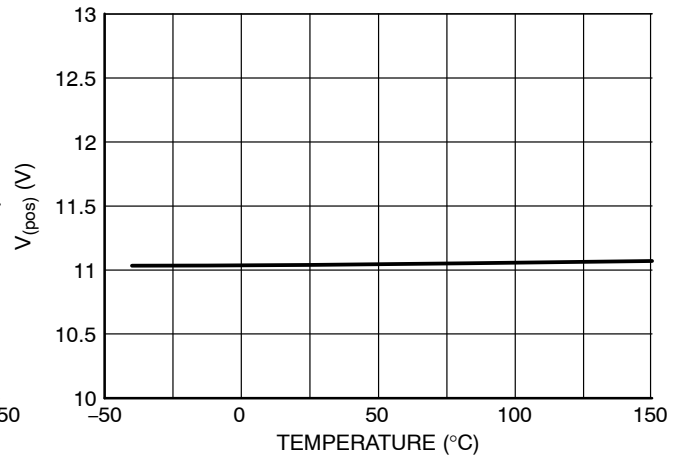


**Figure 22. Status Clamp Voltage (Positive) vs. Temperature**

## TYPICAL CHARACTERISTICS CURVES
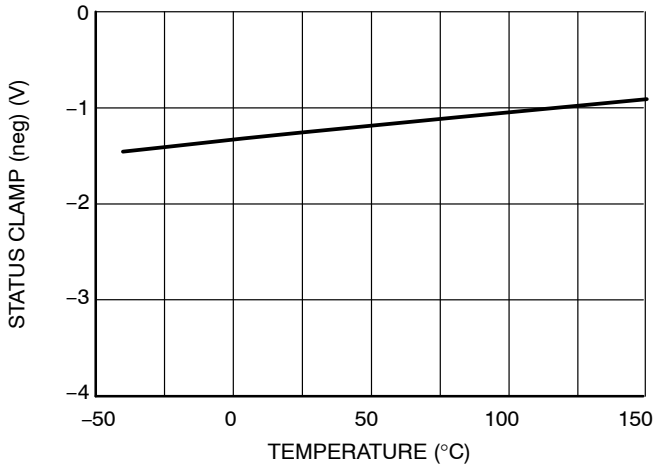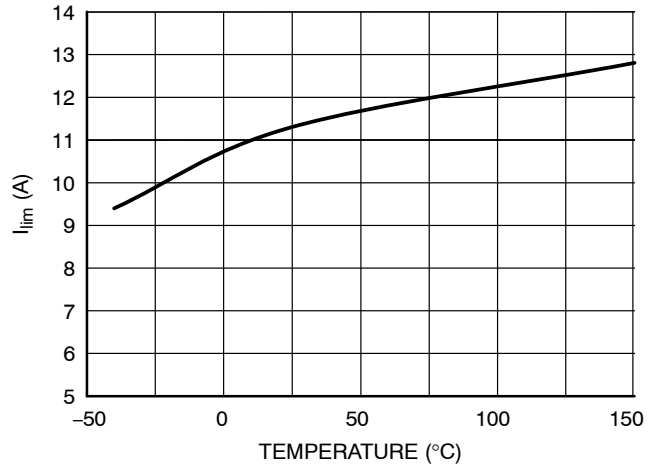


**Figure 23. Status Clamp Voltage (Negative) vs. Temperature**



**Figure 24. Current Limit vs. Temperature**
$V_D = 13.5$ V
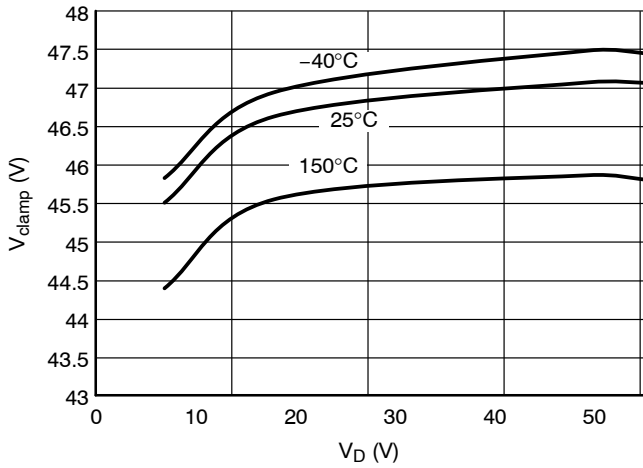


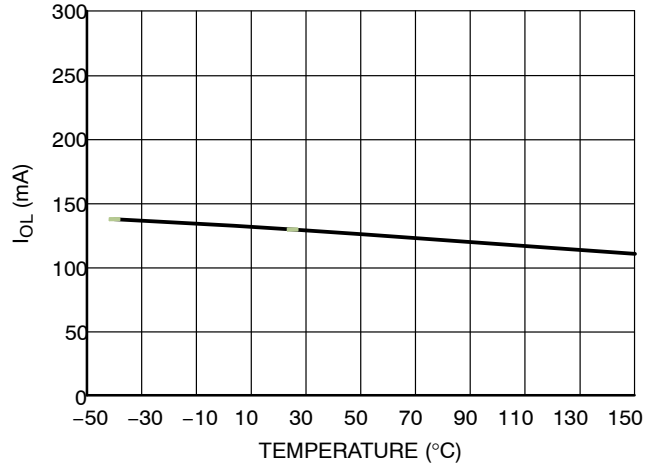**Figure 25. Turn Off Output Clamp Voltage vs. $V_D$ and Temperature**



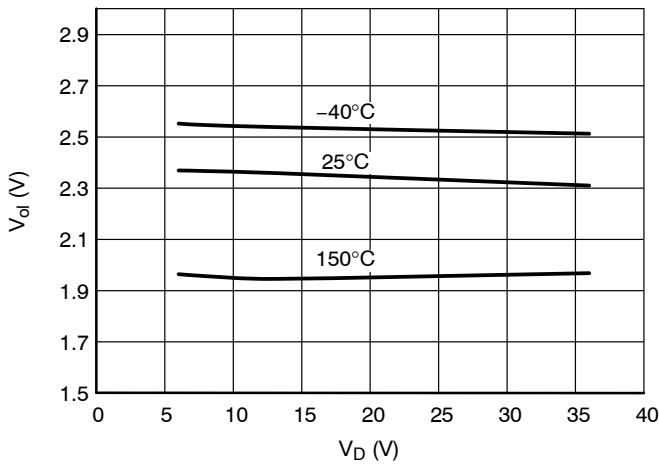**Figure 26. ON State Open Load Detection vs. Temperature $V_D = 13.5$ V**



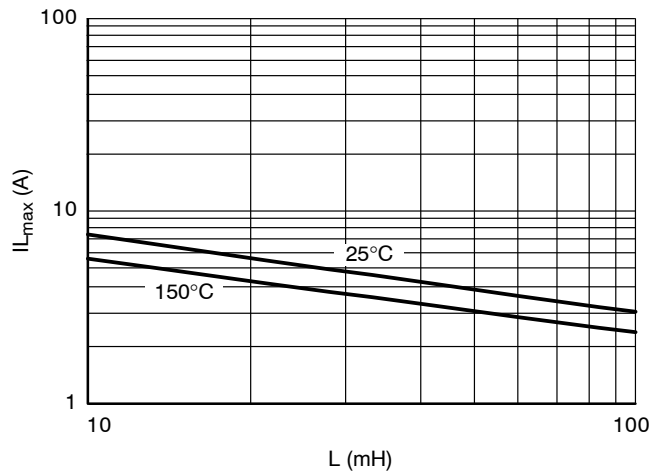**Figure 27. Off State OL Detection Threshold vs. $V_D$ and Temperature**



**Figure 28. Single−Pulse Maximum Switch−off Current vs. Load Inductance**

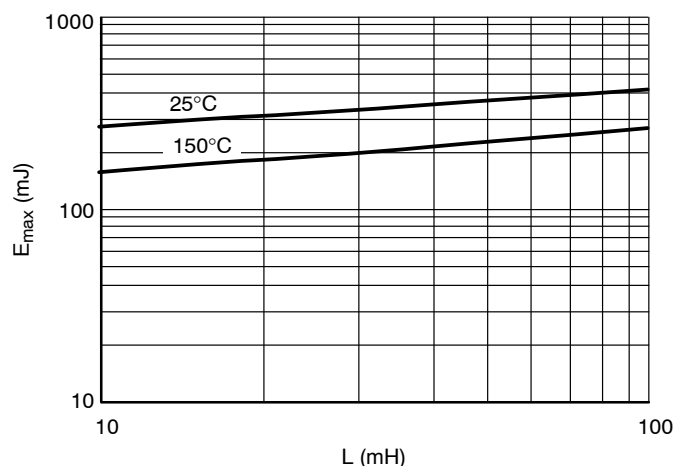## TYPICAL CHARACTERISTICS CURVES



**Figure 29. Single−Pulse Maximum Switch−off
Current vs. Load Inductance**

## ISO 7637−2: 2004(E) PULSE TEST RESULTS

| ISO 7637−2:2004(E) | Test Levels | | | | Delays and |
|---|---|---|---|---|---|
| **Test Pulse** | **I** | **II** | **III** | **IV** | **Impedance** |
| 1 | g | g | −75 V | −100 V | 2 ms, 10 Ω |
| 2a | g | g | +37 V | +50 V | 0.05 ms, 10 Ω |
| 3a | g | g | −112 V | −150 V | 0.1 μs, 50 Ω |
| 3b | g | g | +75 V | +100 V | 0.1 μs, 50 Ω |
| 4 | g | g | −6 V | −7 V | 5 s, .01 Ω |
| 5 (Load Dump) | g | g | +65 V | +87 V | 400 ms, 2 Ω |

| ISO 7637−2:2004(E) | Test Results | | | |
|---|---|---|---|---|
| **Test Pulse** | **I** | **II** | **III** | **IV** |
| 1 | | | C | C |
| 2a | | | C | C |
| 3a | | | C | C |
| 3b | | | C | C |
| 4 | | | A | A |
| 5 (Load Dump) | | | C | E |

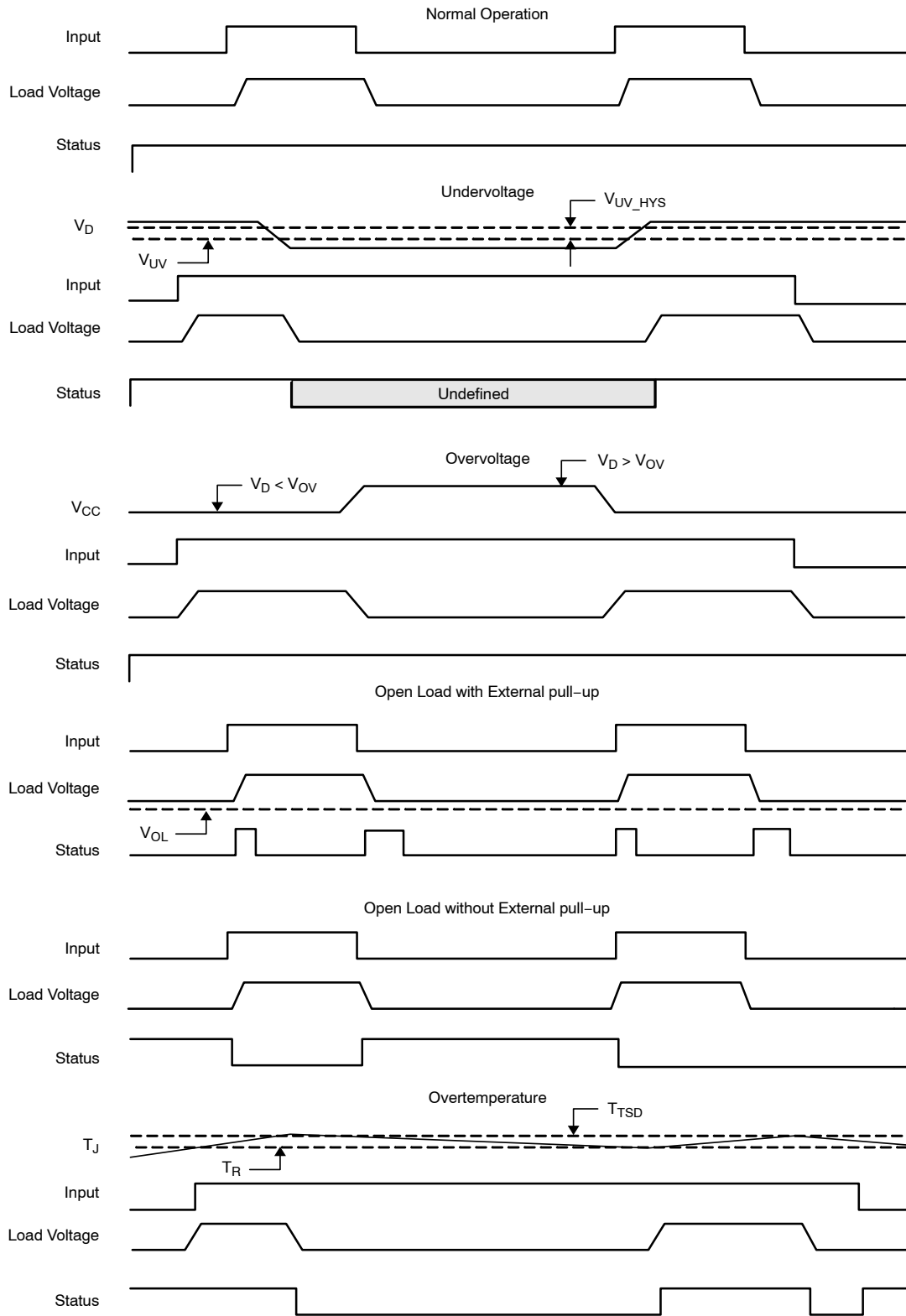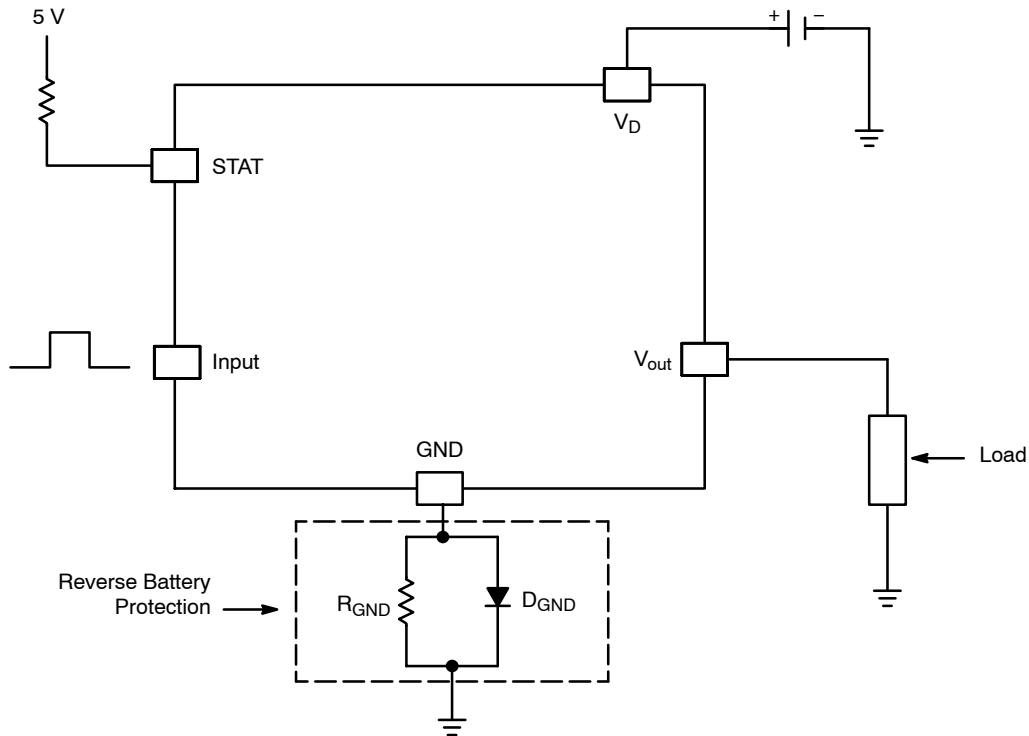| Class | Functional Status |
|---|---|
| A | All functions of a device perform as designed during and after exposure to disturbance. |
| B | All functions of a device perform as designed during exposure. However,one or more of them can go beyond specified tolerance. All functions return automatically to within normal limits after exposure is removed. Memory functions shall remain class A. |
| C | One or more functions of a device do not perform as designed during exposure but return automatically to normal operation after exposure is removed. |
| D | One or more functions of a device do not perform as designed during exposure and do  not return to normal operation until exposure is removed and the device is reset by simple |
| E | One or more functions of a device do not perform as designed during and after exposure and cannot be returned to proper operation without replacing the device. |

# NCV8460

Normal Operation

Input

Load Voltage

Status

Undervoltage

$V_D$ — $V_{UV\_HYS}$

$V_{UV}$

Input

Load Voltage

Status — Undefined

Overvoltage — $V_D > V_{OV}$

$V_D < V_{OV}$

$V_{CC}$

Input

Load Voltage

Status

Open Load with External pull−up

Input

Load Voltage

$V_{OL}$

Status

Open Load without External pull−up

Input

Load Voltage

Status

Overtemperature — $T_{TSD}$

$T_J$

$T_R$

Input

Load Voltage

Status

**Figure 30. Waveforms**

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**Figure 31. Application Diagram**

## Reverse Battery Protection

An external resistor $R_{GND}$ is required to adequately protect the device from a Reverse Battery event. The resistor value can be calculated using the following two formulas.

1. $R_{GND} \geq 600 \text{ mV} / (I_d \text{ (on) max})$
2. $R_{GND} \geq (-V_D) / (-I_{gnd})$

Maximum $(-I_{gnd})$ current, which is the reverse GND pin current, can be found in the Maximum Ratings section. Several High Side Devices can share same the reverse battery protection resistor. Please note that the sum of $(I_d$ (on) max) of all devices should be used to calculate $R_{GND}$ value. If the microprocessor ground is not common with the device ground, $R_{GND}$ will produce a voltage offset $((I_d$ (on) max) x $R_{GND})$ with respect to the IN and STAT pins.

This offset will be increased when more than one device shares the resistor.

Power Dissipation during a reverse battery event is equal to:

$$P_D = \left( -V_D \right)^2 / R_{GND}$$

In the case of high power dissipation due to several devices sharing $R_{GND}$, it is recommended to place a diode $D_{GND}$ in the ground path as an alternate reverse battery protection method. When driving an inductive load, a 1 kΩ resistor should be placed in parallel with the $D_{GND}$ diode. This method will also produce a voltage offset of ~600 mV with respect to the IN and STAT pins. This diode can also be shared amongst several High Side Devices. This voltage offset will vary if $D_{GND}$ is shared by multiple devices.
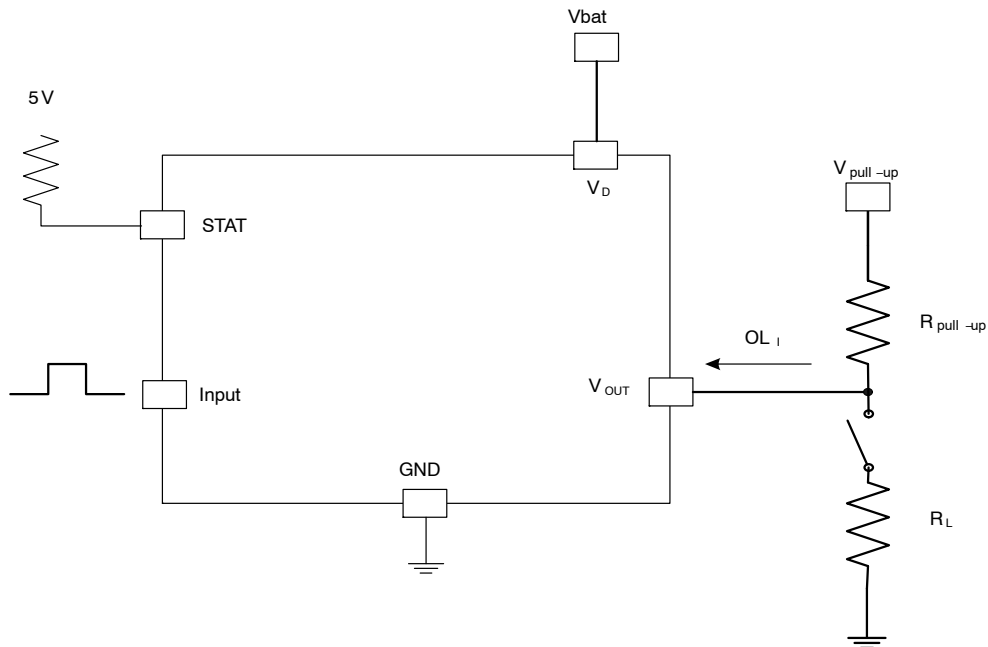
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**Figure 32. Open Load Detection In Off State**

**OFF State Open Load Detection**

Off State Open Load Detection requires an external pull-up resistor ($R_{pull\text{-}up}$) connected between $V_{OUT}$ pin and a positive supply voltage ($V_{pull\text{-}up}$).

The external $R_{pull\text{-}up}$ resistor value should be selected to ensure that a false OFF State OL condition is not detected when the load ($R_L$) is connected. A $V_{OUT}$ voltage above the $V_{OL\_min}$ (Openload Off State Detection Threshold) minimum value with the load ($R_L$) connected needs to be avoided. The following formula shows this relationship:

$$V_{OUT} = \left(V_{pull-up}/\left(R_L + R_{pull-up}\right)\right) R_L < V_{OL\_min}$$

In addition to ensuring the selected $R_{pull\text{-}up}$ resistor value does not cause a false OFF State OL detection condition

when the load is connected, the $R_{pull\text{-}up}$ must also not cause the OFF State OL to miss detecting an OL condition when the load is disconnected. A $V_{OUT}$ voltage below the $V_{OL\_max}$ (Openload Off State Detection Threshold) maximum value with the load ($R_L$) disconnected needs to be avoided. The following formula shows this relationship:

$$R_{pull-up} < \left(V_{pull-up} - V_{OL\_max}\right)/OL_1$$

$$OL_1 = I_L\left(\text{Output Leakage with } V_{OUT} = 3.5\text{ V}\right)$$

Because $I_d$ (OFF) may significantly increase if $V_{OUT}$ is pulled high (up to several mA), $R_{pull\text{-}up}$ resistor should be connected to a supply that is switched OFF when the module is in standby.

# NCV8460
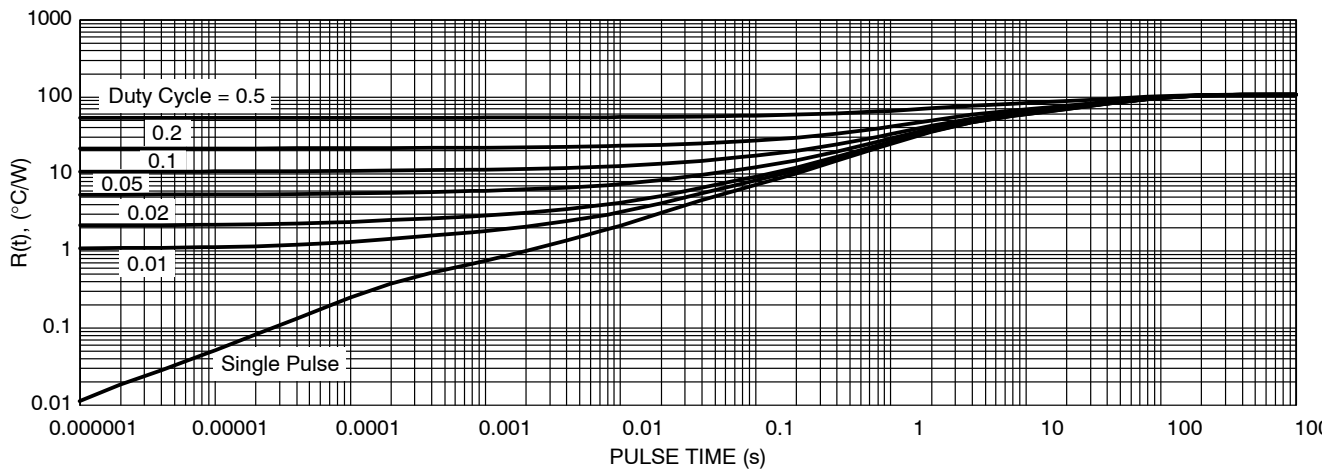
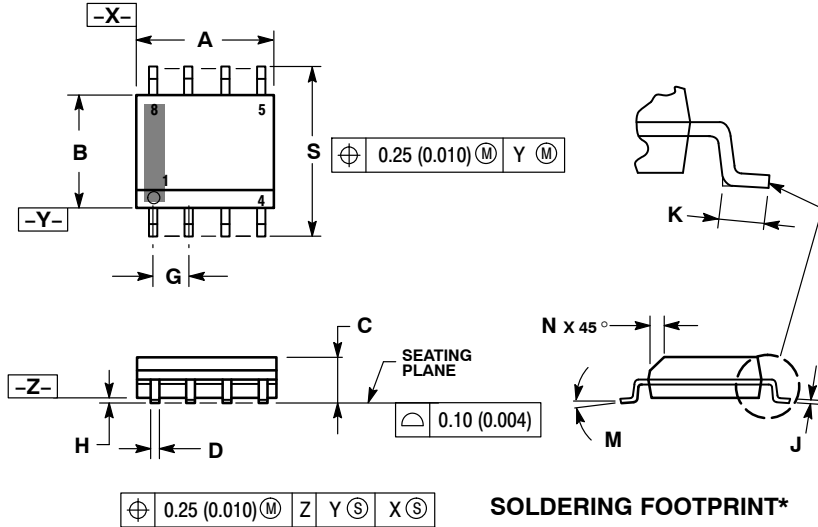

**Figure 33. Transient Thermal Impedance**
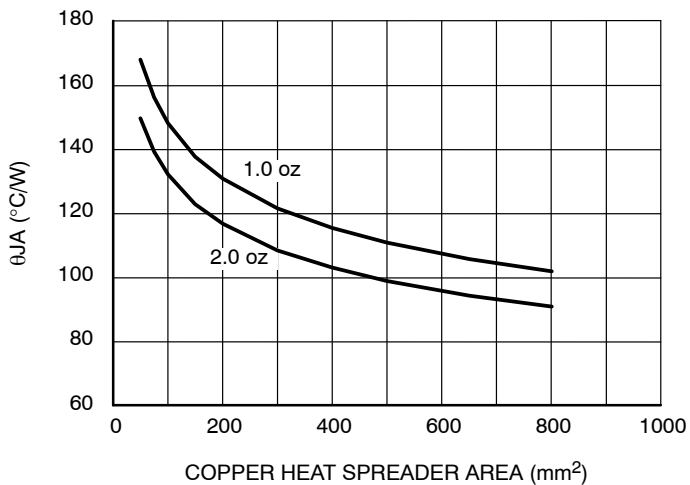


**Figure 34. R$_{\theta JA}$ vs Copper Area**

# NCV8460

## PACKAGE DIMENSIONS
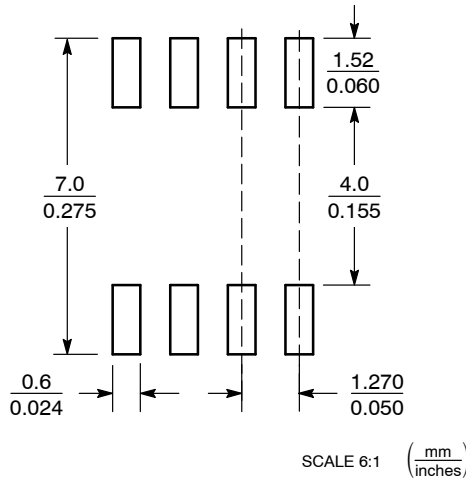
**SOIC−8 NB**
CASE 751−07
ISSUE AK

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0 ° | 8 ° | 0 ° | 8 ° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

0.25 (0.010) Ⓜ Y Ⓜ

0.25 (0.010) Ⓜ Z Y Ⓢ X Ⓢ

SEATING PLANE

0.10 (0.004)

N X 45 °

**SOLDERING FOOTPRINT\***

1.52 / 0.060

7.0 / 0.275

4.0 / 0.155

0.6 / 0.024

1.270 / 0.050

SCALE 6:1  (mm / inches)

\*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**NCV8460/D**