

# SANYO Semiconductors DATA SHEET

An ON Semiconductor Company

# LV5681P — Monolithic Linear IC For Car Audio Systems Multi-Power Supply System IC

#### Overview

The LV5681P is a multi-power supply system IC that provides four regulator outputs and two high side switches as well as a number of protection functions including overcurrent protection, overvoltage protection and overheat protection. It is an optimal power supply IC for car audio and car entertainment systems and similar products.

#### **Features**

• Four regulator output systems

For microcontroller: 5.7V output voltage, 200mA maximum output current

For CD drive: 7.0V output voltage, 1300mA maximum output current

For illumination: 8 to 12V output voltage (output can be set with external resistors), 300mA maximum output current For audio systems: 8 to 9V output voltage (output voltage can be set with external resistors), 300mA maximum output current

• Two V<sub>CC</sub>-linked high side switch systems

EXT: 350mA maximum output current, 0.5V voltage difference between input and output.

ANT: 300mA maximum output current, 0.5V voltage difference between input and output.

• Two VDD 5V-linked high side switch systems

SW5V: 200mA maximum output current, 0.2V voltage difference between input and output.

ACC (accessory voltage detection output): 100mA maximum output current, 0.2V voltage difference between input and output.

- Overcurrent protection function
- Overvoltage protection function, typ 21V (excluding V<sub>DD</sub> 5V output)
- Overheat protection function, typ 175°C
- On-chip accessory voltage detection circuit
- P-channel LDMOS used for power output block

#### CAUTION)

The protection functions are provided in order to improve the ability of the ICs to withstand breakdown, and they are not intended to guarantee safety when used under conditions outside the safe operating area or rated operating conditions.

Use of the ICs under any conditions exceeding the safe operating area or above the IOmax, and especially use in overcurrent protection areas or under conditions in which they are subject to thermal protection, may reduce their reliability and result in permanent breakdown.

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# **Specifications**

# **Absolute Maximum Ratings** at Ta = 25°C

Parameter	Conditions	Conditions		Ratings	Unit
Supply voltage	V <sub>CC</sub> max			36	V
Peak supply voltage	V <sub>CC</sub> peak	See below for the waveform applied.		50	V
Allowable Power dissipation	Pd max	Independent IC	Ta ≤ 25°C	1.5	W
		Al heat sink *		5.6	W
		With an infinity heat sink		32.5	W
Junction temperature	Tj max			150	°C
Operating ambient temperature	Topr			-40 to +85	°C
Storage temperature	Tstg			-55 to +150	°C

<sup>\* :</sup> When the Aluminum heat sink (50mm  $\times$  50mm  $\times$  1.5mm) is used

# Allowable Operating range at Ta = 25°C

Parameter	Conditions	Ratings	Unit
Operating supply voltage 1	V <sub>DD</sub> output, SW output, ACC output	7.5 to 16	V
Operating supply voltage 2	ILM output at 10V	12 to 16	V
	ILM output at 8V	10 to 16	V
Operating supply voltage 3	Audio output at 9V	10 to 16	V
Operating supply voltage 4	CD output (CD output current = 1.3A)	10.5 to 16	V
	CD output (CD output current ≤ 1A)	10 to 16	V

# **Electrical Characteristics** at Ta = 25°C, $V_{CC} = 14.4$ V

\*: All the specifications are defined based on the tests that Tj is almost equal to Ta (=25°C). To suppress the rise of Tj in the junction temperature as much as possible, it tests by the pulse loading.

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Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain	Icc	$V_{DD}$ no load, CTRL1/2 = $\lceil L/L \rfloor$ , ACC = 0V		400	800	μΑ
CTRL1 Input						
Low input voltage	V <sub>IL</sub> 1		0		0.4	V
M1 input voltage	V <sub>IM1</sub> 1		0.8	1.1	1.4	V
M2 input voltage	V <sub>IM2</sub> 1		1.9	2.2	2.5	V
High input voltage	V <sub>IH</sub> 1		2.9	3.3	5.5	V
Input impedance	R <sub>IH</sub> 1		350	500	650	kΩ
CTRL2 Input				<u> </u>		
Low input voltage	V <sub>IL</sub> 2		0		0.5	V
M input voltage	V <sub>IM</sub> 2		1.1	1.65	2.1	V
High input voltage	V <sub>IH</sub> 2		2.5	3.3	5.5	V
Input impedance	R <sub>IH</sub> 2		350	500	650	kΩ
V <sub>DD</sub> 5.7V Output *1		The V <sub>DD</sub> 5.7V output supplie	es the output c	urrents of SV	V 5.7V and A	CC 5.7V.
Output voltage 1	V <sub>O</sub> 1	I <sub>O</sub> 1 = 200mA, I <sub>O</sub> 7, I <sub>O</sub> 8 = 0A	5.4	5.7	6.0	V
Output voltage 2	V <sub>O</sub> 1'	I <sub>O</sub> 1 = 200mA, I <sub>O</sub> 7 = 200mA, I <sub>O</sub> 8 = 100mA	5.4	5.7	6.0	V
Output total current	Ito1	$V_{O}1 \ge 5.4V$ , $Ito1 = I_{O}1 + I_{O}7 + I_{O}8$	500			mA
Line regulation	ΔV <sub>OLN</sub> 1	7.5V < V <sub>CC</sub> < 16V, I <sub>O</sub> 1 = 200mA *2		30	90	mV
Load regulation	ΔV <sub>OLD</sub> 1	1mA < I <sub>O</sub> 1 < 200mA *2		70	150	mV
Dropout voltage 1	V <sub>DROP</sub> 1	I <sub>O</sub> 1 = 200mA *2		1.0	1.5	V
Dropout voltage 2	V <sub>DROP</sub> 1'	I <sub>O</sub> 1 = 100mA *2		0.7	1.05	V
Dropout voltage 3	V <sub>DROP</sub> 1"	I <sub>O</sub> 1+I <sub>O</sub> 7+I <sub>O</sub> 8 = 500mA		2.5	3.75	V
Ripple rejection	R <sub>REJ</sub> 1	f = 120Hz, I <sub>O</sub> 1 = 200mA *2	40	50		dB
CD Output ; CTRL2 = H	•	•		1.		
Output voltage	V <sub>O</sub> 2	I <sub>O</sub> 2 = 1000mA	6.65	7.0	7.35	V

<sup>\*1 :</sup> The  $V_{DD}$  5.7V output also supplies the output currents of SW 5.7V and ACC 5.7V. Therefore, the current supply capability of the  $V_{DD}$  5.7V output and its other electrical characteristics are affected by the output statuses of SW 5.7V and ACC 5.7V.

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 $<sup>^{*}2</sup>$  : SW 5V and ACC 5.7V are not subject to a load.

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Continued	from	preceding	nage

Parameter	Symbol	Conditions		Ratings		Unit
			min	typ	max	
Output current	I <sub>O</sub> 2	V <sub>O</sub> 2 ≥ 6.65V	1300			mA
Line regulation	ΔV <sub>OLN</sub> 2	10.5V < V <sub>CC</sub> < 16V, I <sub>O</sub> 2 = 1000mA		50	100	mV
Load regulation	∆V <sub>OLD</sub> 2	10mA < I <sub>O</sub> 2 < 1000mA		100	200	mV
Dropout voltage 1	V <sub>DROP</sub> 2	I <sub>O</sub> 2 = 1000mA		1.0	1.5	V
Dropout voltage 2	V <sub>DROP2</sub> '	I <sub>O</sub> 2 = 500mA		0.5	0.75	V
Ripple rejection	R <sub>REJ</sub> 2	f = 120Hz, I <sub>O</sub> 2 = 1000mA	40	50		dB
AUDIO (8-9V) Output ; CTRL2	= [M]	<b>,</b>				
AUDIO_F pin voltage	V <sub>I</sub> 3		1.222	1.260	1.298	V
AUDIO_F pin inflow current	I <sub>IN</sub> 3		-1		1	μΑ
AUDIO output voltage 1	V <sub>O</sub> 3	$I_{O}3 = 200 \text{mA}, R2 = 30 \text{k}\Omega, R3 = 5.6 \text{k}\Omega *3$	7.65	8.0	8.35	V
AUDIO output voltage 2	V <sub>O</sub> 3'	$I_{O}3' = 200\text{mA}, R2 = 27\text{k}\Omega, R3 = 4.7\text{k}\Omega *3$	8.13	8.5	8.87	V
AUDIO output voltage 3	V <sub>O</sub> 3"	$I_{O}3$ " = 200mA, R2 = 24k $\Omega$ , R3 = 3.9k $\Omega$ *3	8.6	9.0	9.4	V
AUDIO output current	I <sub>O</sub> 3		300			mA
Line regulation	ΔV <sub>OLN</sub> 3	10V < V <sub>CC</sub> < 16V, I <sub>O</sub> 3 = 200mA		30	90	mV
Load regulation	ΔV <sub>OLD</sub> 3	1mA < I <sub>O</sub> 3 < 200mA		70	150	mV
Dropout voltage 1	V <sub>DROP</sub> 3	I <sub>O</sub> 3 = 200mA		0.3	0.45	V
Dropout voltage 2	V <sub>DROP</sub> 3'	I <sub>O</sub> 3 = 100mA		0.15	0.23	V
Ripple rejection	R <sub>REJ</sub> 3	f = 120Hz, I <sub>O</sub> 3 = 200mA	40	50		dB
ILM (8-12V) Output ; CTRL1 =	M1				•	
ILM_F pin voltage	V <sub>I</sub> 4		1.222	1.260	1.298	V
ILM output voltage 1	V <sub>O</sub> 4	$I_{O}4 = 200$ mA, R2 = $30$ k $\Omega$ , R3 = $5.6$ k $\Omega$ *3	7.65	8.0	8.35	V
ILM output voltage 2	V <sub>O</sub> 4'	$I_04' = 200$ mA, R2 = $27$ k $\Omega$ , R3 = $3.9$ k $\Omega$ *3	9.55	10.0	10.45	V
ILM output voltage 3	V <sub>O</sub> 4"	$I_04$ " = 200mA, R2 = 33k $\Omega$ , R3 = 3.9k $\Omega$ *3	11.36	11.9	12.44	V
ILM output current	I <sub>O</sub> 4		300			mA
Line regulation	∆V <sub>OLN</sub> 4	12V < V <sub>CC</sub> < 16V, I <sub>O</sub> 4 = 200mA		30	90	mV
Load regulation	∆V <sub>OLD</sub> 4	1mA < I <sub>O</sub> 4 < 200mA		70	150	mV
Dropout voltage 1	V <sub>DROP</sub> 4	I <sub>O</sub> 4 = 200mA		0.7	1.05	V
Dropout voltage 2	V <sub>DROP4</sub> '	I <sub>O</sub> 4 = 100mA		0.35	0.53	V
Ripple rejection	R <sub>REJ</sub> 4	f = 120Hz, I <sub>O</sub> 4 = 200mA	40	50		dB
Remoto (EXT) ; CTRL1 = M2		-	l.	<u> </u>	<u> </u>	
Output voltage	V <sub>O</sub> 5	I <sub>O</sub> 5 = 350mA	V <sub>CC</sub> -1.0	V <sub>CC</sub> -0.5		V
Output current	I <sub>O</sub> 5	V <sub>O</sub> 5 ≥ V <sub>CC</sub> -1.0	350			mA
ANT remoto ; CTRL1 = H		1 2 22				
Output voltage	V <sub>O</sub> 6	I <sub>O</sub> 6 = 300mA	V <sub>CC</sub> -1.0	V <sub>CC</sub> -0.5		V
Output current	106	V <sub>O</sub> 6 ≥ V <sub>CC</sub> -1.0	300			mA
SW 5V Output ; CTRL2 = M		1 3 33				
Output voltage 1	V <sub>O</sub> 7	I <sub>O</sub> 7 = 1mA, I <sub>O</sub> 1, I <sub>O</sub> 8 = 0A *4	V <sub>O</sub> 1-0.25	V <sub>O</sub> 1		V
Output voltage 2	V <sub>O</sub> 7'	I <sub>O</sub> 7 = 200mA, I <sub>O</sub> 1, I <sub>O</sub> 8 = 0A *4	V <sub>O</sub> 1-0.45	V <sub>O</sub> 1-0.2		V
Output current	107	V <sub>O</sub> 7 ≥ 4.55	200			mA
ACC Detection ; ACC Integrati		-	I.	L		
ACC detection voltage	V <sub>TH</sub> 8		2.75	3.0	3.25	V
Hysteresis width	V <sub>HIS</sub> 8		0.2	0.3	0.4	V
Input impedance	ZI8	(Pull-down resistance internal)	42	60	78	kΩ
ACC output voltage 1	V <sub>O</sub> 8	I <sub>O</sub> 8 = 0.5mA, I <sub>O</sub> 1, I <sub>O</sub> 7 = 0A *4	V <sub>O</sub> 1-0.25	V <sub>O</sub> 1		V
ACC output voltage 2	AO8,	I <sub>O</sub> 8 = 100mA, I <sub>O</sub> 1, I <sub>O</sub> 7 = 0A *4	V <sub>O</sub> 1-0.45	V <sub>O</sub> 1-0.2		

<sup>\*3 :</sup> When a component with a resistance accuracy of  $\pm 1\%$  is used

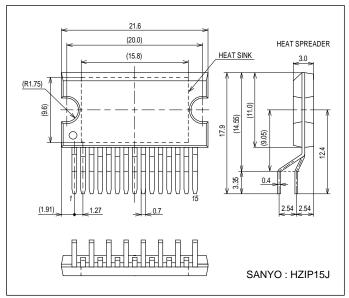
<sup>&</sup>lt;Reference> When a component with a resistance accuracy of  $\pm 0.5\%$  is used,  $V_03"$  is  $8.67V \le 9.0V \le 9.33V$ .

<sup>\*4 :</sup> Since the SW 5.7V and ACC 5.7V are output from V<sub>DD</sub> 5.7V through the SW, the voltage drops by an amount equivalent to the ON resistance of the SW.

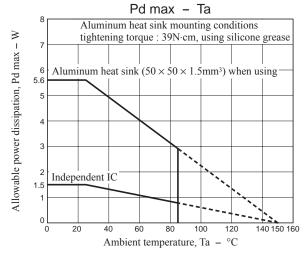
# **Package Dimensions**

unit: mm (typ)

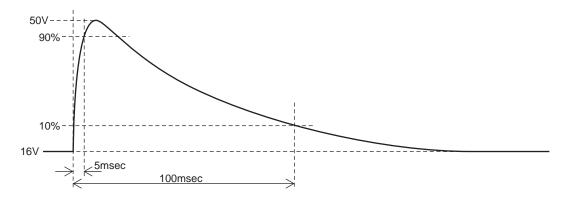
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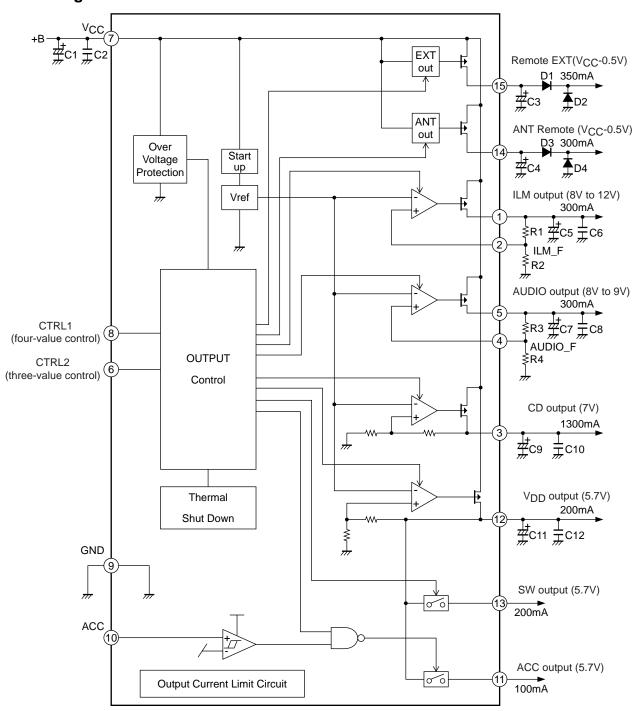
• Allowable power dissipation derating curve



• Waveform applied during surge test



# **Block Diagram**



#### Pin Function

	IIICUOII		
Pin No.	Pin name	Description	Equivalent Circuit
1	ILM	ILM output pin ON when CTRL1 = M1, M2, H 8.0 to12.0V/300mA	7 VCC VCC XX
2	ILM_F	ILM output voltage adjustment pin	2

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Continued from preceding page. Pin No. Pin name Description Equivalent Circuit CD 3 CD output pin Vcc ON when CTRL2 = M, H7.0V/1.3A (3) ↓ ≨182kΩ ] . \$40kΩ (9) GND 4 AUDIO\_F AUIDO output voltage adjustment pin (7)VCC AUDIO 5 AUDIO output pin ON when CTRL2 = M, H 8.0 to 9.0V/300mA 9 GND CTRL2 6 CTRL2 input pin (7)VCC three-value input (6) GND 7 Supply terminal  $^{\text{VCC}}$ 8 CTRL1 CTRL1 input pin -Vcc four-value input GND 9 GND GND pin

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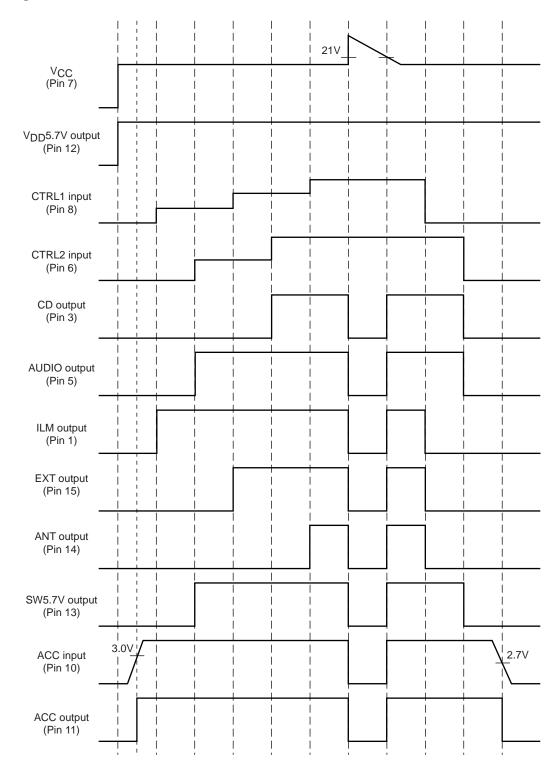
Pin No.	rom preceding pa	Description	Equivalent Circuit
10	ACC	Accessory input	₹ Vcc
			45kΩ 10 45kΩ 15kΩ 9 GND
11	ACC5V	Accessory detection output ON when ACC > 3V	7 Vcc
12	V <sub>DD</sub> 5V	V <sub>DD</sub> 5.7V output pin 5.7V/500mA	12 Δ Δ 9H: 205kΩ 1 11)
13	SW5V	SW5.7V output pin ON when CTRL2 = M, H	13 Σ 50kΩ 50kΩ 125kΩ GND
14	ANT	ANT output pin ON when CTRL1 = H V <sub>CC</sub> -0.5V/300mA	7 VCC VCC VCC VCC VCC VCC VCC VCC VCC VC
			9 GND
15	EXT	EXT output pin ON when CTRL1 = M2, H V <sub>CC</sub> -0.5V/350mA	7
			(15) WHE WHY
			9 GND

**CTRL Pin Output Truth Table** 

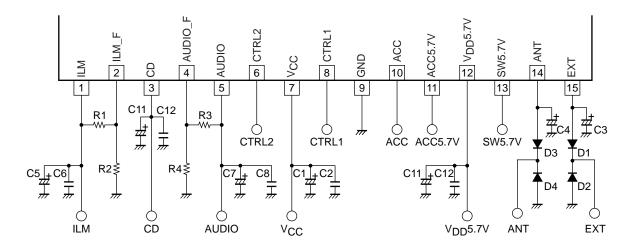
CTRL1	ANT	EXT	ILM
L	OFF	OFF	OFF
M1	OFF	OFF	ON
M2	OFF	ON	ON
Н	ON	ON	ON

CTRL2	CD	AUDIO	SW5
L	OFF	OFF	OFF
М	OFF	ON	ON
Н	ON	ON	ON

# **Timing Chart**



# **Recommended Operation Circuit**



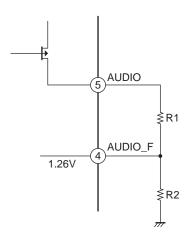
Peripheral parts list

Name of part	Description	Recommended value	Remarks
C1	Power supply bypass capacitor	100μF or more	These capacitors must be placed near
C2	Oscillation prevention capacitor	0.22μF or more	the V <sub>CC</sub> and GND pins.
C3	EXT output stabilization capacitor	2.2μF or more	
C4	ANT output stabilization capacitor	2.2μF or more	
C5, C57 C9, C11	Output stabilization capacitor	4.7μF or more	Electrolytic capacitor *
C6, C8, C10, C12	Output stabilization capacitor	0.22μF or more	Ceramic capacitor *
R1,R2	Resistor for ILM voltage adjustment	R1/R2 :30k $\Omega$ /5.6k $\Omega$ = 8.0V :27k $\Omega$ /3.9k $\Omega$ = 10.0V :33k $\Omega$ /3.9k $\Omega$ = 11.9V	A resistor with resistance accuracy as low as less than ±1% must be used.
R3, R4	Resistor for AUDIO voltage setting	R3/R4 :30kΩ/5.6kΩ = 8.0V :27kΩ/4.7kΩ = 8.5V :24kΩ/3.9kΩ = 9.0V	A resistor with resistance accuracy as low as less than ±1% must be used.
D1, D2, D3, D4	Diode for internal device breakdown protection		

<sup>\*:</sup> In order to stabilize the regulator outputs, it is recommended that the electrolytic capacitor and ceramic capacitor be connected in parallel.

Furthermore, the values listed above do not guarantee stabilization during the overcurrent protection operations of the regulator, so oscillation may occur during an overcurrent protection operation.

# • AUDIO/ILM output voltage setting method



The AUDIO\_F voltage is determined by the internal band gap voltage of the IC (typ = 1.26V).

Formula for AUDIO voltage calculation

$$AUDIO = \frac{1.26[V]}{R_2} \times R_1 + 1.26[V]$$

$$\frac{R_1}{R_2} = \frac{(AUDIO - 1.26)}{1.26}$$

The circuit must be designed in such a way that the R1:R2 ratio satisfies the formula given above for the AUDIO voltage that has been set.

Example: AUDIO = 8.5V setting method

$$\frac{R_1}{R_2} = \frac{\left(8.5 - 1.26\right)}{1.26} \cong 5.75$$

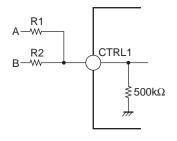
$$\frac{R_1}{R_2} = \frac{27k\Omega}{4.7k\Omega} \cong 5.74$$

$$AUDIO = 1.26V \times 5.74 + 1.26V \cong 8.49V$$

The ILM output voltage can be set by the above-mentioned method.

Note: In the above, the typical values are given in all instances for the values used and, as such, they will vary due to the effects of production-related variations of the IC and external resistors.

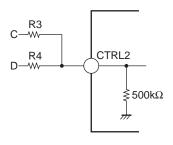
#### • CTRL1 Application Circuit Example



# (1) 3.3V input: $R1 = 4.7k\Omega$ , $R2 = 10k\Omega$

Α	В	CTRL1
0V	0V	0V
0V	3.3V	1.05V
3.3V	0V	2.23V
3.3V	3.3V	3.20V

# • CTRL2 Application Circuit Example



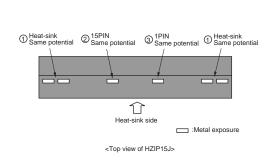
#### (1) 3.3V input: $R3 = R4 = 4.7k\Omega$

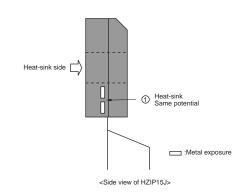
•	3.5 1 mput. 1t5 1t1 1.7 km					
	Α	В	CTRL2			
	0V	0V	0V			
	0V	3.3V	1.61V			
	3.3V	0V	1.61V			
	3.3V	3.3V	3.29V			

# Caution for implementing LV5681P to a system board

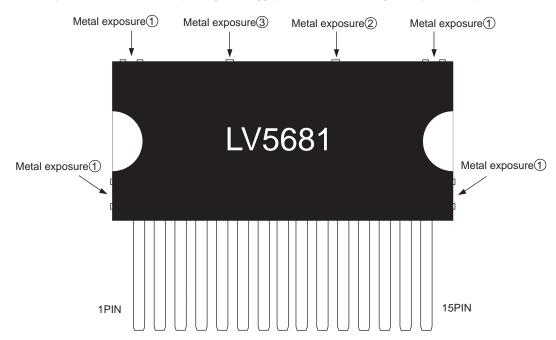
In HZIP15J, the package used in this IC, there are several metal exposure other than the connection pins and heat-sinks as shown in the following diagrams. In the diagrams, the electric potential of 2 and 3 are the same as Pin15 and Pin1, respectively. 2 (=Pin15) is EXT pin and 3 (=Pin1) is ILM output (regulator). When the IC is implemented to the system, make sure that no attachment clamp touches the exposed Pin1/Pin15. When the exposed Pin1/Pin15 touch the attachment clamp (same electrical potential as GND), ILM output or VCC enter the same state as time when GND was shorted. The electric potential of the exposed metal connected to heat-sinks 1 is the same as that of sub board of the IC (GND). Therefore, even if the exposed metal and GND of the system board are adjacent to each other, there should be no problem.

#### • HZIP15J external view





• Frame diagram (LV5681P) \*In the system power supply other than LV5681P, pin assignment may differ.

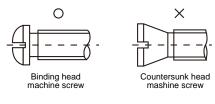


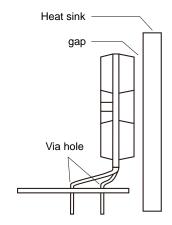
#### HZIP15J Heat sink attachment

Heat sinks are used to lower the semiconductor device junction temperature by leading the head generated by the device to the outer environment and dissipating that heat.

- a. Unless otherwise specified, for power ICs with tabs and power ICs with attached heat sinks, solder must not be applied to the heat sink or tabs.
- b. Heat sink attachment
  - · Use flat-head screws to attach heat sinks.
  - · Use also washer to protect the package.
  - · Use tightening torques in the ranges 39-59Ncm(4-6kgcm).
  - · If tapping screws are used, do not use screws with a diameter larger than the holes in the semiconductor device itself.
  - · Do not make gap, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
  - · Take care a position of via hole.
  - · Do not allow dirt, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
  - · Verify that there are no press burrs or screw-hole burrs on the heat sink.
  - · Warping in heat sinks and printed circuit boards must be no more than 0.05 mm between screw holes, for either concave or convex warping.
  - · Twisting must be limited to under 0.05 mm.
  - · Heat sink and semiconductor device are mounted in parallel.

    Take care of electric or compressed air drivers
  - The speed of these torque wrenches should never exceed 700 rpm, and should typically be about 400 rpm.





### c. Silicone grease

- · Spread the silicone grease evenly when mounting heat sinks.
- · Sanyo recommends YG-6260 (Momentive Performance Materials Japan LLC)

#### d. Mount

- · First mount the heat sink on the semiconductor device, and then mount that assembly on the printed circuit board.
- · When attaching a heat sink after mounting a semiconductor device into the printed circuit board, when tightening up a heat sink with the screw, the mechanical stress which is impossible to the semiconductor device and the pin doesn't hang.
- e. When mounting the semiconductor device to the heat sink using jigs, etc.,
  - · Take care not to allow the device to ride onto the jig or positioning dowel.
  - · Design the jig so that no unreasonable mechanical stress is not applied to the semiconductor device.

#### f. Heat sink screw holes

- · Be sure that chamfering and shear drop of heat sinks must not be larger than the diameter of screw head used.
- · When using nuts, do not make the heat sink hole diameters larger than the diameter of the head of the screws used. A hole diameter about 15% larger than the diameter of the screw is desirable.
- · When tap screws are used, be sure that the diameter of the holes in the heat sink are not too small. A diameter about 15% smaller than the diameter of the screw is desirable.
- g. There is a method to mount the semiconductor device to the heat sink by using a spring band. But this method is not recommended because of possible displacement due to fluctuation of the spring force with time or vibration.

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