



SANYO Semiconductors

# DATA SHEET

An ON Semiconductor Company

## LV5609LP — Bi-CMOS LSI For CCD Vertical Clock Driver

### Overview

The LV5609LP is vertical clock driver for CCD.

### Functions

- Ternary output ×2ch
- Binary output ×2ch
- SHT output ×1ch
- Output ON resistance : 30Ω typ

### Specifications

**Absolute Maximum Ratings** at  $T_a = 25^\circ\text{C}$ ,  $V_{SS} = V_M = 0\text{V}$

| Parameter                   | Symbol       | Conditions                 | Ratings     | Unit             |
|-----------------------------|--------------|----------------------------|-------------|------------------|
| Maximum supply voltage      | $V_{DD}$ max |                            | 6           | V                |
|                             | VH max       |                            | 20          | V                |
|                             | VL max       |                            | -10         | V                |
|                             | VH-VL max    |                            | 24          | V                |
| Allowable power dissipation | $P_d$ max    | with specified substrate * | 0.8         | W                |
| Operating temperature       | $T_{opr}$    |                            | -20 to +80  | $^\circ\text{C}$ |
| Storage temperature         | $T_{stg}$    |                            | -40 to +125 | $^\circ\text{C}$ |

\* : Specified substrate : 40×50×0.8mm<sup>3</sup>, glass epoxy four-layer (2S2P) board

**Allowable Operating Ratings** at  $T_a = 25^\circ\text{C}$ ,  $V_{SS} = V_M = 0\text{V}$

| Parameter               | Symbol    | Conditions | Ratings     |      |          | Unit |
|-------------------------|-----------|------------|-------------|------|----------|------|
|                         |           |            | min         | typ  | max      |      |
| Supply voltage          | $V_{DD}$  |            | 2.0         | 3.3  | 5.5      | V    |
|                         | VH        |            |             | 15   | 17       | V    |
|                         | VL        |            | -8.5        | -7.5 | -4       | V    |
|                         | VH-VL     |            |             |      | 23.5     | V    |
| CMOS input High voltage | $V_{INH}$ |            | $0.8V_{DD}$ |      | $V_{DD}$ | V    |
| CMOS input Low voltage  | $V_{INL}$ |            | -0.1        |      | 0.4      | V    |

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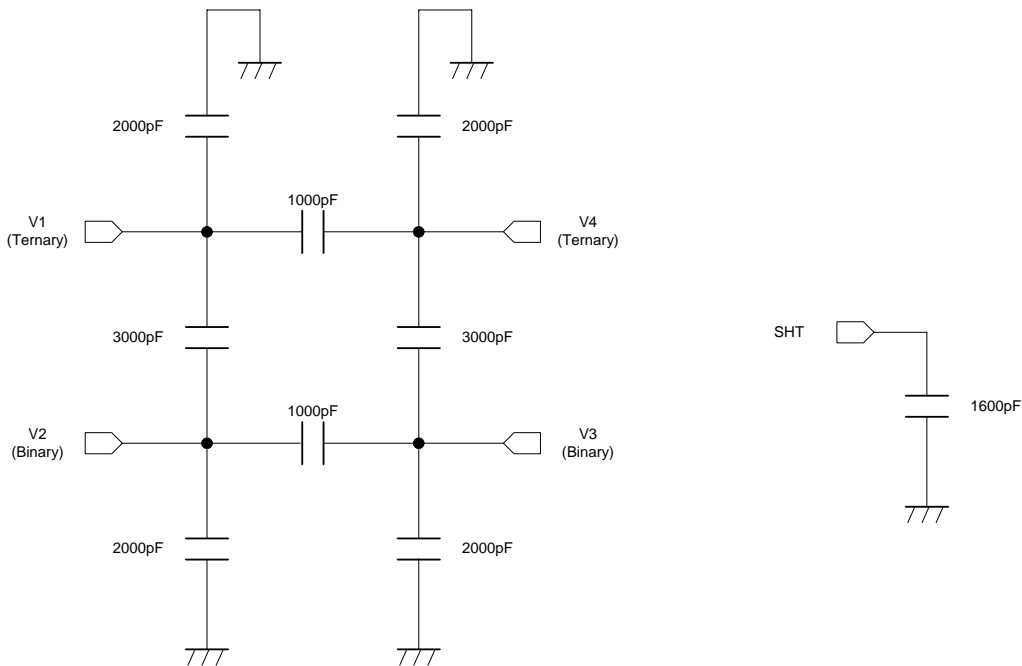
# LV5609LP

**Electrical Characteristics** at  $T_a = 25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V}$ ,  $V_{SS} = 0\text{V}$ ,  $V_H = 15\text{V}$ ,  $V_L = -7.5\text{V}$ ,  $V_M = 0\text{V}$ ,  
Unless otherwise specified

| Parameter              | Symbol    | Conditions                           | Ratings |     |     | Unit          |
|------------------------|-----------|--------------------------------------|---------|-----|-----|---------------|
|                        |           |                                      | min     | typ | max |               |
| Static current drain   | $I_{DD}$  | $V_{DD}$ pin                         |         |     | 1   | $\mu\text{A}$ |
|                        | $I_H$     | $V_H$ pin                            |         |     | 10  | $\mu\text{A}$ |
|                        | $I_L$     | $V_L$ pin                            |         |     | 1   | $\mu\text{A}$ |
| Dynamic current drain  | $I_{DD}$  | $V_{DD}$ pin See *1 and *2.          |         |     | 1   | $\text{mA}$   |
|                        | $I_H$     | $V_H$ pin See *1 and *2.             |         | 2.4 | 4.5 | $\text{mA}$   |
|                        | $I_L$     | $V_L$ pin See *1 and *2.             |         | 3   | 5   | $\text{mA}$   |
| Output ON resistance   | $R_L$     | $I_O = +10\text{mA}$                 |         | 20  | 30  | $\Omega$      |
|                        | $R_M$     | $I_O = \pm 10\text{mA}$              |         | 30  | 45  | $\Omega$      |
|                        | $R_H$     | $I_O = -10\text{mA}$                 |         | 30  | 40  | $\Omega$      |
|                        | $R_{SHT}$ | $I_O = -10\text{mA}$                 |         | 30  | 40  | $\Omega$      |
| Propagation delay time | TPLM      | No load                              |         |     | 200 | ns            |
|                        | TPMH      | No load                              |         |     | 200 | ns            |
|                        | TPLH      | No load                              |         |     | 200 | ns            |
|                        | TPML      | No load                              |         |     | 200 | ns            |
|                        | TPHM      | No load                              |         |     | 200 | ns            |
|                        | TPHL      | No load                              |         |     | 200 | ns            |
| Rise time              | TTLM      | $V_L \rightarrow V_M$ V1, V3 See *1. |         |     | 800 | ns            |
|                        |           | $V_L \rightarrow V_M$ V2, V4 See *1. |         |     | 800 | ns            |
|                        | TTMH      | $V_M \rightarrow V_L$ V1, V3 See *1. |         |     | 800 | ns            |
|                        | TTLH      | $V_L \rightarrow V_H$ SHT See *1.    |         |     | 200 | ns            |
| Fall time              | TTML      | $V_M \rightarrow V_L$ V1, V3 See *1. |         |     | 800 | ns            |
|                        |           | $V_M \rightarrow V_L$ V2, V4 See *1. |         |     | 800 | ns            |
|                        | TTHM      | $V_H \rightarrow V_M$ V1, V3 See *1. |         |     | 800 | ns            |
|                        | TTHL      | $V_H \rightarrow V_L$ SHT See *1.    |         |     | 200 | ns            |

\*1 : Refer to the CCD equivalent load shown below.

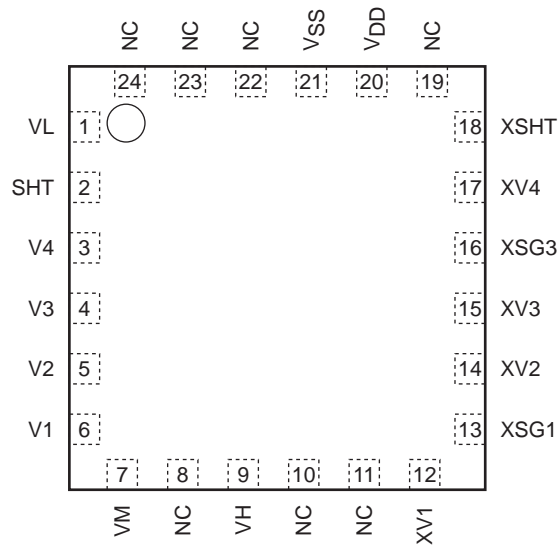
\*2 : Refer to the timing waveform on Page 7.





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## Pin Assignment

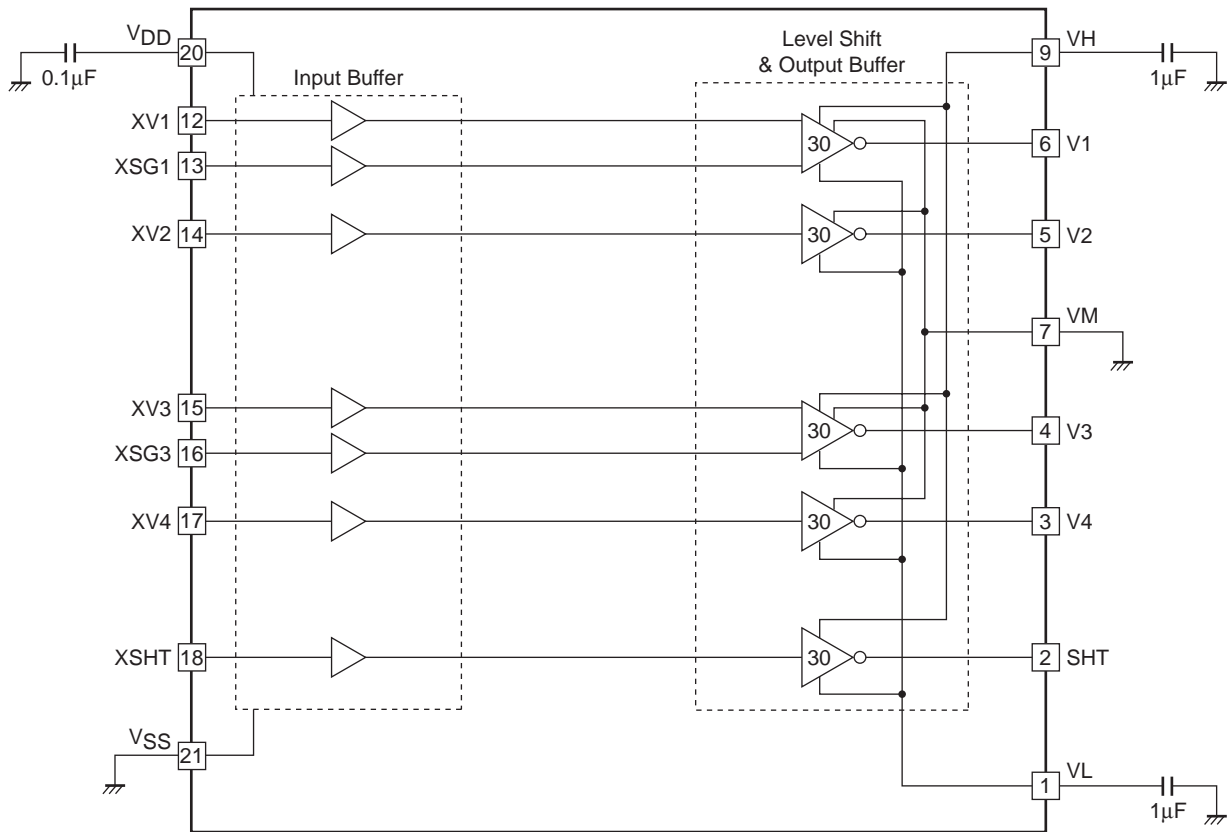


## Pin Function

| Pin No. | Name            | Mode  |
|---------|-----------------|---|
| 1       | VL              | Lo power for output (-7.5V system)          |
| 2       | SHT             | Level shift output (binary VH, VL)          |
| 3       | V4              | Level shift output (binary VM, VL)          |
| 4       | V3              | Level shift output (ternary VH, VM, VL)     |
| 5       | V2              | Level shift output (binary VM, VL)          |
| 6       | V1              | Level shift output (ternary VH, VM, VL)     |
| 7       | VM              | GND for output                              |
| 8       | NC              |   |
| 9       | VH              | Hi power supply for output (15V system)     |
| 10      | NC              |   |
| 11      | NC              |   |
| 12      | XV1             | V1 transfer pulse input                     |
| 13      | XSG1            | V1 read pulse input                         |
| 14      | XV2             | V2 transfer pulse input                     |
| 15      | XV3             | V3 transfer pulse input                     |
| 16      | XSG3            | V3 read pulse input                         |
| 17      | XV4             | V4 transfer pulse input                     |
| 18      | XSHT            | SHT pulse input                             |
| 19      | NC              |   |
| 20      | V <sub>DD</sub> | Power supply for input buffer (3.3V system) |
| 21      | V <sub>SS</sub> | GND for input buffer                        |
| 22      | NC              |   |
| 23      | NC              |   |
| 24      | NC              |   |

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## Block Diagram

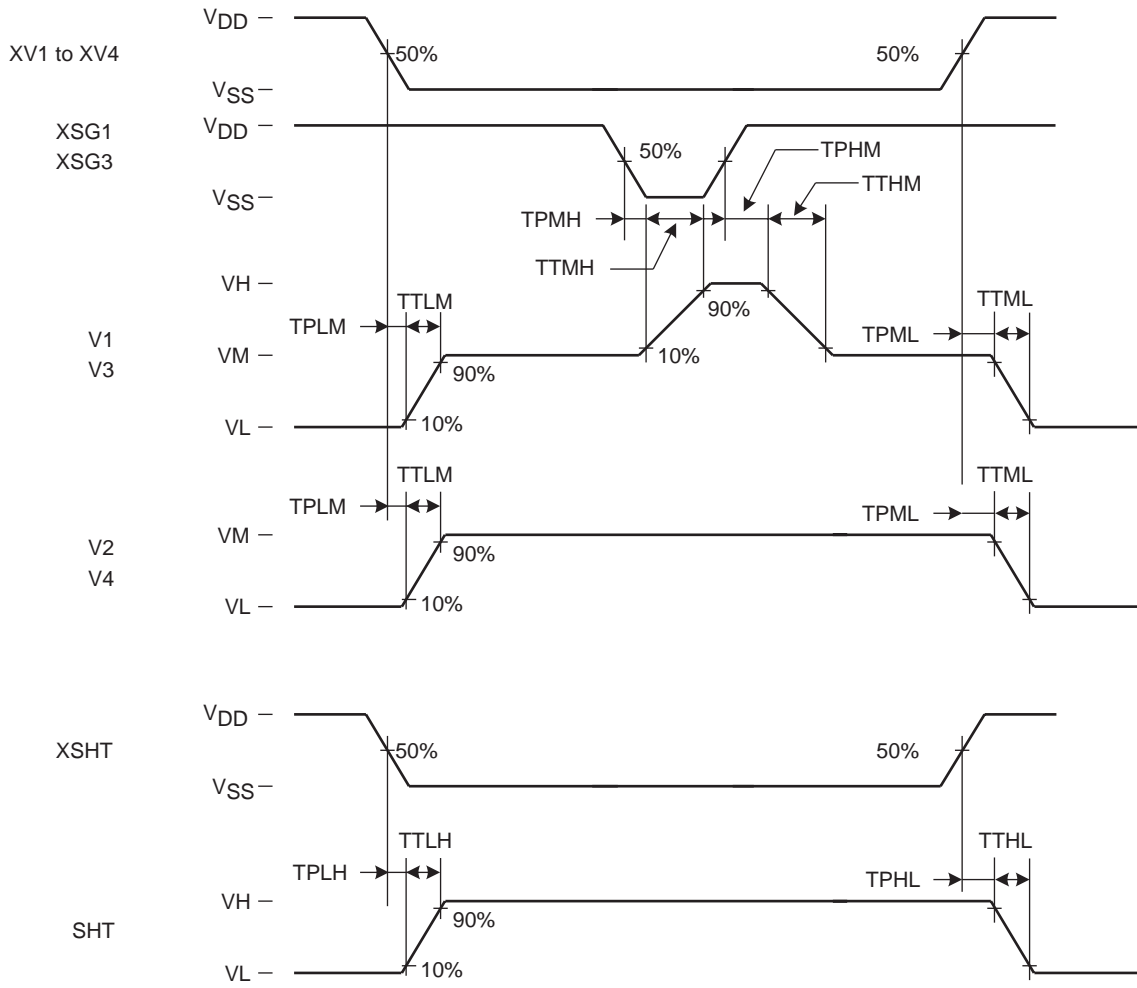


## Logical Function Table

| Input      |              |            |      | Output   |          |     |
|------------|--------------|------------|------|----------|----------|-----|
| XV1<br>XV3 | XSG1<br>XSG3 | XV2<br>XV4 | XSHT | V1<br>V3 | V2<br>V4 | SHT |
| L          | L            | X          | X    | VH       | X        | X   |
| L          | H            | X          | X    | VM       | X        | X   |
| H          | L            | X          | X    | VL       | X        | X   |
| H          | H            | X          | X    | VL       | X        | X   |
| X          | X            | L          | X    | X        | VM       | X   |
| X          | X            | H          | X    | X        | VL       | X   |
| X          | X            | X          | L    | X        | X        | VH  |
| X          | X            | X          | H    | X        | X        | VL  |

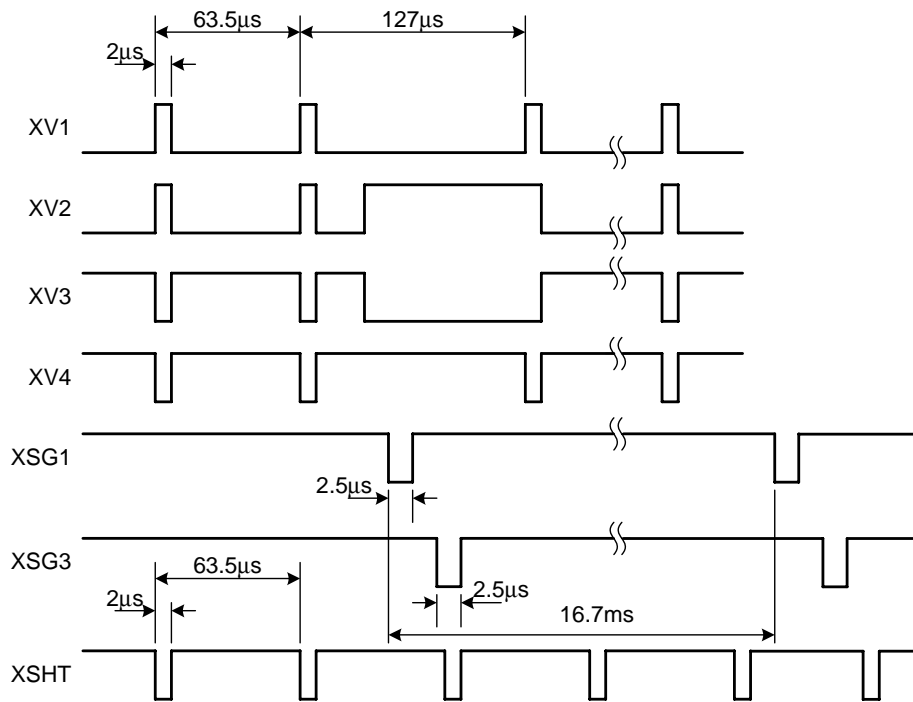
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## Timing Chart

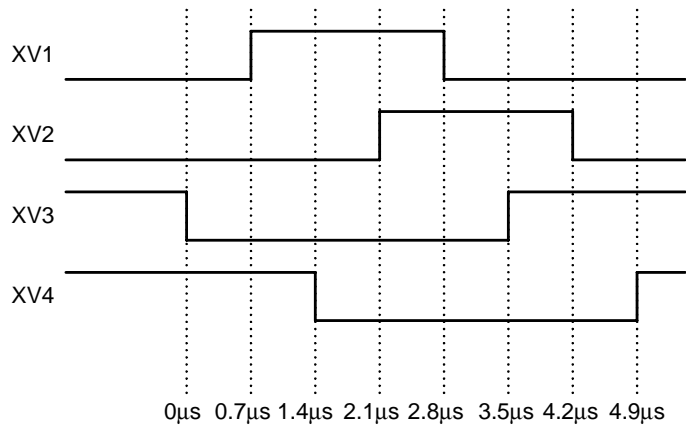


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## CCD Equivalent Load Measurement Timing Waveform



## Enlarged View of overlapped portion



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