Ordering number : EN*A1811A

Preliminary

SANYO Semiconductors
DATA SHEET

CMOS IC

LE24CBK222 — Triple port EEPROM Two Wire Serial Interface (2K+2K EEPROM)

Overview

The triple port EEPROM series consists of two independent banks, and each bank can be controlled separately using dedicated control pins. The EEPROM also features a control port, which is a third pin separate from the pins used for the banks, and by accessing the memory areas from this control port, the two-bank configuration (2K bits + 2K bits) can be used as a pseudo-one-bank configuration (4K bits). Together with the 16-byte page write function, this enables a reduction in the number of factory write processes.

Furthermore, the EEPROM has a configuration area which is separate from the 2K-bit + 2K-bit area, and by using the settings stored in this configuration area, it is possible to change the slave address for each port and to set read/write protection for each port.

This product incorporates SANYO's high performance CMOS EEPROM technology and realizes high-speed operation and high-level reliability. The interface of this product is compatible with the I^2C bus protocol, making it ideal as a nonvolatile memory for small-scale parameter storage.

In addition, this product also supports DDC2™, so it can also be used as an EDID data storage memory for display equipment.

Functions

- Capacity : Bank1:2K bits (256 × 8 bits) + Bank2:2K bits (256 × 8 bits)
  + configuration area: 128 bits (16 × 8 bits), 4224 bits in total
- Single supply voltage : 2.5V to 5.5V
- Interface : Two wire serial interface (I^2C Bus*), VESA DDC2™ compliant** 3-port access
- Operating clock frequency : 400kHz (max)
- Low power consumption : Standby: 5μA (max)
  : One-bank read: 0.5 mA (max.), Two-bank simultaneous read: 1.0 mA (max.)

Continued on next page.

* : I^2C Bus is a trademark of Philips Corporation.
** : DDC and EDID are trademarks of Video Electronics Standard Association (VESA).

* This product is licensed from Silicon Storage Technology, Inc. (USA), and manufactured and sold by SANYO Semiconductor Co., Ltd.

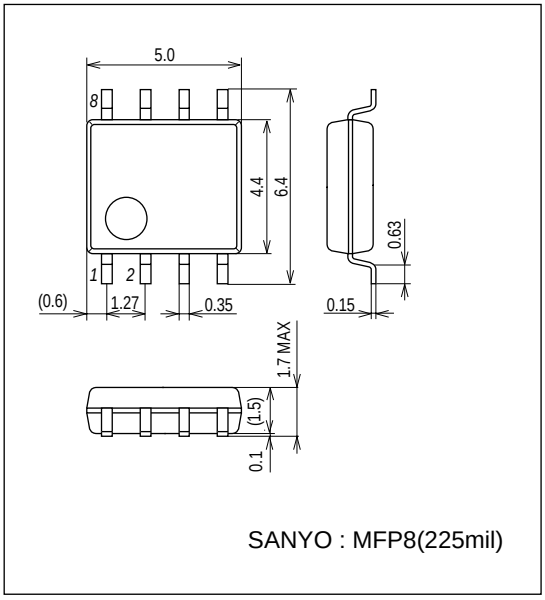
Continued from preceding page.

- Automatic page write mode: 16 bytes
- Slave address setting : Slave address can be set for each port.
- Protect function : Read/write protection can be set for each port.
- Read mode : Sequential read and random read
- Erase/Write cycles : 10^6 cycles
- Data Retention : 20 years
- High reliability : Adopts SANYO's proprietary symmetric memory array configuration (USP6947325)
  Noise filters connected to SCL1, SDA1, SCL2, SDA2, SCLC and SDAC pins
  Incorporates a feature to prohibit write operations under low voltage conditions.
- Package : LE24CBK222M MFP8 (225mil)
  : LE24CBK222TT MSOP8 (150mil)

Package Dimensions

unit:mm (typ)

3032E [LE24CBK222M]

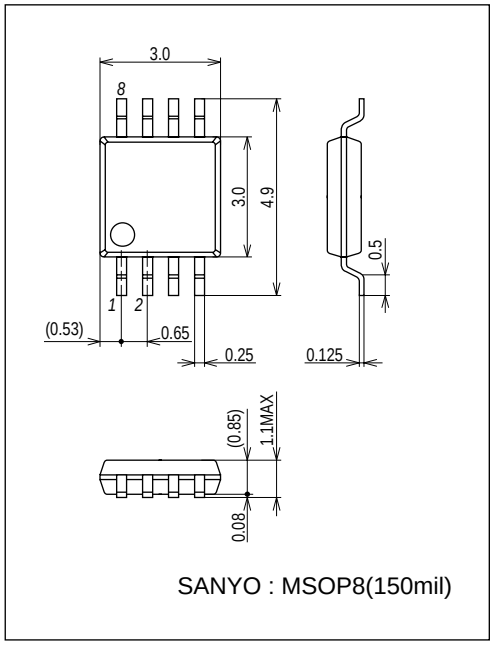


SANYO : MFP8(225mil)

Package Dimensions

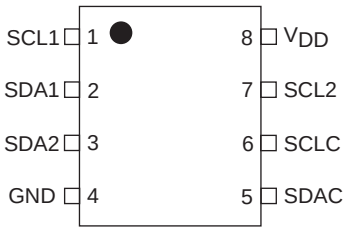
unit:mm (typ)

3245B [LE24CBK222TT]



SANYO : MSOP8(150mil)

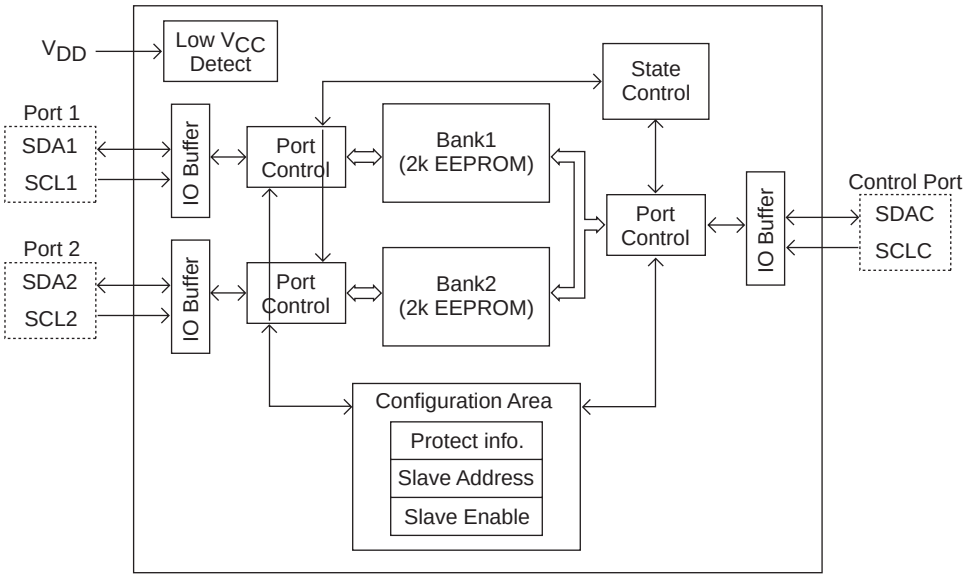
Pin Assignment



Pin Descriptions

PIN.1	SCL1	Clock input	Port 1
PIN.2	SDA1	Data input/output	
PIN.3	SDA2	Data input/output	Port 2
PIN.4	GND	Ground	
PIN.5	SDAC	Data input/output	Control port
PIN.6	SCLC	Clock input	
PIN.7	SCL2	Clock input	Port 2
PIN.8	V_{DD}	Power supply	

Block Diagram



Description of Operation

Access to Bank1 is performed through port 1 (SCL1 / SDA1), and access to Bank2 through port 2 (SCL2 / SDA2). When read operations are performed, Bank1 and Bank2 can be controlled independently of each other and both banks can be accessed at the same time. When write operations are performed, it is not possible to access both banks while a write operation is in progress in one of the banks (including the write wait time).

Both Bank1 and Bank2 can be accessed from the control port (SCLC, SDAC). The two-bank configuration (2K bits + 2K bits) can be used as a pseudo-one-bank configuration (4K bits). Data correlation is guaranteed between the mode in which accesses are made from port1 or port 2 and the mode in which accesses are made from the control port, enabling operations such as writing data from control port in a lump and reading data from port 1 or port 2.

Access to the configuration area where the slave addresses of the ports and protect information is stored is made from the control port.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage			-0.5 to +6.5	V
DC input voltage			-0.5 to +5.5	V
Over-shoot voltage		Below 20ns	-1.0 to +6.5	V
Storage temperature	Tstg		-65 to +150	°C

Note: If an electrical stress exceeding the maximum rating is applied, the device may be damaged.

Operating Conditions

Parameter	Symbol	Conditions	Ratings	Unit
Operating supply voltage			2.5 to 5.5	V
Operating temperature			-40 to +85	°C

DC Electrical Characteristics

Parameter	Symbol	Conditions	V_{DD}=2.5V to 5.5V			Unit
			min	typ	max	
Supply current at reading (when either Bank1 or Bank2 is read)	$I_{CC}11$	f=400kHz			0.5	mA
Supply current at reading (when both Bank1 and Bank2 are read simultaneously)	$I_{CC}12$	f=400kHz			1.0	mA
Supply current at writing	$I_{CC}2$	f=400kHz, t_{WC}=5ms			5	mA
Standby current	I_{SB}	V_{IN}=V_{DD} or GND		0.7	5	μA
Input leakage current	I_{LI}	V_{IN}=GND to V_{DD}	-2.0		+2.0	μA
Output leakage current (SDA)	I_{LO}	V_{OUT}=GND to V_{DD}	-2.0		+2.0	μA
Input low voltage	V_{IL}				V_{DD}*0.3	V
Input high voltage	V_{IH}		V_{DD}*0.7			V
Output low level voltage	V_{OL}	I_{OL}=0.7mA, V_{DD}=2.5V			0.2	V
		I_{OL}=3.0mA, V_{DD}=2.5V			0.4	V
		I_{OL}=3.0mA, V_{DD}=5.5V			0.4	V
		I_{OL}=6.0mA, V_{DD}=4.5V			0.6	V

Capacitance/Ta=25°C, f=100kHz

Parameter	Symbol	Conditions	min	typ	max	Unit
In/Output capacitance	$C_{I/O}$	$V_{I/O}$=0V (SDA1, SDA2, SDAC)		2	5	pF
Input capacitance	C_I	V_{IN}=0V (SCL1, SCL2, SCLC)		2	5	pF

Note: This parameter is sampled and not 100% tested.

AC Electric Characteristics

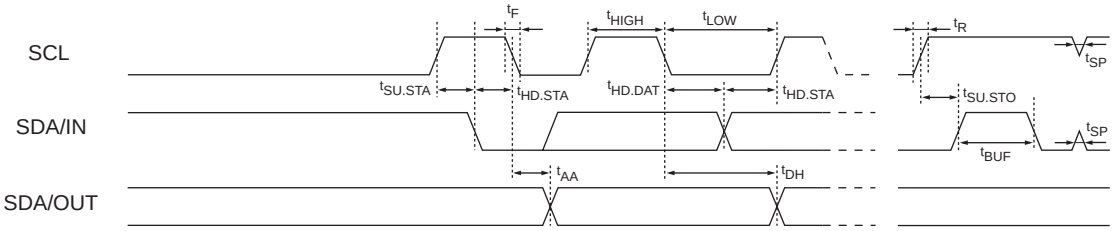
Fast Mode

Parameter	Symbol	V_{DD}=2.5V to 5.5V			unit
		min	typ	max	
Slave mode SCL clock frequency	f_{SCLS}			400	kHz
SCL clock low time	t_{LOW}	1200			ns
SCL clock high time	t_{HIGH}	600			ns
SDA output delay time	t_{AA}	100		900	ns
SDA data output hold time	t_{DH}	100			ns
Start condition setup time	$t_{SU.STA}$	600			ns
Start condition hold time	$t_{HD.STA}$	600			ns
Data in setup time	$t_{SU.DAT}$	100			ns
Data in hold time	$t_{HD.DAT}$	0			ns
Stop condition setup time	$t_{SU.STO}$	600			ns
SCL, SDA rise time	t_R			300	ns
SCL, SDA fall time	t_F			300	ns
Bus release time	t_{BUF}	1200			ns
Noise suppression time	t_{SP}			100	ns
Write cycle time	t_{WC}			5	ms

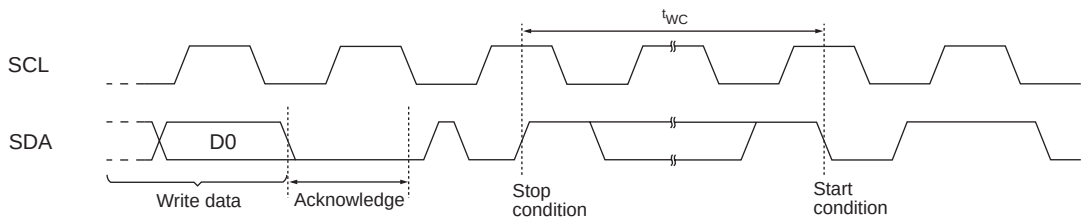
Standard Mode

Parameter	Symbol	V_{DD}=2.5V to 5.5V			unit
		min	typ	max	
Slave mode SCL clock frequency	f_{SCLS}			100	kHz
SCL clock low time	t_{LOW}	4700			ns
SCL clock high time	t_{HIGH}	4000			ns
SDA output delay time	t_{AA}	100		3500	ns
SDA data output hold time	t_{DH}	100			ns
Start condition setup time	$t_{SU.STA}$	4700			ns
Start condition hold time	$t_{HD.STA}$	4000			ns
Data in setup time	$t_{SU.DAT}$	250			ns
Data in hold time	$t_{HD.DAT}$	0			ns
Stop condition setup time	$t_{SU.STO}$	4000			ns
SCL, SDA rise time	t_R			1000	ns
SCL, SDA fall time	t_F			300	ns
Bus release time	t_{BUF}	4700			ns
Noise suppression time	t_{SP}			100	ns
Write cycle time	t_{WC}			5	ms

Bus Timing



Write Timing



Pin Functions

(Port1: For Bank1)

SCL1 (serial clock input) pin

The SCL1 pin is the serial clock input pin used to access the Bank1 area, and processes signals at the rising and falling edges of the SCL1 clock signal.

This pin must be pulled up by a resistor to the V_{DD} level, and wired-ORed with another open drain (or open collector) output device for use.

While this product is being accessed from the control port, it cannot be accessed from port 1.

SDA1 (serial data input/output) pin

The SDA1 pin is used to transfer serial data to the input/output of the Bank1 side area and it consists of a signal input pin and n-channel transistor open drain output pin.

Like the SCL1 line, the SDA1 line must be pulled up by a resistor to the V_{DD} level and wired-ORed with another open drain (or open collector) output device for use.

While this product is being accessed from the control port, it cannot be accessed from port 1.

(Port2: For Bank2)

SCL2 (serial clock input) pin

The SCL2 pin is the serial clock input pin used to access the Bank2 area, and processes signals at the rising and falling edges of the SCL2 clock signal.

This pin must be pulled up by a resistor to the V_{DD} level, and wired-ORed with another open drain (or open collector) output device for use.

While this product is being accessed from the control port, it cannot be accessed from port 2.

SDA2 (serial data input/output) pin

The SDA2 pin is used to transfer serial data to the input/output of the Bank2 side area and it consists of a signal input pin and n-channel transistor open drain output pin.

Like the SCL2 line, the SDA2 line must be pulled up by a resistor to the V_{DD} level and wired-ORed with another open drain (or open collector) output device for use.

While this product is being accessed from the control port, it cannot be accessed from port 2.

(Control port: For accessing both banks and for accessing the configuration area)

SCLC (serial clock input) pin

The SCLC pin is the serial clock input pin used for accessing both the Bank1 and Bank2 areas and the configuration area. The signals are processed at the rising and falling edges of the SCLC clock signal.

The pin must be pulled up by a resistor to the V_{DD} level, and it is wired-ORed with another open drain (or open collector) output device for use.

SDAC (serial data input/output) pin

The SDAC pin is used to transfer serial data to the input/output of both Bank1 and Bank2 areas and the configuration area, and it consists of a signal input pin and n-channel transistor open drain output pin.

Like the SCLC line, the SDAC line must be pulled up by a resistor to the V_{DD} level, and it is wired-ORed with another open drain (or open collector) output device for use.

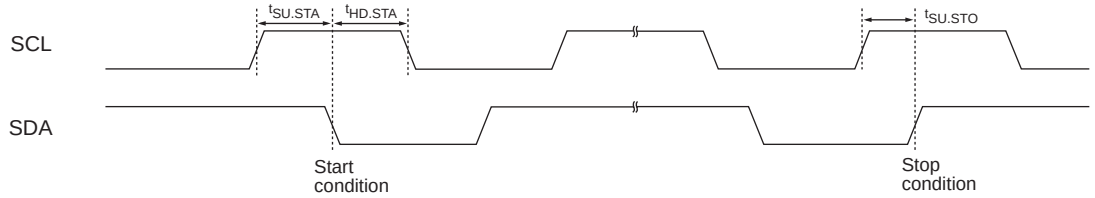
Functional Description

1. Start condition

When the SCL line is at the high level, the start condition is established by changing the SDA line from high to low. The operation of the EEPROM as a slave starts in the start condition.

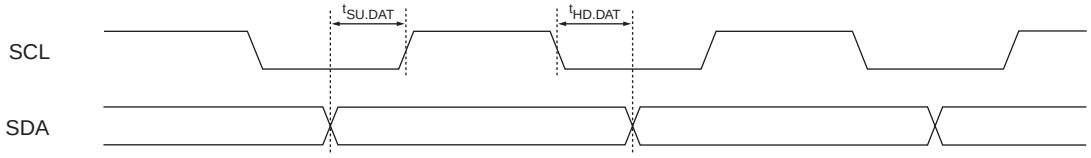
2. Stop condition

When the SCL line is at the high level, the stop condition is established by changing the SDA line from low to high. When the device is set up for the read sequence, the read operation is suspended when the stop condition is received, and the device is set to standby mode. When it is set up for the write sequence, the capture of the write data is ended when the stop condition is received, and the EEPROM internal write operation is started.



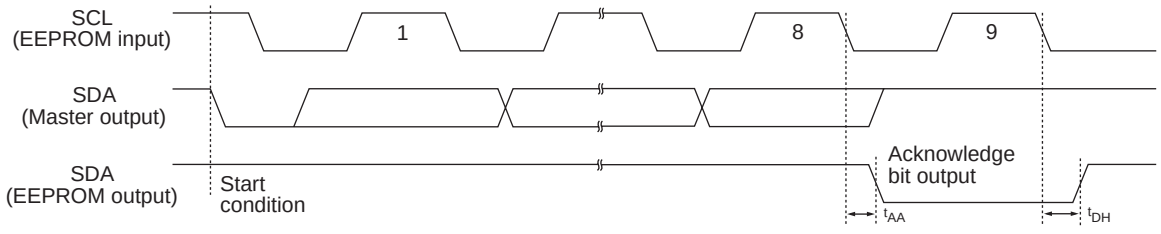
3. Data transfer

Data is transferred by changing the SDA line while the SCL line is low. When the SDA line is changed while the SCL line is high, the resulting condition will be recognized as the start or stop condition.



4. Acknowledge

During data transfer, 8 bits are transferred in succession, and then in the ninth clock cycle period the device on the system bus receiving the data sets the SDA line to low, and sends the acknowledge signal indicating that the data has been received. The acknowledge signal is not sent during an EEPROM internal write operation.

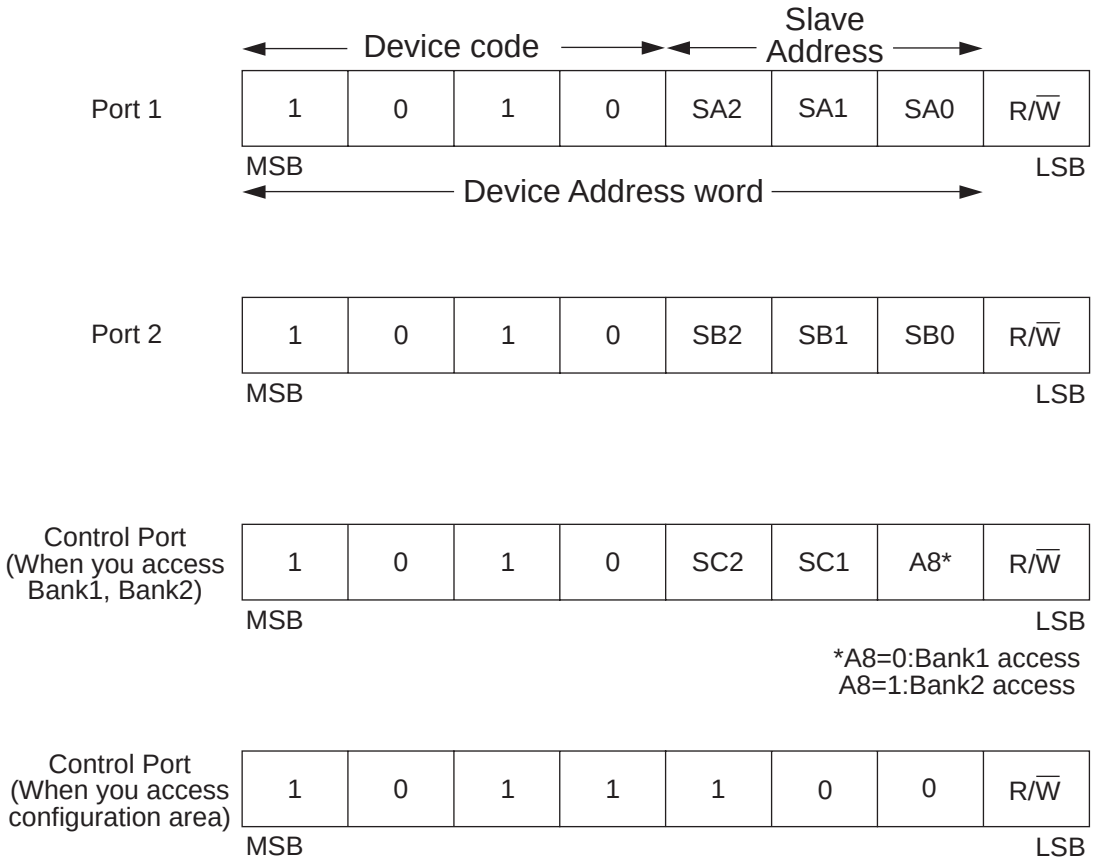


5. Device addressing

For the purposes of communication, the master device in the system generates the start condition for the slave device. Communication with a particular slave device is enabled by sending along the SDA bus the device address, which is 7 bits long, and the read/write command code, which is 1 bit long, immediately following the start condition.

The upper four bits of the device address are called the device code which, for this product, are fixed at “1010b.” The 3-bit slave address (SA2, SA1, and SA0 for access from port 1; SB2, SB1, and SB0 for access from port 2; SC2 and SC1for access from the control port) following the device code are stored in the configuration area, and any values can be set for these addresses. However, the device address to be used to access the configuration area is fixed at “1011_100b” and cannot be changed.

When the device code input from SDA and the slave addresses are compared with the product’s device code and configuration area that were set at the mounting stage and found to match, the product sends the acknowledge signal during the ninth clock cycle period, and initiates the read or write operation in accordance with the read or write command code. If they do not match, the EEPROM returns to standby mode. When a read operation is performed immediately after the slave device has been switched, the random read command must be used.



The slave addresses are set as follows when this product is shipped.
(SA2, SA1, SA0) = (0, 0, 0)
(SB2, SB1, SB0) = (0, 0, 0)
(SC2, SC1) = (0, 0)

6 Internal mode

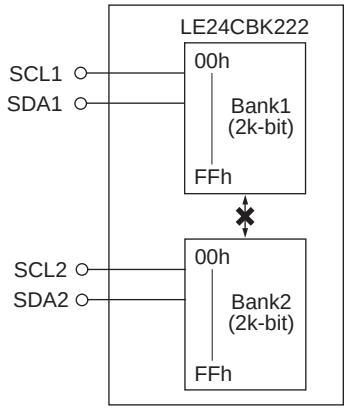
This product functions in bank mode when it is accessed from port 1 or port 2 and in combined mode when it is accessed from the control port.

6-1. Bank mode

The EEPOM functions in the bank mode when it is accessed from port 1 or port 2. In the bank mode, Bank1 is controlled from the port 1 pins (SCL1, SDA1), and Bank2 is controlled from the port 2 pins (SCL2, SDA2).

When read operations are performed, the two banks can be controlled independently of each other, and access to different addresses can be made at the same time. This enables the EEPROM to be handled as two independent EEPROM devices incorporated in a single package. In turn, this makes it possible for the Bank1 and Bank2 sides to be connected to the MCU of separate systems.

When write operations are performed, it is not possible to write data in two banks at the same time. After the write data has been input into one of the banks and the internal rewriting operation has started, access to the two banks is not possible during the write time tWC period.



6-2. Combine mode

The EEPROM functions in the combined mode when it is accessed from the control port. In the combined mode, Bank1 and Bank2 are controlled from the control port pins (SCLC, SDAC). The combined mode uses the two-bank configuration (2K bits + 2K bits) as a pseudo-one-bank configuration (4K bits). Since the memory area is processed as a single 4K-bit bank in this mode, the MSB address changes from A7 to A8. Input A8=0 to control the Bank1 area, and input A8=1 to control the Bank2 area.

When, in the combined mode, the last address (0FFh) of Bank1 has been reached in a sequential read operation, the address (100h) in the Bank2 side is sequentially read. Similarly, when the last address (1FFh) of Bank2 has been reached, it is rolled over to the Bank1 address (000h) and continues to be read into this address.

Data correlation is guaranteed between the bank mode and combined mode, enabling operations while switching the mode such as performing write in the combined mode and read in the bank mode.

While the EEPROM is functioning in the combined mode, access from port 1 and port 2 is disabled. In the bank mode, the read operation stops while data is being read from the ports. And, in the bank mode, while the data of one of the banks is being written, access from the control port is disabled until the internal write operation is completed.

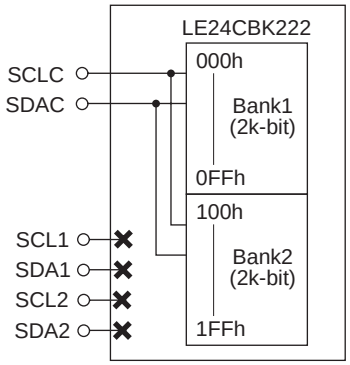


Fig.: configuration area memory map

address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0h	×	×	×	Slv_ENBC	×	SC2	SC1	×
1h	×	×	×	Slv_ENB1	×	SA2	SA1	SA0
2h	×	×	×	Slv_ENB2	×	SB2	SB1	SB0
3h	Reserved R/W							
4h	Reserved R/W							
5h	Reserved R/W							
6h	Reserved R/W							
7h	Reserved R/W							
8h	×	×	×	×	×	×	PB1C	PB0C
9h	×	×	×	×	×	×	PB1A	PB0A
Ah	×	×	×	×	×	×	PB1B	PB0B
Bh	Reserved R/W							
Ch	Reserved R/W							
Dh	Reserved R/W							
Eh	Reserved R/W							
Fh	Device Revision (Reserved R only)							

7. Configuration area

This product has a configuration area equivalent to 16 addresses that is separate from Bank1 and Bank2. Refer to the above table for the memory map of the configuration area. Access to the configuration area is performed by inputting device address “1011_100b” from the control port.

7-1. Slave address bits (SA2, SA1, SA0, SB2, SB1, SB0, SC2, SC1)

The slave address bits are used to set the slave address in the device address. This product does not have slave address pins, but has slave address bits inside instead. By changing the values of these bits, it is possible to change the slave addresses at any time. Each port contains a slave address bit, and a different slave address can be assigned to the ports.

Port	Slave address bit
Port 1	SA2, SA1, SA0
Port 2	SB2, SB1, SB0
Control Port	SC2, SC1

7-2. Slave address enable bits (Slv_ENB1, Slv_ENB2, Slv_ENBC)

The slave address enable bits (Slv_ENB) are used to enable or disable the slave addresses of the ports, which have been set in the configuration area. When Slv_ENB=”0,” the slave address bits of the ports which have been set in the configuration area are disabled, and the slave address value input in the device address is don’t care. When another slave device exists on the same bus as the EEPROM, Slv_ENB=”1” must be set without fail.

Port	Slave address enable bit
Port 1	Slv_ENB1
Port 2	Slv_ENB2
Control Port	Slv_ENBC

7-3. Protect bits (PB1A, PB0A, PB1B, PB0B, PB1C, PB0C)

The protect bits are used to set the access level. The value of the protect bits determine whether the product is to be protected against read and write operations. The protect bits can be set for each port.

PB1n	PB0n	access level
0	0	access inhibit
0	1	Read write prohibition. Only the acknowledge response.
1	0	Write prohibition. Only the read.
1	1	Read write possible.

7-4. Reserved R/W

The bits in addresses 3h to 7h and Bh to Eh in the configuration area are reserved bits, and have no significance. Read and write are possible in the areas with these addresses, but it is recommended that the areas not be used.

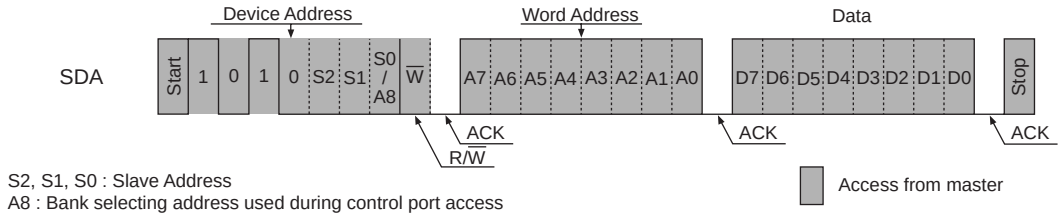
7-5. Device revision

The revision code of this product is stored in the Fh address of the configuration area. It is read-only and cannot be rewritten with a write operation.

8 EEPROM write operation

8-1. Byte writing

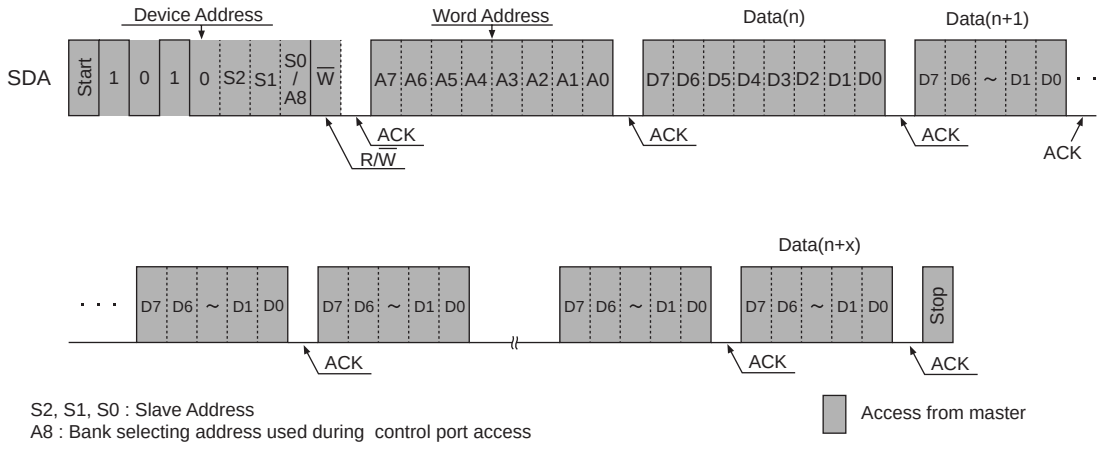
When the EEPROM receives the 7-bit device address and write command code “0” after the start condition, it generates an acknowledge signal. After this, if it receives the 8-bit word address, generates an acknowledge signal, receives the 8-bit write data, generates an acknowledge signal and then receives the stop condition, the internal write operation of the EEPROM in the designated memory address will start. Rewriting is completed in the t_{WC} period after the stop condition. During an EEPROM internal write operation, no input is accepted and no acknowledge signals are generated.



8-2. Page writing

This product enables pages with up to 16 bytes to be written. The basic data transfer procedure is the same as for byte writing: Following the start condition, the 7-bit device address and write command code “0,” word address (n), and data (n) are input in this order while confirming acknowledge “0” every 9 bits. The page write mode is established if, after data (n) is input, the write data (n+1) is input without inputting the stop condition. After this, the write data equivalent to the largest page size can be received by a continuous process of repeating the receiving of the 8-bit write data and generating the acknowledge signals.

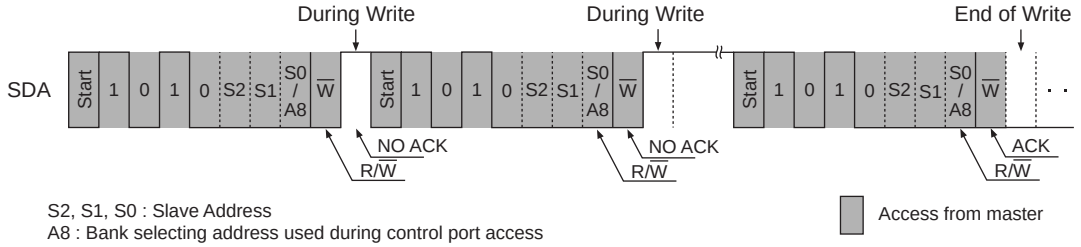
At the point when the write data (n+1) has been input, the lower 4 bits (A0-A3) of the word addresses are automatically incremented to form the (n+1) address. In this way, the write data can be successively input, and the word address on the page is incremented each time the write data is input. If the write data exceeds 16 bytes or the last address of the page is exceeded, the word address on the page is rolled over. Write data will be input into the same address two or more times, but in such cases the write data that was input last will take effect. Finally, the EEPROM internal write operation corresponding to the page size for which the write data is received starts from the designated memory address when the stop condition is received.



8-3. Acknowledge polling

Acknowledge polling is used to find out when the EEPROM internal write operation is completed. When the stop condition is received and the EEPROM starts rewriting, all operations are prohibited, and no response can be given to the signals sent by the master device. Therefore, in order to find out when the EEPROM internal write operation is completed, the start condition, device address and write command code are sent from the master device to the EEPROM (slave device), and the response of the slave device is detected.

In other words, if the slave device does not send the acknowledge signal, it means that the internal write operation is in progress; conversely, if it does send the acknowledge signal, it means that the internal write operation has been completed.



9 EEPROM read operations

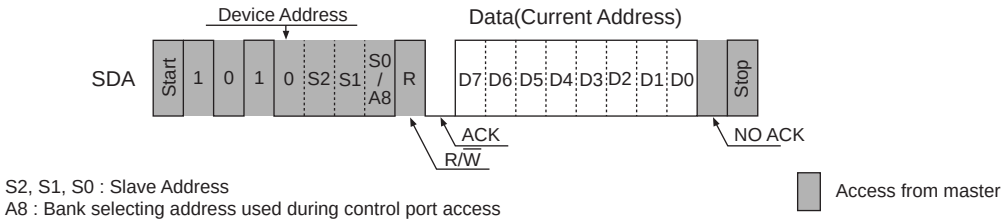
9-1. Current address reading

The address equivalent to the memory address accessed last +1 is held as the internal address of the EEPROM for both write* and read operations. Therefore, provided that the master device has recognized the position of the EEPROM address pointer, data can be read from the memory address with the current address pointer without specifying the word address.

As with writing, current address reading involves receiving the 7-bit device address and read command code “1” following the start condition, at which time the EEPROM generates an acknowledge signal. After this, the 8-bit data of the (n+1) address is output serially starting with the highest bits. After the 8 bits have been output, by not sending an acknowledge signal and inputting the stop condition, the EEPROM completes the read operation and is set to standby mode.

If the previous read address is the last address, the address for the current address reading is rolled over to become address 0.

* The current address assigned after a page write is the number of bytes written at the designated word address plus 1 if the volume of the write data is greater than 1 byte or less than or equal to 16 bytes, and is the designated word address if the volume of the write data is 16 bytes or more. If the last address of the page (A3 to A0 = 1111b) is specified as the word address for a byte write, the internal address after the write becomes the first address in that page (A3 to A0 = 0000b).

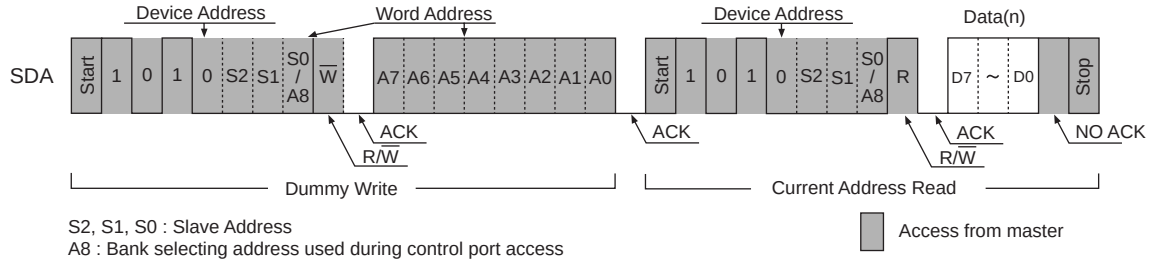


9-2. Random read

Random read is a mode in which any memory address is specified and its data read. The address is specified by a dummy write input.

First, when the EEPROM receives the 7-bit device address and write command code “0” following the start condition, it generates an acknowledge signal. It then receives the 8-bit word address, and generates an acknowledge signal. Through these operations, the word address is loaded into the address counter inside the EEPROM.

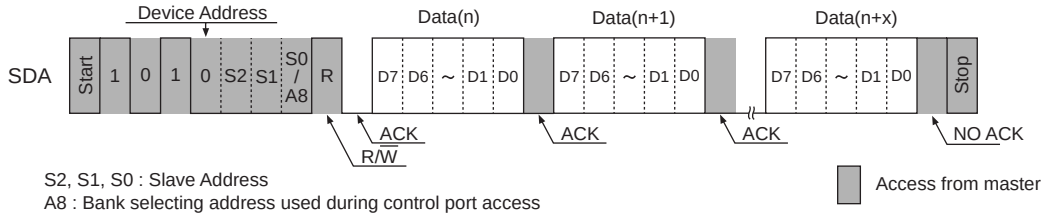
Next, the start condition is input again and the current read is initiated. This causes the data of the word address that was input using the dummy write input to be output. If, after the data is output, an acknowledge signal is not sent and the stop condition is input, reading is completed, and the EEPROM returns to standby mode.



9-3. Sequential read

In this mode, the data is read continuously, and sequential read operations can be performed with both current address read and random read. If, after the 8-bit data has been output, acknowledge “0” is input and reading is continued without issuing the stop condition, the address is incremented, and the data of the next address is output.
If acknowledge “0” continues to be input after the data has been output in this way, the data is successively output while the address is incremented. When the last address is reached, it is rolled over to address 0, and the data continues to be read. As with current address read and random read, the operation is completed by inputting the stop condition without sending an acknowledge signal.

*: For accesses from port 1 or port 2, the last address is FFh and for accesses to Bank1 or Bank2 from the control port, it is 1FFh. And, for accesses to the configuration area, the last address is Fh.



10. Operations during protect

The access level can be set for each port by using the values of the protect bits stored in the configuration area. However, access to the configuration area from the control port (device address 1011_100b) is always enabled regardless of the access level of the control port.

10-1. Access disabled state (PB1n=0, PB0n=0)

When the protect bits in the configuration area are set to”00b,” all the operations from the corresponding port are protected, and the access from the port is disabled. When a read or write operation is input from a port in this state, the product does not start the operation and enters the standby state. In addition, it does not return an acknowledge signal.

10-2. Read/write disabled state (PB1n=0, PB0n=1)

When the protect bits in the configuration area are set to “01b,” the read and write operations from the corresponding port are protected. When a read or write operation is input from a port in this state, the product returns an acknowledge signal and enters the standby state without initiating a read or write operation.
*: In read operations, the product generates an acknowledge signal on the high-to-low transition of the SCL clock in the 9^{th} cycle from the start condition. It enters the standby state on the low-to-high transition of the SCL clock in the same cycle.

10-3. Write prohibited state (PB1n=1, PB0n=0)

When the protect bits in the configuration area are set to “10b,” the write operations from the corresponding port are protected. When a write operation is input from a port in this state, the product returns an acknowledge signal and enters the standby state without initiating a write operation.

10-4. Read/write enabled state (PB1n=1, PB0n=1)

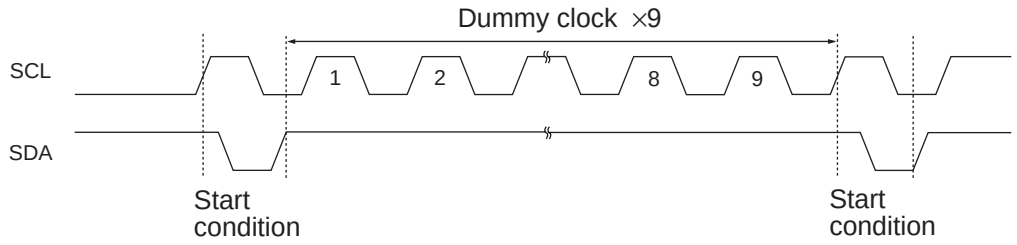
When the protect bits in the configuration area are set to “11b,” the read operations and write operations from the corresponding port are enabled.

Application Notes

1) Software reset function

Software reset (start condition + 9 dummy clock cycles + start condition), shown in the figure below, is executed in order to avoid erroneous operation after power-on and to reset while the command input sequence. During the dummy clock input period, the SDA bus must be opened (set to high by a pull-up resistor). Since it is possible for the ACK output and read data to be output from the EEPROM during the dummy clock period, forcibly entering H will result in an overcurrent flow.

Note that this software reset function does not work during the internal write cycle.



2) Pull-up resistor of SDA pin

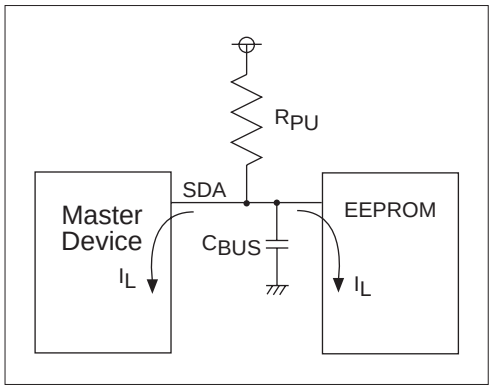
Due to the demands of the I^2C bus protocol function, the SDA pin must be connected to a pull-up resistor (with a resistance from several kΩ to several tens of kΩ) without fail. The appropriate value must be selected for this resistance (R_{PU}) on the basis of the V_{IL} and I_{IL} of the microcontroller and other devices controlling this product as well as the V_{OL}–I_{OL} characteristics of the product. Generally, when the resistance is too high, the operating frequency will be restricted; conversely, when it is too low, the operating current consumption will increase.

R_{PU} maximum resistance

The maximum resistance must be set in such a way that the bus potential, which is determined by the sum total (I_L) of the input leaks of the devices connected to the SDA bus and by R_{PU}, can completely satisfy the input high level (V_{IH} min) of the microcontroller and EEPROM. However, a resistance value that satisfies SDA rise time t_R and fall time t_F must be set.

R_{PU} maximum value = $(V_{DD} - V_{IH})/I_L$

Example: When V_{DD}=3.0V and I_L= 2μA
R_{PU} maximum value = (3.0V – 3.0V × 0.8)/2μA = 300kΩ



R_{PU} minimum value

A resistance corresponding to the low-level output voltage (V_{OL} max) of SANYO's EEPROM must be set.

R_{PU} minimum value = $(V_{DD} - V_{OL})/I_{OL}$

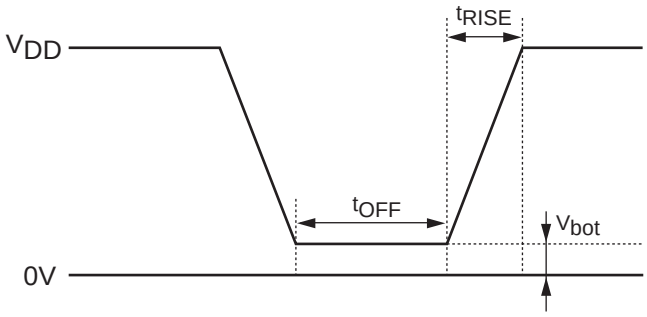
Example: When V_{DD}=3.0V, V_{OL} = 0.4V and I_{OL} = 1mA
R_{PU} minimum value = (3.0V – 0.4)/1mA = 2.6kΩ

Recommended R_{PU} setting

R_{PU} is set to strike a good balance between the operating frequency requirements and power consumption. If it is assumed that the SDA load capacitance is 50pF and the SDA output data strobe time is 500ns, R_{PU} will be about R_{PU} = 500ns/50pF = 10kΩ.

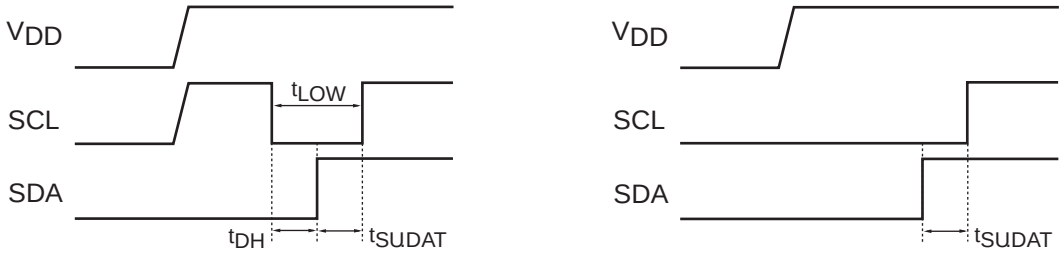
3) Precautions when turning on the power
This product contains a power-on reset circuit for preventing the inadvertent writing of data when the power is turned on. The following conditions must be met in order to ensure stable operation of this circuit. No data guarantees are given in the event of an instantaneous power failure during the internal write operation.

Item	Symbol	V_{DD}=2.5 to 5.5V			unit
		min	typ	max	
Power rise time	t_{RISE}			100	ms
Power off time	t_{OFF}	10			ms
Power bottom voltage	V_{bot}			0.2	V



Notes:
1) The SDA pin must be set to high and the SCL pin to low or high.
2) Steps must be taken to ensure that the SDA and SCL pins are not placed in a high-impedance state.

A. If it is not possible to satisfy the instruction 1 in Note above, and SDA is set to low during power rise
After the power has stabilized, the SCL and SDA pins must be controlled as shown below, with both pins set to high.



B. If it is not possible to satisfy the instruction 2 in Note above
After the power has stabilized, software reset must be executed.

C. If it is not possible to satisfy the instructions both 1 and 2 in Note above
After the power has stabilized, the steps in A must be executed, then software reset must be executed.

4) Noise filter for the SCL and SDA pins
This product contains a filter circuit for eliminating noise at the SCL and SDA pins. Pulses of 100ns or less are not recognized because of this function.

5) Function to inhibit writing when supply voltage is low
This product contains a supply voltage monitoring circuit that inhibits inadvertent writing below the guaranteed operating supply voltage range. The data is protected by ensuring that write operations are not started at voltages (typ.) of 1.3V and below.

6) Initial values in the configuration
The slave address values as well as the slave address enable bit and protect bit values of the ports are stored in the configuration area. These values are set as follows when the EEPROM is shipped:
- Slave address values: “000b” for all ports
- Slave address enable bits: “1b” for all ports (enabled)
- Protect bit values: “11b” for all ports (no protection)

When these values are to be changed, input the device address “1011_100b” from the control port, and perform the write operation.

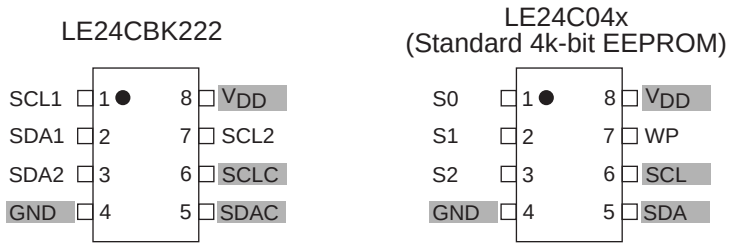
7) Precautions when changing the mode

This product enables to actively change the bank accessing mode during period in which no write operation is performed between the bank operation mode (access from port 1 or port 2 to Bank1 or Bank2) and the combined operation mode (access from the control port to both banks). However, the current address value for each mode is not held internally. When conducting read operations after changing the mode, random access read must be performed without fail.

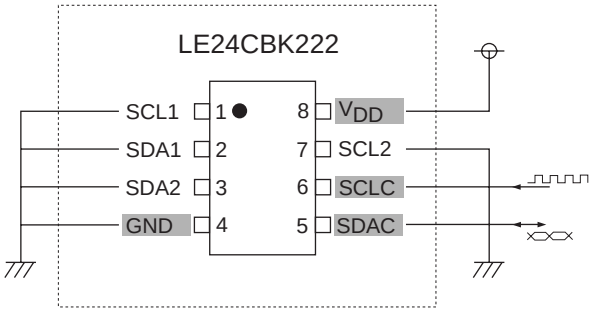
When switching the bank accessing mode, start the operations in the next mode after the operations in the previous mode have been completed (when the stop condition is input or no acknowledge “0” input for a sequential read).

8) Writing with a ROM writer from the control port

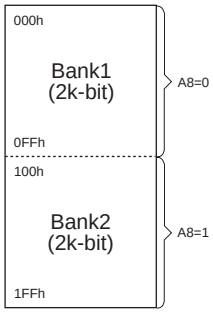
This product enables two-bank configuration (2K bits + 2K bits) to be used as a pseudo-one-bank configuration (4K bits) by accessing the memory areas from the control port (SCLC, SDAC). As a result, data can be written using a ROM writer with the EEPROM serving as a regular 4K-bit EEPROM. Fix the port 1 and port 2 pins to high or low.



ROM writer connection example



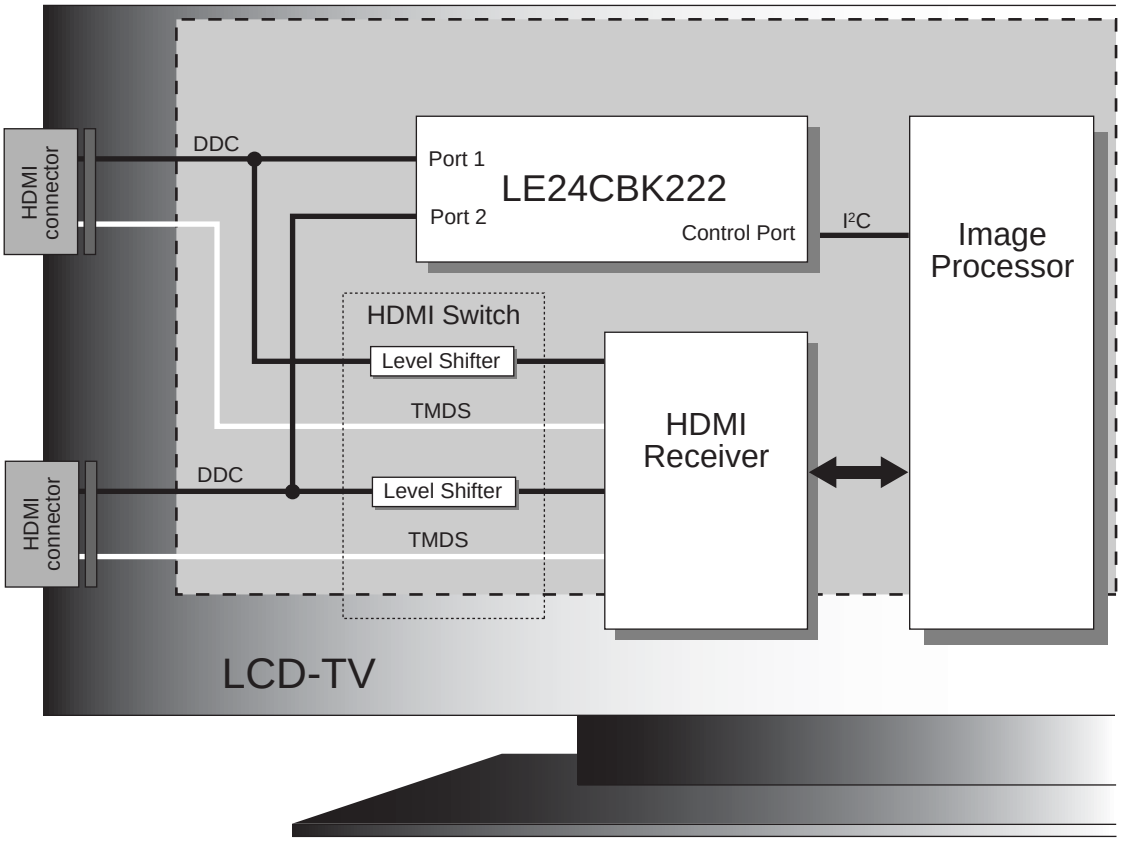
Memory Area (4K-bit)



The MSB address in combined mode is A8. A8 is used to select the Bank1 or Bank2 area. Set A8 = 0 to control the Bank1 area, or A8 = 1 to control the Bank2 area.

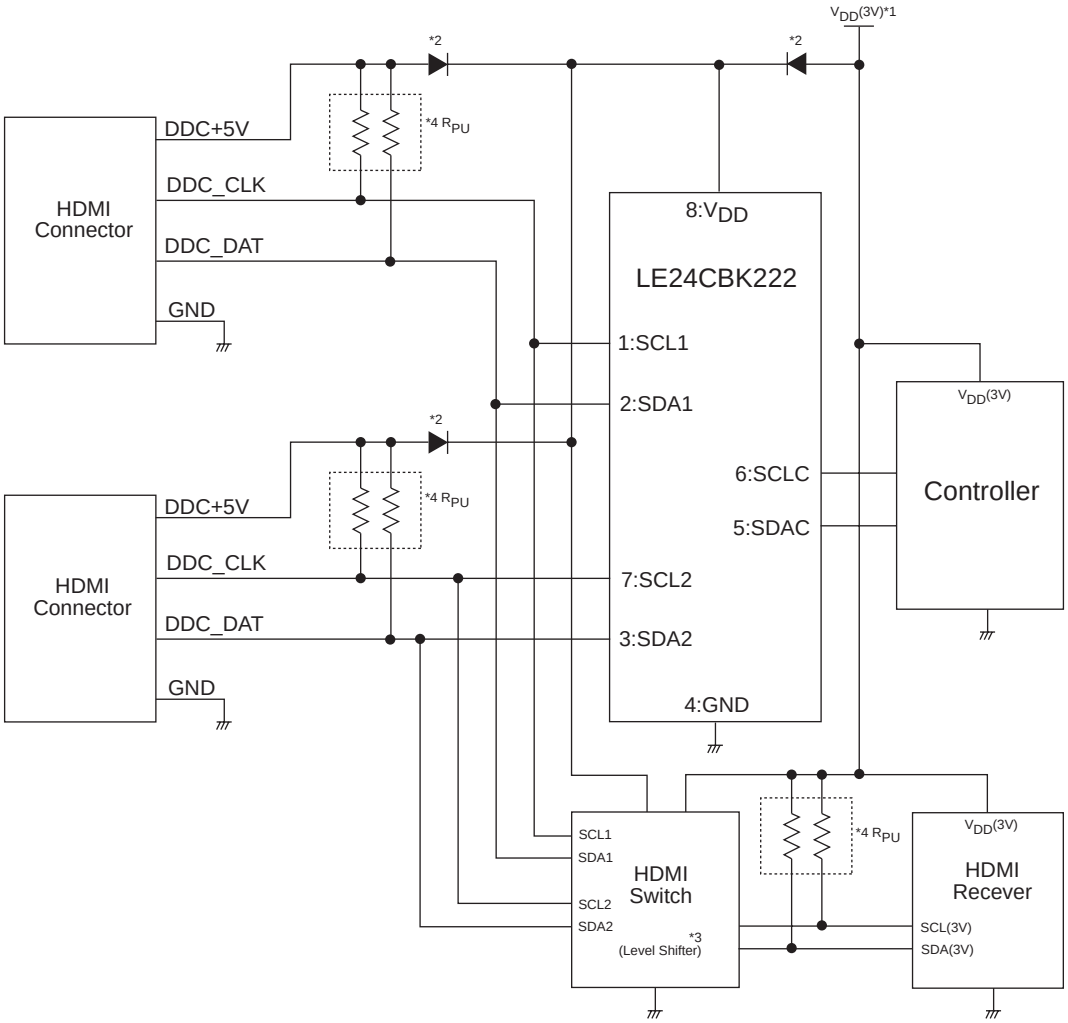
10) System Configuration Image
(HDMI System)

This product can support two HDMI ports simultaneously. Both ports can be accessed at the same time when performing read operations of the ports. All the data can be written together from a image processor into the areas allocated to the two ports from the control port in a single operation.



10) Peripheral Circuit Diagram

Example of connection with HDMI receiver



*1: System power supply (3V) for HDMI receiver, etc.

*2: Reverse-current preventing diode

This device can be operated by supplying power from any of the connected HDMI connectors (DDC + 5V) or the system power supply (3V). However, the supply voltage must be set so that the voltage stepped-down by the reverse-current preventing diode is within the guaranteed operation voltage range of this device.

*3: Level shifter

When connecting the 5V HDMI connector side with a 3V system, level shifters must generally be inserted. However, this is not necessary when the HDMI receiver supports 5V input signals.

*4: Pull-up resistors for the I^2C and DDC interfaces.

See item 2) in the Application Notes for the resistance value settings.