DS89C430/DS89C440/DS89C450
Ultra-High-Speed Flash Microcontrollers

www.maxim-ic.com

GENERAL DESCRIPTION

The DS89C430, DS89C440, and DS89C450 offer the highest performance available in 8051-compatible microcontrollers. They feature newly designed processor cores that execute instructions up to 12 times faster than the original 8051 at the same crystal speed. Typical applications will experience a speed improvement up to 10x. At 1 million instructions per second (MIPS) per megahertz, the microcontrollers achieve 33 MIPS performance from a maximum 33MHz clock rate.

The *Ultra-High-Speed Flash Microcontroller User's Guide* should be used in conjunction with this data sheet. **Download it at www.maxim-ic.com/microcontrollers.**

APPLICATIONS

Data Logging
Automotive Test Equipment
Magstripe Reader/Scanner
Gaming Equipment
HVAC
Uninterruptible Power Supplies
Building Energy Control and Management
White Goods (Washers, Microwaves, etc.)
Vending
Motor Control
Consumer Electronics
Telephones
Programmable Logic Controllers
Building Security and Door Access Control
Industrial Control and Automation

ORDERING INFORMATION

PART	FLASH MEMORY SIZE	PIN-PACKAGE
DS89C430-MNL	16kB x 8	40 PDIP
DS89C430-QNL	16kB x 8	44 PLCC
DS89C430-ENL	16kB x 8	44 TQFP
DS89C440-MNL	32kB x 8	40 PDIP
DS89C440-QNL	32kB x 8	44 PLCC
DS89C440-ENL	32kB x 8	44 TQFP
DS89C450-MNL	64kB x 8	40 PDIP
DS89C450-QNL	64kB x 8	44 PLCC
DS89C450-ENL	64kB x 8	44 TQFP

Complete Selector Guide appears at end of data sheet.

Pin Configurations appear at end of data sheet.

FEATURES

- **High-Speed 8051 Architecture**
  - One Clock-Per-Machine Cycle
  - DC to 33MHz Operation
  - Single Cycle Instruction in 30ns
  - Optional Variable Length MOVX to Access Fast/Slow Peripherals
  - Dual Data Pointers with Automatic Increment/Decrement and Toggle Select
  - Supports Four Paged Memory-Access Modes
- **On-Chip Memory**
  - 16kB/32kB/64kB Flash Memory
  - In-Application Programmable
  - In-System Programmable Through Serial Port
  - 1kB SRAM for MOVX
- **80C52 Compatible**
  - 8051 Pin and Instruction Set Compatible
  - Four Bidirectional, 8-Bit I/O Ports
  - Three 16-Bit Timer Counters
  - 256 Bytes Scratchpad RAM
- **Power-Management Mode**
  - Programmable Clock Divider
  - Automatic Hardware and Software Exit
- **ROMSIZE Feature**
  - Selects Internal Program Memory Size from 0 to 64kB
  - Allows Access to Entire External Memory Map
  - Dynamically Adjustable by Software
- **Peripheral Features**
  - Two Full-Duplex Serial Ports
  - Programmable Watchdog Timer
  - 13 Interrupt Sources (Six External)
  - Five Levels of Interrupt Priority
  - Power-Fail Reset
  - Early Warning Power-Fail Interrupt
  - Electromagnetic Interference (EMI) Reduction

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground……..-0.3V to +6.0V
Ambient Temperature Range (under bias)……-40°C to +85°C
Storage Temperature Range……-55°C to +125°C
Soldering Temperature……See IPC/JEDEC J-STD-020A

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage (Notes 2, 3)	V_{CC}	4.5	5.0	5.5	V
Power-Fail Warning (Notes 2, 4)	V_{PFW}	4.2	4.375	4.6	V
Reset Trip Point (Min Operating Voltage) (Notes 2, 3, 4)	V_{RST}	3.95	4.125	4.35	V
Supply Current, Active Mode (Note 5)	I_{CC}		75	110	mA
Supply Current, Idle Mode at 33MHz (Note 6)	I_{IDLE}		40	50	mA
Supply Current, Stop Mode, Bandgap Disabled (Note 7)	I_{STOP}		1	100	µA
Supply Current, Stop Mode, Bandgap Enabled (Note 7)	I_{SPBG}		150	300	µA
Input Low Level (Note 2)	V_{IL}	-0.3		+0.8	V
Input High Level (Note 2)	V_{IH}	2.0		V_{CC} + 0.3	V
Input High Level XTAL and RST (Note 2)	V_{IH2}	3.5		V_{CC} + 0.3	V
Output Low Voltage, Port 1 and 3 at I_{OL} = 1.6mA (Note 2)	V_{OL1}		0.15	0.45	V
Output Low Voltage, Port 0 and 2, ALE, $\overline{PSEN}$ at I_{OL} = 3.2mA (Note 2)	V_{OL2}		0.15	0.45	V
Output High Voltage, Port 1, 2, and 3, at I_{OH} = -50µA (Notes 2, 8)	V_{OH1}	2.4			V
Output High Voltage, Port 1, 2, and 3 at I_{OH} = -1.5mA (Notes 2, 9)	V_{OH2}	2.4			V
Output High Voltage, Port 0, 1, 2, ALE, $\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$ in Bus Mode at I_{OH} = -8mA (Notes 2, 10)	V_{OH3}	2.4			V
Output High Voltage, RST at I_{OL} = -0.4mA (Note 2, 11)	V_{OH4}	2.4			V
Input Low Current, Port 1, 2, and 3 at 0.4V	I_{IL}	-50			µA
Transition Current from 1 to 0, Port 1, 2, and 3 at 2V (Note 12)	I_{TL}	-650			µA
Input Leakage Current, Port 0 in I/O Mode and $\overline{EA}$ (Note 13)	I_L	-10		+10	µA
Input Current, Port 0 in Bus Mode (Note 14)	I_L	-300		+300	µA
RST Pulldown Resistance (Note 13)	R_{RST}	50	120	200	kΩ

Note 1: Specifications to -40°C are guaranteed by design and not production tested.

Note 2: All voltages are referenced to ground.

Note 3: The user should note that this part is tested and guaranteed to operate down to 4.5V (10%) and that V_{RST} (min) is specified below that point. This indicates that there is a range of voltages [(V_{MIN} to V_{RST} (min)] where the processor's operation is not guaranteed, but the reset trip point has not been reached. This should not be an issue in most applications, but should be considered when proper operation must be maintained at all times. For these applications, it may be desirable to use a more accurate external reset.

Note 4: While the specifications for V_{PFW} and V_{RST} overlap, the design of the hardware makes it so this is not possible. Within the ranges given, there is guaranteed separation between these two voltages.

Note 5: Active current is measured with a 33MHz clock source driving XTAL1, V_{CC} = RST = 5.5V. All other pins are disconnected.

Note 6: Idle mode current is measured with a 33MHz clock source driving XTAL1, V_{CC} = 5.5V, RST at ground. All other pins are disconnected.

Note 7: Stop mode is measured with XTAL and RST grounded, V_{CC} = 5.5V. All other pins are disconnected.

Note 8: RST = 5.5V. This condition mimics the operation of pins in I/O mode.

Note 9: During a 0-to-1 transition, a one shot drives the ports hard for two clock cycles. This measurement reflects a port pin in transition mode.

Note 10: When addressing external memory.

Note 11: Guaranteed by design.

Note 12: Ports 1, 2, and 3 source transition current when pulled down externally. The current reaches its maximum at approximately 2V.

Note 13: RST = 5.5V. Port 0 is floating during reset and when in the logic-high state during I/O mode.

Note 14: This port is a weak address holding latch in bus mode. Peak current occurs near the input transition point of the holding latch at approximately 2V.

AC CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.) (See Figure 1, Figure 2, and Figure 3.)

PARAMETER	SYMBOL	1-CYCLE PAGE MODE 1		2-CYCLE PAGE MODE 1		4-CYCLE PAGE MODE 1		PAGE MODE 2		NONPAGE MODE		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
System Clock External Oscillator (Note 15)	$1/t_{CLCL}$	0	33	0	33	0	33	0	33	0	33	MHz
System Clock External Crystal (Note 15)	$1/t_{CLCL}$	1	33	1	33	1	33	1	33	1	33	
ALE Pulse Width (Note 16)	t_{LHLL}	$0.5t_{CLCL}$ - 2 + t_{STC3}		t_{CLCL} - 2 + t_{STC3}		$2t_{CLCL}$ - 4 + t_{STC3}		$1.5t_{CLCL}$ - 5 + t_{STC3}		$1.5t_{CLCL}$ - 5 + t_{STC3}		ns
Port 0 Instruction Address Valid to ALE Low	t_{AVLL}							t_{CLCL} - 3		$0.5t_{CLCL}$ - 3		ns
Port 2 Instruction Address Valid to ALE Low	t_{AVLL2}	$0.5t_{CLCL}$ - 4		$0.5t_{CLCL}$ - 4		$1.5t_{CLCL}$ - 4		$0.5t_{CLCL}$ - 4		t_{CLCL} - 4		ns
Port 0 Data AddressValid to ALE Low	t_{AVLL3}							t_{CLCL} - 3 + t_{STC3}		$0.5t_{CLCL}$ - 3 + t_{STC3}		ns
Program Address Hold After ALE Low	t_{LLAX}	$0.5t_{CLCL}$ - 8		$1.5t_{CLCL}$ - 8		$2.5t_{CLCL}$ - 8		$1t_{CLCL}$ - 10		$1t_{CLCL}$ - 10		ns
Address Hold after ALE Low MOVX Write	t_{LLAX2}	$0.5t_{CLCL}$ - 8 + t_{STC4}		$1.5t_{CLCL}$ - 8 + t_{STC4}		$2.5t_{CLCL}$ - 8 + t_{STC3}		$0.5t_{CLCL}$ - 8 + t_{STC2}		$0.5t_{CLCL}$ - 8 + t_{STC2}		ns
Address Hold after ALE Low MOVX Read	t_{LLAX3}	$0.5t_{CLCL}$ - 8 + t_{STC4}		$1.5t_{CLCL}$ - 8 + t_{STC4}		$2.5t_{CLCL}$ - 8 + t_{STC3}		$0.5t_{CLCL}$ - 8 + t_{STC3}		$0.5t_{CLCL}$ - 8 + t_{STC2}		ns
ALE Low to Valid Instruction In	t_{LLIV}								$2t_{CLCL}$ - 6		$2t_{CLCL}$ - 6	ns
ALE Low to $\overline{PSEN}$ Low	t_{LLPL}							$1.5t_{CLCL}$ - 6		$0.5t_{CLCL}$ - 2		ns
$\overline{PSEN}$ Pulse Width for Program Fetch	t_{PLPH}	t_{CLCL} - 5		t_{CLCL} - 5		$2t_{CLCL}$ - 5		t_{CLCL} - 5		$2t_{CLCL}$ - 5		ns

AC CHARACTERISTICS (continued)

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.) (See Figure 1, Figure 2, and Figure 3.)

PARAMETER	SYMBOL	1-CYCLE PAGE MODE 1		2-CYCLE PAGE MODE 1		4-CYCLE PAGE MODE 1		PAGE MODE 2		NONPAGE MODE		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$\overline{PSEN}$ Low to Valid Instruction In	t_{PLIV}		t_{CLCL} - 20		t_{CLCL} - 20		$2t_{CLCL}$ - 20		t_{CLCL} - 20		$2t_{CLCL}$ - 20	ns
Input Instruction Hold After $\overline{PSEN}$	t_{PXIX}	0		0		0		0		0		ns
Input Instruction Float After $\overline{PSEN}$	t_{PXIZ}								t_{CLCL} - 5		t_{CLCL} - 5	ns
Port 0 Address to Valid Instruction In	t_{AVIV0}								$1.5t_{CLCL}$ - 22		$3t_{CLCL}$ - 22	ns
Port 2 Address to Valid Instruction In	t_{AVIV2}		t_{CLCL} - 20		$1.5t_{CLCL}$ - 20		$2.5t_{CLCL}$ - 20		$3t_{CLCL}$ - 20		$3.5t_{CLCL}$ - 20	ns
$\overline{PSEN}$ Low to Port 0 Address Float	t_{PLAZ}								0		0	ns
$\overline{RD}$ Pulse Width (P3.7) (Note 16)	t_{RLRH}	t_{CLCL} - 5 + t_{STC1}		t_{CLCL} - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		ns
$\overline{WR}$ Pulse Width (P3.6) (Note 16)	t_{WLWH}	t_{CLCL} - 5 + t_{STC1}		t_{CLCL} - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		ns
$\overline{RD}$ (P3.7) Low to Valid Data In (Note 16)	t_{RLDV}		t_{CLCL} - 18 + t_{STC1}		t_{CLCL} - 18 + t_{STC1}		$2t_{CLCL}$ - 18 + t_{STC1}		$2t_{CLCL}$ - 18 + t_{STC1}		$2t_{CLCL}$ - 18 + t_{STC1}	ns
Data Hold After $\overline{RD}$ (P3.7)	t_{RHDX}	0		0		0		0		0		ns
Data Float After $\overline{RD}$ (P3.7)	t_{RHDZ}								t_{CLCL} - 5		t_{CLCL} - 5	ns
MOVX ALE Low to Input Data Valid (Note 16)	t_{LLDV}								$2t_{CLCL}$ - 8 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}	ns

AC CHARACTERISTICS (continued)

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.) (See Figure 1, Figure 2, and Figure 3.)

PARAMETER	SYMBOL	1-CYCLE PAGE MODE 1		2-CYCLE PAGE MODE 1		4-CYCLE PAGE MODE 1		PAGE MODE 2		NONPAGE MODE		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Port 0 Address to Valid Data In (Note 16)	t_{AVDV0}								$3t_{CLCL}$ - 20 + t_{STC1}		$3t_{CLCL}$ - 20 + t_{STC1}	ns
Port 2 Address to Valid Data In (Note 16)	t_{AVDV2}		t_{CLCL} - 20 + t_{STC1}		$1.5t_{CLCL}$ - 20 + t_{STC1}		$3.5t_{CLCL}$ - 20 + t_{STC1}		$3.0t_{CLCL}$ - 20 + t_{STC1}		$3.5t_{CLCL}$ - 20 + t_{STC1}	ns
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low (Note 16)	t_{LLRL} (t_{LLWL})	$0.5t_{CLCL}$ - 8 + t_{STC2}	$0.5t_{CLCL}$ + 6 + t_{STC2}	$2t_{CLCL}$ - 8 + t_{STC2}	$2t_{CLCL}$ + 6 + t_{STC2}	$4t_{CLCL}$ - 8 + t_{STC2}	$4t_{CLCL}$ + 6 + t_{STC2}	$0.5t_{CLCL}$ - 8 + t_{STC2}	$0.5t_{CLCL}$ + 4 + t_{STC2}	$0.5t_{CLCL}$ - 8 + t_{STC2}	$0.5t_{CLCL}$ + 5 + t_{STC2}	ns
Port 0 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low (Note 16)	t_{AVRL0} (t_{AVWL0})							$1.5t_{CLCL}$ - 5 + t_{STC2}		t_{CLCL} - 5 + t_{STC2}		ns
Port 2 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low (Note 16)	t_{AVRL2} (t_{AVWL2})	0 + t_{STC5} - 5		$0.5t_{CLCL}$ - 5 + t_{STC5}		$1.5t_{CLCL}$ - 5 + t_{STC5}		t_{CLCL} - 5 + t_{STC5}		$1.5t_{CLCL}$ - 5 + t_{STC5}		ns
Data Out Valid to $\overline{WR}$ Transition (Note 15)	t_{QVWX}	-5		-5		-5		-5		-5		ns
Data Hold After $\overline{WR}$ (Note 15)	t_{WHQX}	t_{CLCL} + t_{STC2} - 10		t_{CLCL} + t_{STC2} - 10		t_{CLCL} + t_{STC2} - 10		t_{CLCL} + t_{STC2} - 10		t_{CLCL} + t_{STC2} - 10		ns
$\overline{RD}$ or $\overline{WR}$ High to ALE High (Note 15)	t_{RHLH} (t_{WHLH})	t_{STC2} - 2	t_{STC2} + 4	t_{STC2} - 2	t_{STC2} + 4	t_{STC2} - 2	t_{STC2} + 4	t_{STC2} - 2	t_{STC2} + 4	t_{STC2} - 2	t_{STC2} + 4	ns

Note: Specifications to -40°C are guaranteed by design and are not production tested. AC electrical characteristics assume 50% duty cycle for the oscillator and are not 100% tested, but are guaranteed by design.

Note 15: The clock divide and crystal multiplier control bits in the PMR register determine the system clock frequency and the minimum/maximum external clock speed. The term "$1/t_{CLCL}$" used in the *AC Characteristics* variable timing table is determined from the following table. The minimum/maximum external clock speed columns clarify that [(external clock speed) x (multipliers)] cannot exceed the rated speed of the device. In addition, the use of the crystal multiplier feature establishes a minimum external speed.

4X/$\overline{2X}$	CD1	CD0	Number of External Clock Cycles per System Clock ($1/t_{CLCL}$)	External Clock Speed	
				Min	Max
1	0	0	1/4	5MHz	8.25MHz
0	0	0	1/2	10MHz	16.5MHz
X	0	1	Reserved	—	—
X	1	0	1	See AC Characteristics	See AC Characteristics
X	1	1	1024	See AC Characteristics	See AC Characteristics

Note 16: External MOVX instruction times are dependent upon the setting of the MD2, MD1, and MD0 bits in the clock control register. The terms "t_{STC1}, t_{STC2}, t_{STC3}" used in the variable timing table above are calculated through the use of the table given below.

MD2	MD1	MD0	MOVX Instruction Time	t_{STC1}	t_{STC2}	t_{STC3}	t_{STC4}	t_{STC5}
0	0	0	2 Machine Cycles	0 t_{CLCL}	0 t_{CLCL}	0 t_{CLCL}	0 t_{CLCL}	0 t_{CLCL}
0	0	1	3 Machine Cycles	2 t_{CLCL}	1 t_{CLCL}	0 t_{CLCL}	0 t_{CLCL}	1 t_{CLCL}
0	1	0	4 Machine Cycles	6 t_{CLCL}	1 t_{CLCL}	0 t_{CLCL}	0 t_{CLCL}	1 t_{CLCL}
0	1	1	5 Machine Cycles	10 t_{CLCL}	1 t_{CLCL}	0 t_{CLCL}	0 t_{CLCL}	1 t_{CLCL}
1	0	0	6 Machine Cycles	14 t_{CLCL}	5 t_{CLCL}	4 t_{CLCL}	1 t_{CLCL}	1 t_{CLCL}
1	0	1	7 Machine Cycles	18 t_{CLCL}	5 t_{CLCL}	4 t_{CLCL}	1 t_{CLCL}	1 t_{CLCL}
1	1	0	8 Machine Cycles	22 t_{CLCL}	5 t_{CLCL}	4 t_{CLCL}	1 t_{CLCL}	1 t_{CLCL}
1	1	1	9 Machine Cycles	26 t_{CLCL}	5 t_{CLCL}	4 t_{CLCL}	1 t_{CLCL}	1 t_{CLCL}

Note 17: Maximum load capacitance (to meet the above timing) for Port 0, ALE, $\overline{PSEN}$, $\overline{WR}$, and $\overline{RD}$ is limited to 60pF. XTAL1 and XTAL2 load capacitance are dependent upon the frequency of the selected crystal.

Figure 1. Nonpage Mode Timing

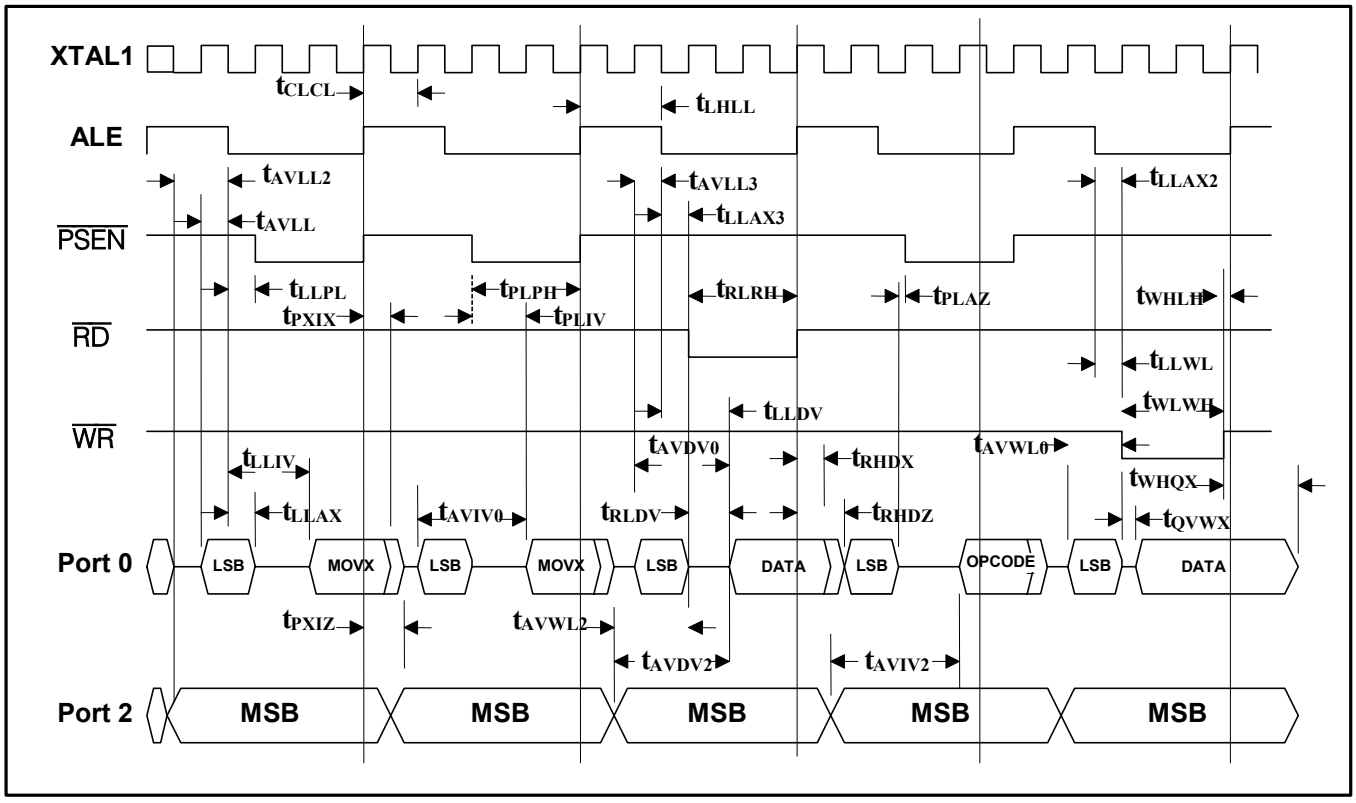


Figure 2. Page Mode 1 Timing

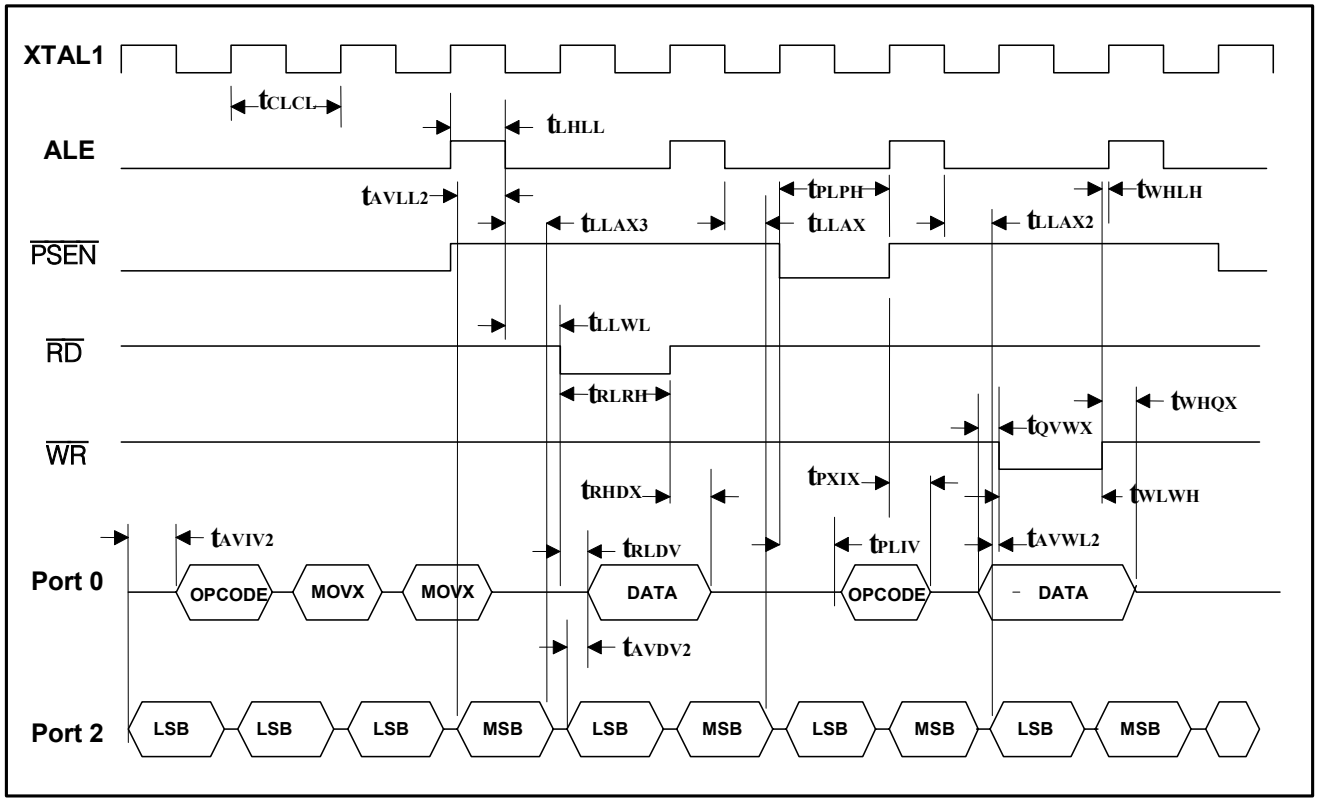
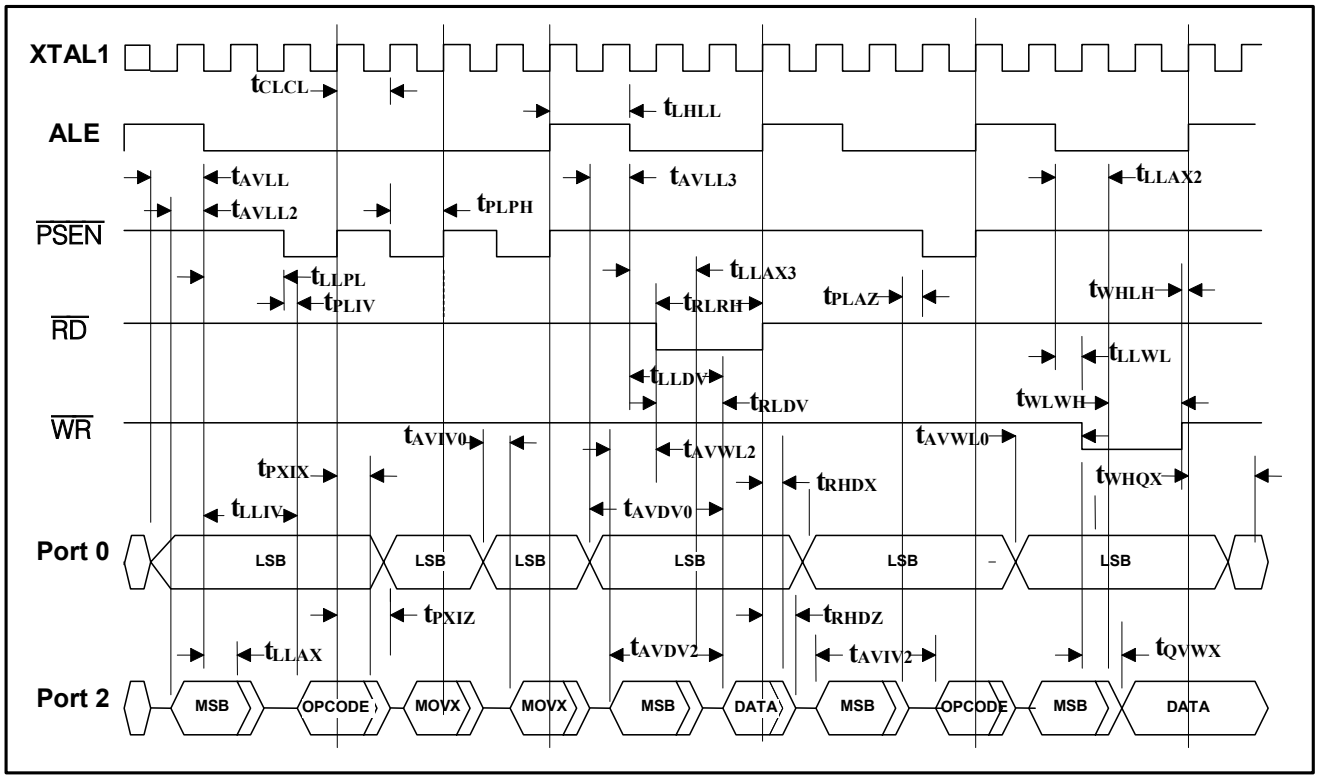


Figure 3. Page Mode 2 Timing



EXTERNAL CLOCK CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Clock High Time	t_{CHCX}	10		ns
Clock Low Time	t_{CLCX}	10		ns
Clock Rise Time	t_{CLCH}		5	ns
Clock Fall Time	t_{CHCL}		5	ns

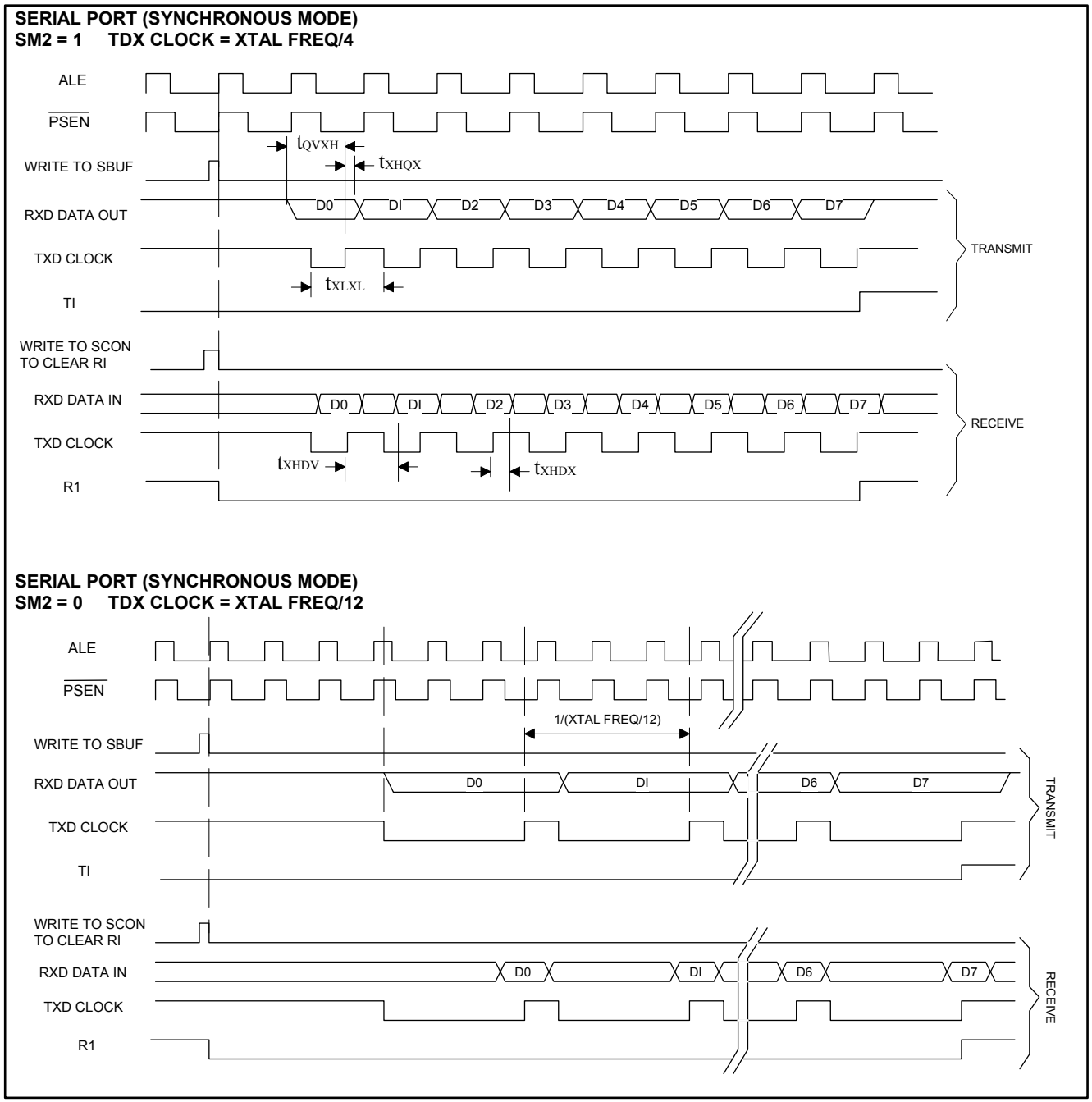
SERIAL PORT MODE 0 TIMING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.) (Figure 4)

PARAMETER	SYMBOL	CONDITIONS	33MHz		VARIABLE		UNITS
			MIN	MAX	MIN	MAX	
Clock Cycle Time	t_{XLXL}	SM2 = 0	360		$12t_{CLCL}$		ns
		SM2 = 1	120		$4t_{CLCL}$		ns
Output Data Setup to Clock Rising	t_{QVXH}	SM2 = 0	200		$10t_{CLCL}$ - 100		ns
		SM2 = 1	40		$3t_{CLCL}$ - 10		ns
Output Data Hold to Clock Rising	t_{XHQX}	SM2 = 0	50		$2t_{CLCL}$ - 10		ns
		SM2 = 1	20		t_{CLCL} - 100		
Input Data Hold After Clock Rising	t_{XHDX}	SM2 = 0	0		0		ns
		SM2 = 1	0		0		
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0		200		$10t_{CLCL}$ - 100	ns
		SM2 = 1		40		$3t_{CLCL}$ - 50	ns

Note: SM2 is the serial port 0 mode bit 2. When serial port 0 is operating in mode 0 (SM0 = SM1 = 0), SM2 determines the number of crystal clocks in a serial port clock cycle.

Figure 4. Serial Port Timing



POWER-CYCLE TIMING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Crystal Startup Time (Note 18)	t_{CSU}		8		ms
Power-On Reset Delay (Note 19)	t_{POR}		65,536		t_{CLCL}

Note 18: Startup time for a crystal varies with load capacitance and manufacturer. The time shown is for an 11.0592MHz crystal manufactured by Fox Electronics.

Note 19: Reset delay is a synchronous counter of crystal oscillations after crystal startup. Counting begins when the level on the XTAL1 pin meets the V_{IH2} criteria. At 33MHz, this time is 1.99ms.

FLASH MEMORY PROGRAMMING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Data Retention	t_{DR}	100			years
Write/Erase Endurance	t_{ENDURE}	10,000			cycles
Program/Time	t_{PROG}			40	µs
Erase Time	t_{ERASE}	4			ms

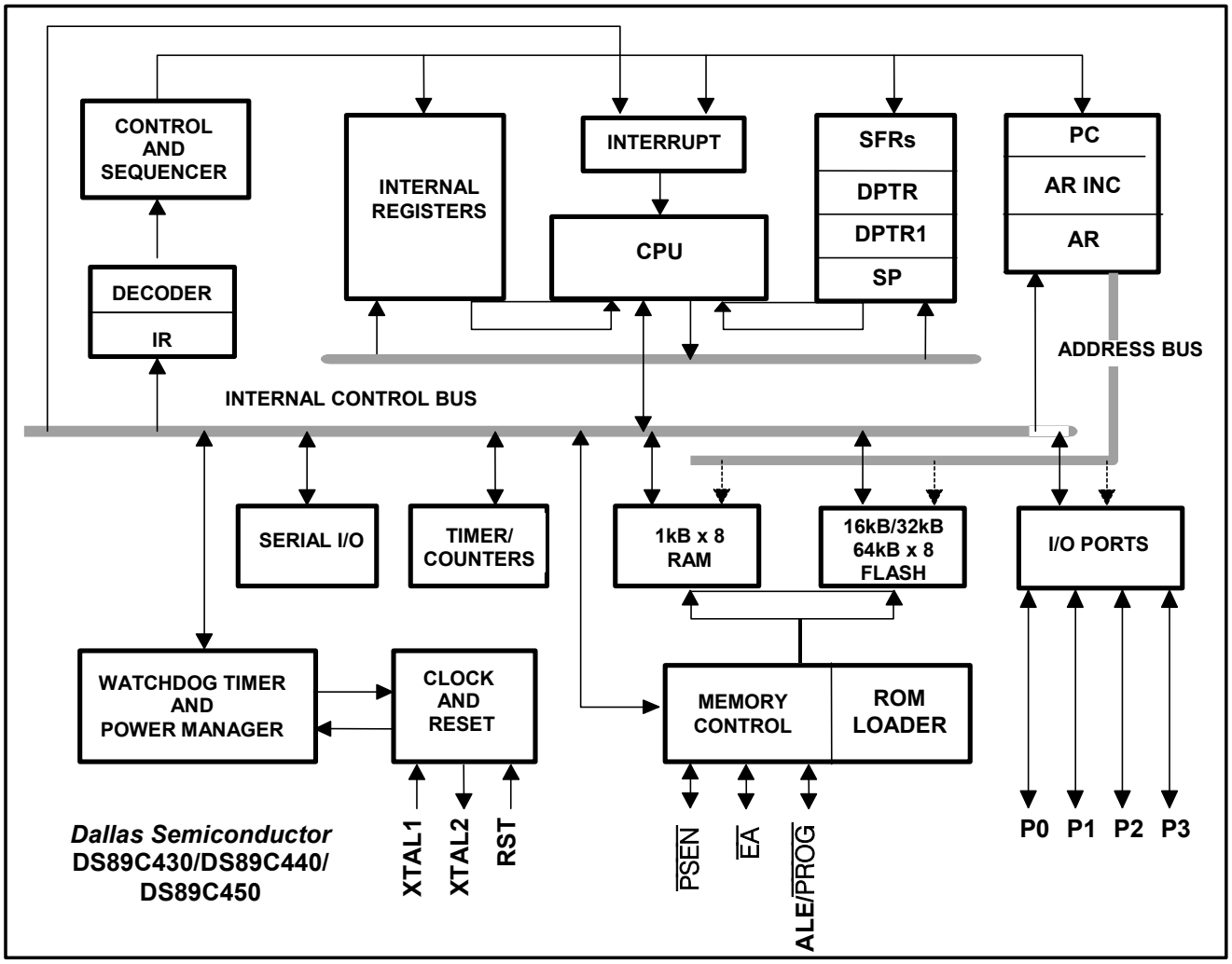
PIN DESCRIPTION

PIN			NAME	FUNCTION
PDIP	PLCC	TQFP		
40	12, 44	6, 38	V_{CC}	**+5V**
20	1, 22, 23, 34	16, 17, 28, 39	GND	**Logic Ground**
9	10	4	RST	**External Reset.** The RST input pin is bidirectional and contains a Schmitt Trigger to recognize external active-high reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wire-ORed external reset sources. An RC is not required for power-up, as the device provides this function internally.
19	21	15	XTAL1	**Crystal Oscillators.** These pins provide support for fundamental-mode parallel-resonant AT-cut crystals. XTAL1 also acts as an input if there is an external clock source in place of a crystal. XTAL2 serves as the output of the crystal amplifier.
18	20	14	XTAL2	
29	32	26	$\overline{PSEN}$	**Program Store Enable.** This signal is commonly connected to optional external program memory as a chip enable. $\overline{PSEN}$ provides an active-low pulse and is driven high when external program memory is not being accessed. In one-cycle page mode 1, $\overline{PSEN}$ remains low for consecutive page hits.
30	33	27	ALE/$\overline{PROG}$	**Address Latch Enable.** This signal functions as a clock to latch the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external 373-family transparent latch. In default mode, ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. In page mode, the ALE pulse width is altered according to the page mode selection. In traditional 8051 mode, ALE is high when using the EMI reduction mode and during a reset condition. ALE can be enabled by writing ALEON = 1 (PMR.2). Note that ALE operates independently of ALEON during external memory accesses. As an alternate mode, this pin ($\overline{PROG}$) is used to execute the parallel program function.
39	43	37	P0.0 (AD0)	**Port 0 (AD0–AD7), I/O.** Port 0 is an open-drain, 8-bit, bidirectional I/O port. As an alternate function, Port 0 can function as the multiplexed address/data bus to access off-chip memory. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls to logic 0, the port transitions to a bidirectional data bus. This bus is used to read external program memory and read/write external RAM or peripherals. When used as a memory bus, the port provides weak pullups for logic 1 outputs. The reset condition of port 0 is tri-state. Pullup resistors are required only when using port 0 as an I/O port.
38	42	36	P0.1 (AD1)	
37	41	35	P0.2 (AD2)	
36	40	34	P0.3 (AD3)	
35	39	33	P0.4 (AD4)	
34	38	32	P0.5 (AD5)	
33	37	31	P0.6 (AD6)	
32	36	30	P0.7 (AD7)	

PIN DESCRIPTION (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>PDIP</th><th>PLCC</th><th>TQFP</th></tr>
<tr><td>1</td><td>2</td><td>40</td><td>P1.0</td><td rowspan="8">Port 1, I/O. Port 1 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for timer 2 I/O, new external interrupts, and new serial port 1. The reset condition of port 1 is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input state, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C430/DS89C440/DS89C450 activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes the output high (and input) state. The alternate functions of port 1 are as follows:
PORT ALTERNATE FUNCTION
P1.0 T2 External I/O for Timer/Counter2
P1.1 T2EX Timer 2 Capture/Reload Trigger
P1.2 RXD1 Serial Port 1 Receive
P1.3 TXD1 Serial Port 1 Transmit
P1.4 INT2 External Interrupt 2 (Positive Edge Detect)
P1.5 $\overline{INT3}$ External Interrupt 3 (Negative Edge Detect)
P1.6 INT4 External Interrupt 4 (Positive Edge Detect)
P1.7 $\overline{INT5}$ External Interrupt 5 (Negative Edge Detect)</td></tr>
<tr><td>2</td><td>3</td><td>41</td><td>P1.1</td></tr>
<tr><td>3</td><td>4</td><td>42</td><td>P1.2</td></tr>
<tr><td>4</td><td>5</td><td>43</td><td>P1.3</td></tr>
<tr><td>5</td><td>6</td><td>44</td><td>P1.4</td></tr>
<tr><td>6</td><td>7</td><td>1</td><td>P1.5</td></tr>
<tr><td>7</td><td>8</td><td>2</td><td>P1.6</td></tr>
<tr><td>8</td><td>9</td><td>3</td><td>P1.7</td></tr>
<tr><td>21</td><td>24</td><td>18</td><td>P2.0 (A8)</td><td rowspan="8">Port 2 (A8–A15), I/O. Port 2 is an 8-bit, bidirectional I/O port. The reset condition of port 2 is logic high. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C430/DS89C440/DS89C450 activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. As an alternate function, port 2 can function as the MSB of the external address bus when reading external program memory and read/write external RAM or peripherals. In page mode 1, port 2 provides both the MSB and LSB of the external address bus. In page mode 2, it provides the MSB and data.</td></tr>
<tr><td>22</td><td>25</td><td>19</td><td>P2.1 (A9)</td></tr>
<tr><td>23</td><td>26</td><td>20</td><td>P2.2(A10)</td></tr>
<tr><td>24</td><td>27</td><td>21</td><td>P2.3(A11)</td></tr>
<tr><td>25</td><td>28</td><td>22</td><td>P2.4(A12)</td></tr>
<tr><td>26</td><td>29</td><td>23</td><td>P2.5(A13)</td></tr>
<tr><td>27</td><td>30</td><td>24</td><td>P2.6(A14)</td></tr>
<tr><td>28</td><td>31</td><td>25</td><td>P2.7(A15)</td></tr>
<tr><td>10</td><td>11</td><td>5</td><td>P3.0</td><td rowspan="8">Port 3, I/O. Port 3 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for external interrupts, serial port 0, timer 0 and 1 inputs, and $\overline{RD}$ and $\overline{WR}$ strobes. The reset condition of port 3 is with all bits at a logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C430/DS89C440/DS89C450 activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. The alternate modes of port 3 are as follows:
PORT ALTERNATE FUNCTION
P3.0 RXD0 Serial Port 0 Receive
P3.1 TXD0 Serial Port 0 Transmit
P3.2 $\overline{INT0}$ External Interrupt 0
P3.3 $\overline{INT1}$ External Interrupt 1
P3.4 T0 Timer 0 External Input
P3.5 T1 Timer 1 External Input
P3.6 $\overline{WR}$ External Data Memory Write Strobe
P3.7 $\overline{RD}$ External Data Memory Read Strobe</td></tr>
<tr><td>11</td><td>13</td><td>7</td><td>P3.1</td></tr>
<tr><td>12</td><td>14</td><td>8</td><td>P3.2</td></tr>
<tr><td>13</td><td>15</td><td>9</td><td>P3.3</td></tr>
<tr><td>14</td><td>16</td><td>10</td><td>P3.4</td></tr>
<tr><td>15</td><td>17</td><td>11</td><td>P3.5</td></tr>
<tr><td>16</td><td>18</td><td>12</td><td>P3.6</td></tr>
<tr><td>17</td><td>19</td><td>13</td><td>P3.7</td></tr>
<tr><td>31</td><td>35</td><td>29</td><td>$\overline{EA}$</td><td>External Access. Allows selection of internal or external program memory. Connect to ground to force the DS89C430/DS89C440/DS89C450 to use an external memory program memory. The internal RAM is still accessible as determined by register settings. Connect to V_{CC} to use internal flash memory.</td></tr>
</table>

Figure 5. Functional Diagram



DETAILED DESCRIPTION

The DS89C430, DS89C440, and DS89C450 are pin compatible with all three packages of the standard 8051 and include standard resources such as three timer/counters, serial port, and four 8-bit I/O ports. The three part numbers vary only by the amount of internal flash memory (DS89C430 = 16kB, DS89C440 = 32kB, DS89C450 = 64kB), which can be in-system/in-application programmed from a serial port using ROM-resident or user-defined loader software. For volume deployments, the flash can also be loaded externally using standard commercially available parallel programmers.

Besides greater speed, the DS89C430/DS89C440/DS89C450 include 1kB of data RAM, a second full hardware serial port, seven additional interrupts, two extra levels of interrupt priority, programmable watchdog timer, brownout monitor, and power-fail reset. Dual data pointers (DPTRs) are included to speed up block data-memory moves with further enhancements coming from selectable automatic increment/decrement and toggle select operation. The speed of MOVX data memory access can be adjusted by adding stretch values up to 10 machine cycles for flexibility in selecting external memory and peripherals.

A power management mode consumes significantly lower power by slowing the CPU execution rate from one clock period per cycle to 1024 clock periods per cycle. A selectable switchback feature can automatically cancel this mode to enable normal speed responses to interrupts.

For EMI-sensitive applications, the microcontroller can disable the ALE signal when the processor is not accessing external memory.

Terminology

The term *DS89C430* is used in the remainder of the document to refer to the DS89C430, DS89C440, and DS89C450, unless otherwise specified.

Compatibility

The DS89C430 is a fully static CMOS 8051-compatible microcontroller similar in functional features to the DS87C520, but it offers much higher performance. In most cases, the DS89C430 can drop into an existing socket for the 8xC51 family, immediately improving the operation. While remaining familiar to 8051 family users, the DS89C430 has many new features. In general, software written for existing 8051-based systems works without modification on the DS89C430, with the exception of critical timing routines, as the DS89C430 performs its instructions much faster for any given crystal selection.

The DS89C430 provides three 16-bit timer/counters, two full-duplex serial ports, and 256 bytes of direct RAM plus 1kB of extra MOVX RAM. I/O ports can operate as in standard 8051 products. Timers default to 12 clocks-per-cycle operation to keep their timing compatible with a legacy 8051 family systems. However, timers are individually programmable to run at the new one clock per cycle if desired. The DS89C430 provides several new hardware features, described in subsequent sections, implemented by new special-function registers (SFRs).

Performance Overview

Featuring a completely redesigned high-speed 8051-compatible core, the DS89C430 allows operation at a higher clock frequency. This updated core does not have the wasted memory cycles that are present in a standard 8051. A conventional 8051 generates machine cycles using the clock frequency divided by 12. The same machine cycle takes one clock in the DS89C430. Thus, the fastest instructions execute 12 times faster for the same crystal frequency (and actually 24 times faster for the INC data pointer instruction). It should be noted that this speed improvement is reduced when using external memory access modes that require more than one clock per cycle.

Individual program improvement depends on the instructions used. Speed-sensitive applications would make the most use of instructions that are 12 times faster. However, the sheer number of 12-to-1 improved op codes makes dramatic speed improvements likely for any code. These architectural improvements produce instruction cycle times as low as 30ns. The dual data pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory. The new page modes allow for increased efficiency in external memory accesses.

Instruction Set Summary

All instructions have the same functionality as their 8051 counterparts, including their affect on bits, flags, and other status functions. However, the timing of each instruction is different, in both absolute and relative number of clocks.

For absolute timing of real-time events, the duration of software loops can be calculated using information given in the *Instruction Set* table in the *Ultra-High-Speed Flash Microcontroller User's Guide*. However, counter/timers default to run at the older 12 clocks per increment. In this way, timer-based events occur at the standard intervals with software executing at higher speed. Timers optionally can run at a reduced number of clocks per increment to take advantage of faster processor operation.

The relative time of some instructions may be different in the new architecture. For example, in the original architecture, the "MOVX A, @DPTR" instruction and the "MOV direct, direct" instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS89C430, the MOVX instruction takes as little as two machine cycles or two oscillator cycles, but the "MOV direct, direct" uses three machine cycles or three oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS89C430 usually uses one machine cycle for each instruction byte and requires one cycle for execution. *The user concerned with precise program timing should examine the timing of each instruction to become familiar with the changes*.

Special-Function Registers (SFRs)

All peripherals and operations that are not explicit instructions in the DS89C430 are controlled through SFRs. The most common features basic to the architecture are mapped to the SFRs. These include the CPU registers (ACC, B, and PSW), data pointers, stack pointer, I/O ports, timer/counters, and serial ports. In many cases, an SFR controls an individual function or reports the function's status. The SFRs reside in register locations 80h–FFh and are only accessible by direct addressing. SFRs with addresses ending in 0h or 8h are bit addressable.

All standard SFR locations from the 8051 are duplicated in the DS89C430, and several SFRs have been added for the unique features of the DS89C430. Most of these features are controlled by bits in SFRs located in unused locations in the 8051 SFR map, allowing for increased functionality while maintaining complete instruction set compatibility. Table 1 shows the SFRs and their locations. Table 2 specifies the default reset condition for all SFR bits.

Data Pointers

The data pointers (DPTR and DPTR1) are used to assign a memory address for the MOVX instructions. This address can point to a MOVX RAM location (on-chip or off-chip) or a memory-mapped peripheral. Two pointers are useful when moving data from one memory area to another, or when using a memory-mapped peripheral for both source and destination addresses. The user can select the active pointer through a dedicated SFR bit (SEL = DPS.0), or can activate an automatic toggling feature for altering the pointer selection (TSL = DPS.5). An additional feature, if selected, provides automatic incrementing or decrementing of the current DPTR.

Stack Pointer

The stack pointer denotes the register location at the top of the stack, which is the last used value. The user can place the stack anywhere in the scratchpad RAM by setting the stack pointer to the desired location, although the lower bytes are normally used for working registers.

I/O Ports

The DS89C430 offers four 8-bit I/O ports. Each I/O port is represented by an SFR location and can be written or read. The I/O port has a latch that contains the value written by software.

Counter/Timers

Three 16-bit timer/counters are available in the DS89C430. Each timer is contained in two SFR locations that can be read or written by software. The timers are controlled by other SFRs, described in the *SFR Bit Description* section of the *Ultra-High-Speed Flash Microcontroller User's Guide*.

Serial Ports

The DS89C430 provides two UARTs that are controlled and accessed by SFRs. Each UART has an address that is used to read and write the value contained in the UART. The same address is used for both read and write operations, and the read and write operations are distinguished by the instruction. Its own SFR control register controls each UART.

Table 1. SFR Register Map

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P0	80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
SP	81h								
DPL	82h								
DPH	83h								
DPL1	84h								
DPH1	85h								
DPS	86h	ID1	ID0	TSL	AID	—	—	—	SEL
PCON	87h	SMOD_0	SMOD0	OFDF	OFDE	GF1	GF0	STOP	IDLE
TCON	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMOD	89h	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
TL0	8Ah								
TL1	8Bh								
TH0	8Ch								

Table 1. SFR Register Map (continued)

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TH1	8Dh								
CKCON	8Eh	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0
P1	90h	P1.7/$\overline{INT5}$	P1.6/INT4	P1.5/$\overline{INT3}$	P1.4/INT2	P1.3/TXD1	P1.2/RXD1	P1.1/T2EX	P1.0/T2
EXIF	91h	IE5	IE4	IE3	IE2	CKRY	RGMD	RGSL	BGS
CKMOD	96h			T2MH	T1MH	T0MH	—	—	—
SCON0	98h	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0
SBUF0	99h								
ACON	9Dh	PAGEE	PAGES1	PAGES0	—	—	—	—	—
P2	A0h	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
IE	A8h	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0
SADDR0	A9h								
SADDR1	AAh								
P3	B0h	P3.7/$\overline{RD}$	P3.6/$\overline{WR}$	P3.5/T1	P3.4/T0	P3.3/$\overline{INT1}$	P3.2/$\overline{INT0}$	P3.1/TXD0	P3.0/RXD0
IP1	B1h	—	MPS1	MPT2	MPS0	MPT1	MPX1	MPT0	MPX0
IP0	B8h	—	LPS1	LPT2	LPS0	LPT1	LPX1	LPT0	LPX0
SADEN0	B9h								
SADEN1	BAh								
SCON1	C0h	SM0/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1
SBUF1	C1h								
ROMSIZE	C2h					PRAME	RMS2	RMS1	RMS0
PMR	C4h	CD1	CD0	SWB	CTM	4X/$\overline{2X}$	ALEON	DME1	DME0
STATUS	C5h	PIS2	PIS1	PIS0	—	SPTA1	SPRA1	SPTA0	SPRA0
TA	C7h								
T2CON	C8h	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
T2MOD	C9h							T2OE	DCEN
RCAP2L	CAh								
RCAP2H	CBh								
TL2	CCh								
TH2	CDh								
PSW	D0h	CY	AC	F0	RS1	RS0	OV	F1	P
FCNTL	D5h	$\overline{FBUSY}$	FERR			FC3	FC2	FC1	FC0
FDATA	D6h								
WDCON	D8h	SMOD_1	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
ACC	E0h								
EIE	E8h	—	—	—	EWDI	EX5	EX4	EX3	EX2
B	F0h								
EIP1	F1h	—	—	—	MPWDI	MPX5	MPX4	MPX3	MPX2
EIP0	F8h	—	—	—	LPWDI	LPX5	LPX4	LPX3	LPX2

Note: Shaded bits are timed-access protected.

Table 2. SFR Reset Value

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P0	80h	1	1	1	1	1	1	1	1
SP	81h	0	0	0	0	0	1	1	1
DPL	82h	0	0	0	0	0	0	0	0
DPH	83h	0	0	0	0	0	0	0	0
DPL1	84h	0	0	0	0	0	0	0	0
DPH1	85h	0	0	0	0	0	0	0	0
DPS	86h	0	0	0	0	0	1	0	0
PCON	87h	0	0	Special	Special	0	0	0	0
TCON	88h	0	0	0	0	0	0	0	0
TMOD	89h	0	0	0	0	0	0	0	0
TL0	8Ah	0	0	0	0	0	0	0	0
TL1	8Bh	0	0	0	0	0	0	0	0
TH0	8Ch	0	0	0	0	0	0	0	0
TH1	8Dh	0	0	0	0	0	0	0	0
CKCON	8Eh	0	0	0	0	0	0	0	1
P1	90h	1	1	1	1	1	1	1	1
EXIF	91h	0	0	0	0	Special	Special	Special	0
CKMOD	96h	1	1	0	0	0	1	1	1
SCON0	98h	0	0	0	0	0	0	0	0
SBUF0	99h	0	0	0	0	0	0	0	0
ACON	9Dh	0	0	0	1	1	1	1	1
P2	A0h	1	1	1	1	1	1	1	1
IE	A8h	0	0	0	0	0	0	0	0
SADDR0	A9h	0	0	0	0	0	0	0	0
SADDR1	AAh	0	0	0	0	0	0	0	0
P3	B0h	1	1	1	1	1	1	1	1
IP1	B1h	1	0	0	0	0	0	0	0
IP0	B8h	1	0	0	0	0	0	0	0
SADEN0	B9h	0	0	0	0	0	0	0	0
SADEN1	BAh	0	0	0	0	0	0	0	0
SCON1	C0h	0	0	0	0	0	0	0	0
SBUF1	C1h	0	0	0	0	0	0	0	0
ROMSIZE	C2h	1	1	1	1	0	1	0	1
PMR	C4h	1	0	0	0	0	0	0	0
STATUS	C5h	0	0	0	1	0	0	0	0
TA	C7h	1	1	1	1	1	1	1	1
T2CON	C8h	0	0	0	0	0	0	0	0
T2MOD	C9h	1	1	1	1	1	1	0	0
RCAP2L	CAh	0	0	0	0	0	0	0	0
RCAP2H	CBh	0	0	0	0	0	0	0	0

Table 2. SFR Reset Value (continued)

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TL2	CCh	0	0	0	0	0	0	0	0
TH2	CDh	0	0	0	0	0	0	0	0
PSW	D0h	0	0	0	0	0	0	0	0
FCNTL	D5h	1	0	1	1	0	0	0	0
FDATA	D6h	0	0	0	0	0	0	0	0
WDCON	D8h	0	Special	0	Special	0	Special	Special	0
ACC	E0h	0	0	0	0	0	0	0	0
EIE	E8h	1	1	1	0	0	0	0	0
B	F0h	0	0	0	0	0	0	0	0
EIP1	F1h	1	1	1	0	0	0	0	0
EIP0	F8h	1	1	1	0	0	0	0	0

Note: Consult the *Ultra-High-Speed Flash Microcontroller User's Guide* for more information about the bits marked "Special."

Memory Organization

There are three distinct memory areas in the DS89C430: scratchpad registers, program memory, and data memory. The registers are located on-chip but the program and data memory spaces can be on-chip, off-chip, or both. The DS89C430/DS89C440/DS89C450 have 16kB/32kB/64kB of on-chip program memory, respectively, implemented in flash memory and also have 1kB of on-chip data memory space that can be configured as program space using the PRAME bit in the ROMSIZE feature. The DS89C430 uses a memory-addressing scheme that separates program memory from data memory. The program and data segments can be overlapped since they are accessed in different manners. If the maximum address of on-chip program or data memory is exceeded, the DS89C430 performs an external memory access using the expanded memory bus. The $\overline{PSEN}$ signal goes active low to serve as a chip enable or output enable when performing a code fetch from external program memory. MOVX instructions activate the $\overline{RD}$ or $\overline{WR}$ signal for external MOVX data memory access. The program memory ROMSIZE feature allows software to dynamically configure the maximum address of on-chip program memory. This allows the DS89C430 to act as a bootloader for an external memory. It also enables the use of the overlapping external program spaces. The lower 128 bytes of on-chip flash memory—if ROMSIZE is greater than 0—are used to store reset and interrupt vectors. 256 bytes of on-chip RAM serve as a register area and program stack, which are separated from the data memory.

Register Space

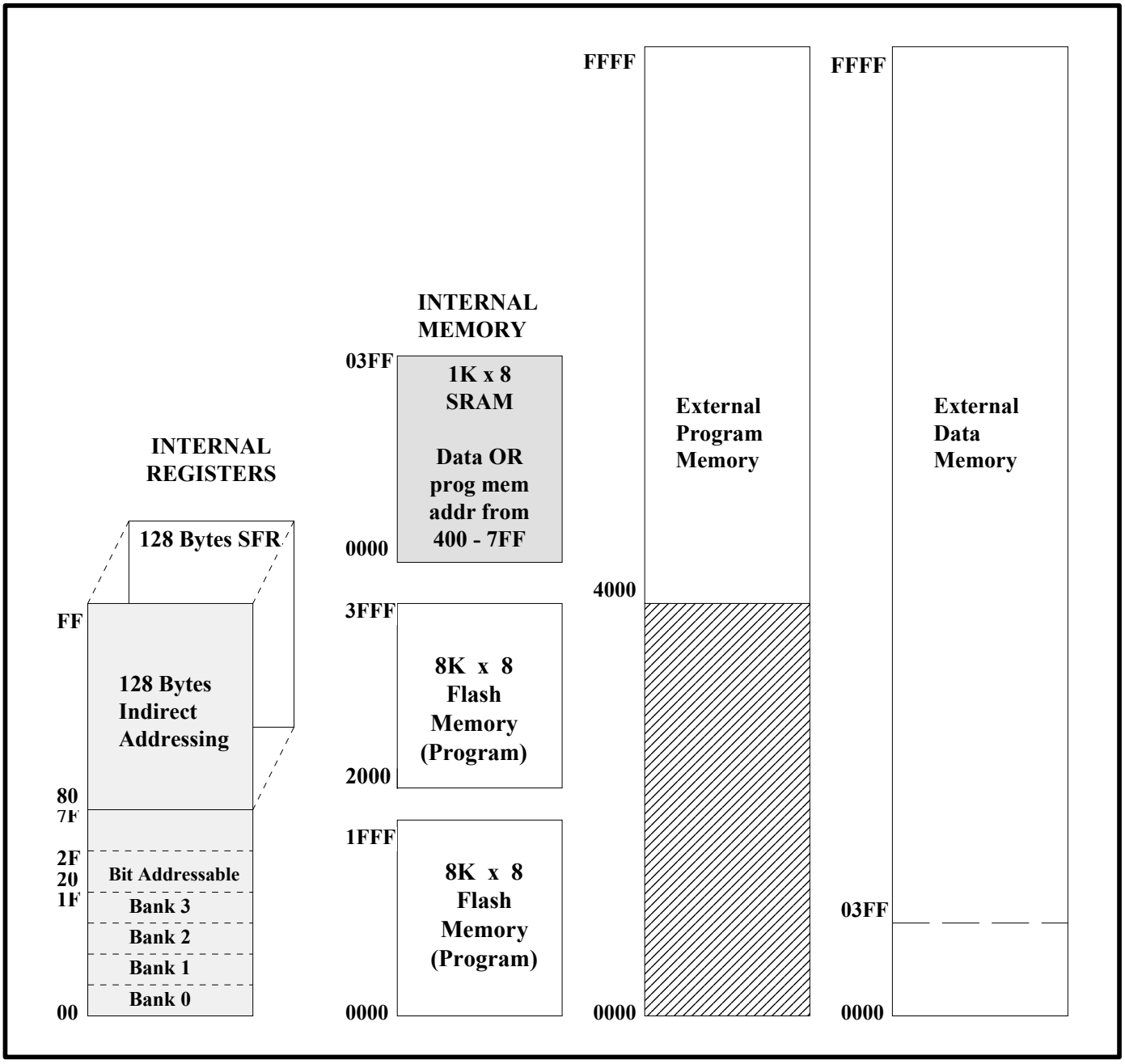
Registers are located in the 256 bytes of on-chip RAM labeled "internal registers" (Figure 6), which can be divided into two sub areas of 128 bytes each. Separate classes of instructions are used to access the registers and the program/data memory. The upper 128 bytes are overlapped with the 128 bytes of SFRs in the memory map. Indirect addressing is used to access the upper 128 bytes of scratchpad RAM, while the SFR area is accessed using direct addressing. The lower 128 bytes can be accessed using direct or indirect addressing.

There are four banks of eight working registers in the lower 128 bytes of scratchpad RAM. The working registers are general-purpose RAM locations that can be addressed within the selected bank by any instructions that use R0–R7. The register bank selection is controlled through the program status register in the SFR area. The contents of the working registers can be used for indirect addressing of the upper 128 bytes of scratchpad RAM.

Individually addressable bits in the RAM and SFR areas support Boolean operations. In the scratchpad RAM area, registers 20h–2Fh are bit addressable by software using Boolean operation instructions.

Another use of the scratchpad RAM area is for the stack. The stack pointer, contained in the SFRs, is used to select storage locations for program variables and for return addresses of control operations.

Figure 6. Memory Map (as shown for the DS89C430)



Memory Configuration

As illustrated in Figure 6, the DS89C430 incorporates two 8kB flash areas for on-chip program memory and 1kB of SRAM for on-chip data memory or a particular range (400–7FF) of “alternate” program memory space. The DS89C440 incorporates two 16kB flash memories and the DS89C450 incorporates two 32kB flash memories. The DS89C430 uses an address scheme that separates program memory from data memory such that the 16-bit address bus can address each memory area up to maximum of 64kB.

Program Memory Access

On-chip program memory begins at address 0000h and is contiguous through 3FFFh (16kB) on the DS89C430, through 7FFFh (32kB) on the DS89C440, and through FFFFh (64kB) on the DS89C450. Exceeding the maximum address of on-chip program memory causes the device to access off-chip memory. The maximum on-chip decoded address is selectable by software using the ROMSIZE feature. Software can cause the DS89C430 to behave like a device with less on-chip memory. This is beneficial when overlapping external memory is used. The maximum memory size is dynamically variable. Thus a portion of memory can be removed from the memory map to access off-chip memory and then be restored to access on-chip memory. In fact, all the on-chip memory can be removed from the memory map allowing the full 64kB memory space to be addressed from off-chip memory. Program memory addresses that are larger than the selected maximum are automatically fetched from outside the part through ports 0 and 2. Figure 6 shows a depiction of the memory map.

The ROMSIZE register is used to select the maximum on-chip decoded address for program memory. Bits RMS2, RMS1, and RMS0 have the following effect:

RMS2	RMS1	RMS0	Maximum On-Chip Program Memory Address (Size/Address)
0	0	0	0kB
0	0	1	1kB/03FFh
0	1	0	2kB/07FFh
0	1	1	4kB/0FFFh
1	0	0	8kB/1FFFh
1	0	1	16kB/3FFFh (DS89C430 default)
1	1	0	32kB/7FFFh (DS89C440 default)
1	1	1	64kB/FFFFh (DS89C450 default)

The reset default condition for all devices is to their maximum on-chip program memory size. When accessing external program memory, that amount of external memory would be inaccessible. To select a smaller effective program memory size, software must alter bits RMS2–RMS0. Altering these bits requires a timed-access procedure, as explained later.

Care should be taken so that changing the ROMSIZE register does not corrupt program execution. For example, assume that a DS89C430 is executing instructions from internal program memory near the 12kB boundary (~3000h) and that the ROMSIZE register is currently configured for a 16kB internal program space. If software reconfigures the ROMSIZE register to 4kB (0000h–0FFFh) in the current state, the device immediately jumps to external program execution because program code from 4kB to 16kB (1000h–3FFFh) is no longer located on-chip. This could result in code misalignment and execution of an invalid instruction. The recommended method is to modify the ROMSIZE register from a location in memory that is internal (or external) both before and after the operation. In the above example, the instruction that modifies the ROMSIZE register should be located below the 4kB (1000h) boundary or above the 16kB (3FFFh) boundary so that it is unaffected by the memory modification. The same precaution should be applied if the internal program memory size is modified while executing from external program memory.

For nonpage mode operations, off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. While serving as a memory bus, these pins are not I/O ports. This convention follows the standard 8051 method of expanding on-chip memory. Off-chip program memory access also occurs if the $\overline{EA}$ pin is a logic 0. $\overline{EA}$ overrides all ROMSIZE bit settings. The $\overline{PSEN}$ signal goes active (low) to serve as a chip enable or output enable when ports 0 and 2 fetch from external program memory.

The $\overline{RD}$ and $\overline{WR}$ signals are used to control the external data memory device. Data memory is accessed by MOVX instructions. The MOVX@Ri instruction uses the value in the designated working register to provide the LSB of the address, while port 2 supplies the address MSB. The MOVX@DPTR instruction uses one of the two data pointers to move data over the entire 64kB external data memory space. Software selects the data pointer used by writing to the SEL bit (DPS.0).

The DS89C430 also provides a user option for high-speed external memory access by reconfiguring the external memory interface into page mode operation.

Note: When using the original 8051 expanded bus structure, the throughput is reduced by 75% compared with that of internal operations. This is because of the CPU being stalled for three out of four clocks, waiting for the data

fetch that takes four clocks. Page mode 1 is the only external addressing mode where the CPU does not require stalls for external memory access, but page misses result in reduced external access performance.

On-Chip Program Memory

The processor can fetch the entire on-chip program memory range automatically. By default, the reset routines and all interrupt vectors are located in the lower 128 bytes of the on-chip program memory.

On-chip program memory is logically divided into pairs of 8kB, 16kB, or 32kB flash memory banks to support in-application programming. The on-chip program memory is designed to be programmed in-application with the standard 5V V_{CC} supply under the control of the user software or by using a built-in program memory loader. It can also be programmed in standard flash or EPROM programmers. The DS89C430 incorporates a memory management unit (MMU) and other hardware to support any of the three programming methods. The MMU controls program and data memory access, and provides sequencing and timing controls for programming of the on-chip program memory. A separate security flash block supports a standard three-level lock, a 64-byte encryption array, and other flash options.

Security Features

The DS89C430 incorporates a 64-byte encryption array, allowing the user to verify program codes while viewing the data in encrypted form. The encryption array is implemented in a security flash memory block that has the same electrical and timing characteristics as the on-chip program memory. Once the encryption array is programmed to non-FFh, the data presented in the verify mode is encrypted. Each byte of data is XNORed with a byte in the encryption array during verification.

A three-level lock restricts viewing of the internal program and data memory contents. By programming the three lock bits, the user can select a level of security as specified in Table 3.

Once a security level is selected and programmed, the setting of the lock bits remains. Only a mass erase can erase these bits and allow reprogramming the security level to a less restricted protection.

Table 3. Flash Memory Lock Bits

LEVEL	LB1	LB2	LB3	PROTECTION
1	1	1	1	No program lock. Encrypted verify if encryption array is programmed.
2	0	1	1	Prevent MOVC in external memory from reading program code in internal memory. $\overline{EA}$ is sampled and latched on reset. Allow no further parallel or program memory loader programming.
3	X	0	1	Level 2 plus no verify operation. Also prevent MOVX in external memory from reading internal SRAM.
4	X	X	0	Level 3 plus no external execution.

The DS89C430 provides user-selectable options that must be set before beginning software execution. The option control register uses flash bits rather than SFRs, and is individually erasable and programmable as a byte-wide register. Bit 3 of this register is defined as the watchdog POR. Setting this bit to 1 disables the watchdog reset function on power-up. Clearing this bit to 0 enables the watchdog reset function automatically. Other bits of this register are undefined and are at logic 1 when read. The value of this register can be read at address FCh in parallel programming mode or executing a verify-option-control register instruction in ROM loader mode or in-application programming mode.

The signature bytes can be read in ROM loader mode or in parallel programming mode. Reading data from addresses 30h, 31h, and 60h provides signature information on manufacturer, part, and extension as follows:

ADDRESS	VALUE	MEANING
30h	DAh	Manufacturer ID
31h	43h	DS89C430 Device ID
31h	44h	DS89C440 Device ID
31h	45h	DS89C450 Device ID
60h	01h	Device Extension

Note: The read/write accessibility of the flash memory during in-application programming is not affected by the state of the lock bits. However, the lock bits do affect the read/write accessibility in ROM loader and parallel programming modes.

In-Application Programming by User Software

The DS89C430 supports in-application programming of on-chip flash memory by user software. In-application programming is initiated by writing a flash command into the flash control (FCNTL:D5h) register to enable the flash memory for erase/program/verify operations. Address and data are input into the MMU through the flash data (FDATA:D6h) register. The flash command also enables read/write accesses to the FDATA. The MMU's sequencer provides the operation sequences and control functions to the flash memory. The MMU is designed to operate independently from the processor, except for read/write access to the SFRs.

Only the upper bank of the on-chip program memory can be in-application programmed by the user software. The lower bank of the on-chip program memory contains system hardware-dependent codes that are crucial to system operation and should not be altered during in-application programming.

All flash operations are self-timed. The user software can monitor the progress of an erase or programming operation through the flash busy (FBUSY;FCNTL.7) bit with a reset value at logic 1. A selected operation automatically starts when required data is written to the FDATA SFR. The MMU clears the FBUSY bit to indicate the start of a write/erase operation. The FBUSY bit may not change state for up to 1μs after the operation is requested. During this time, the application should poll the status of the FBUSY bit waiting for it to change state. This bit is held low until either the end of the operation or until an error indicator is returned. A flash operating failure terminates the current operation and sets the flash error flag (FERR;FCNTL.6) to logic 1. Both the busy and error flags are read-only bits.

Read/write access during in-application programming is not affected by the state of the lock bits.

A sample programming sequence for a "write upper program memory bank" is shown below. The command must be reentered each time an operation is requested, i.e., it is not permissible to issue the "write upper program memory bank" command once and then repeatedly load address and data values to program a block of memory.

1. Make sure the $\overline{\text{FBUSY}}$ bit is 1 to indicate flash MMU is idle.
2. Write 0Bh to the FCNTL register using the timed access sequence.
3. Write address_MSB to the FDATA register.
4. Write address_LSB to the FDATA register.
5. Write data_value to the FDATA register.
6. Make sure the $\overline{\text{FBUSY}}$ bit is 0 to indicate programming has started.
7. Wait for $\overline{\text{FBUSY}}$ bit to return to 1 to indicate end of programming operation.
8. Make sure FERR is 0 to indicate no programming error.

The flash command (FC3–FC0;FCNTL.3:0) bits provide flash commands as listed in Table 4.

Table 4. In-Application Programming Commands

FC3:FC0	COMMAND	OPERATION
0000	Read Mode	Default state. All flash blocks are in read mode. **Note:** The upper bank of flash memory is inaccessible for execution unless the FC3:0 bits are in the read mode (0000b) state.
0001	Verify Option Control Register	Read data from the option control register. Data is available in the FDATA at the end of the following machine cycle. FDATA.3 is the logic value of the watchdog POR default setting.
0010	Verify Security Block	Read a byte of data from the security block. After the address byte is written to the FDATA, data is available in the FDATA at the end of the following machine cycle. (Lock bits are addressed at 40h and FDATA.5:3 are the logic value of LB1, LB2 and LB3, respectively.)
0011	Verify Upper Program Memory Bank	Read a byte of data from upper flash memory bank (address range from 2000h to 3FFFh). The first and second byte writes to the FDATA are the upper and lower byte of the address. Data is available in the FDATA at the end of the following machine cycle after the second address byte is written.
0100	Reserved for Future Use	This command should not be modified by user programs.
1000	Reserved for Future Use	This command should not be modified by user programs.
1001	Write Option Control Register	Write to the option control register as data is written to FDATA. Bit 3 of the data byte represents the watchdog POR default setting.
1010	Write Security Block	Write a byte of data to the security block at a selected locations addressed by the first byte write to the FDATA. The second write to the FDATA is the data byte. (Lock bits are addressed at 40h and the FDATA 5:3 represents lock bits LB3, LB2, and LB1, respectively.)
1011	Write Upper Program Memory Bank	Write a byte of code to the upper flash memory bank (address range from 2000h to 3FFFh). The first and second byte writes to the FDATA are the upper byte and the lower byte of the address. The third write to the FDATA is the data byte.
1100	Erase Option Control Register	Erase the option control register. The contents of this register are returned to FFh. This operation disables the watchdog reset function on power-up.
1101	Erase Security Block	Erase the security flash block that contains the 64-byte encryption array and the lock bits. The content of every memory location is turned into FFh.
1110	Erase Upper Program Memory Bank	Erase the upper bank of flash memory bank. The contents of every memory location are returned to FFh.
1111	System Reset	This command is used to cause a system reset.

The flash command bits are cleared to 0 on all forms of reset, and it is important for the user software to clear these bits to 0 to return the flash memory to read mode from erase/program operation. This setting is a “no operation” condition for the MMU, which allows the processor to return to its normal execution. Note that the busy and error flags have no function in normal flash-read mode.

The FCNTL SFR can only be written using timed access. This procedure provides protection against inadvertent erase/program operation on the flash memory. Any command written to the FCNTL during a flash operation is ignored (FBUSY = 0). To ensure data integrity, an erase command sequence should be reinitiated if an erase or program operation is interrupted by a reset.

ROM Loader

The full on-chip flash program memory space, security flash block, and external SRAM can be programmed in-system from an external source through serial port 0 under the control of a built-in ROM loader. The ROM loader also has an auto-baud feature that determines which baud-rate frequencies are being used for communication and sets the baud-rate generator for that speed.

When the DS89C430 is powered up and has entered its user operating mode, the ROM loader mode can be invoked at any time by forcing RST = 1, $\overline{EA}$ = 0, and $\overline{PSEN}$ = 0. It remains in effect until power-down or when the condition (RST = 1 and $\overline{PSEN}$ = $\overline{EA}$ = 0) is removed. Entering the ROM loader mode forces the processor to start fetching from the 2kB internal ROM for program memory initialization and other loader functions.

The read/write accessibility is determined by the state of the lock bits, which can be verified directly by the ROM loader.

The flash memory can be programmed (by the built-in ROM loader) using commands that are received over the serial interface from a host PC. Full details of the ROM loader commands are given in the *Ultra-High-Speed Flash Microcontroller User's Guide*. Host software to communicate with the ROM loader is available in Windows® format as well as other platforms. Contact our technical support department at micro.support@dalsemi.com for more information.

Parallel Programming Mode

The microcontroller also supports a programming mode such as that used by commercial device programmers. This mode is of little utility in normal applications and is only used by commercial device programmers. For information on this mode, contact our technical support department at micro.support@dalsemi.com.

Data Pointer Increment/Decrement and Options

The DS89C430 incorporates a hardware feature to assist applications that require data pointer increment/decrement. Data pointer increment/decrement bits ID0 and ID1 (DPS.6 and DPS.7) define how the INC DPTR instruction functions in relation to the active DPTR (selected by the SEL bit). Setting ID0 = 1 and SEL = 0 enables the decrement operation for DPTR, and execution of the INC DPTR instruction decrements the DPTR contents by 1. Similarly, setting ID1 = 1 and SEL = 1 enables the decrement operation for DPTR1, and execution of the INC DPTR instruction decrements the DPTR1 contents by 1. With this feature, the user can configure the data pointers to operate in four ways for the INC DPTR instruction:

ID1	ID0	SEL = 0	SEL = 1
0	0	INC DPTR	INC DPTR1
0	1	DEC DPTR	INC DPTR1
1	0	INC DPTR	DEC DPTR1
1	1	DEC DPTR	DEC DPTR1

SEL (DPS.0) bit always selects the active data pointer. The DS89C430 offers a programmable option that allows any instructions related to data pointer to toggle the SEL bit automatically. This option is enabled by setting the toggle-select-enable bit (TSL–DPS.5) to a logic 1. Once enabled, the SEL bit is automatically toggled *after* the execution of one of the following five DPTR-related instructions:

```
INC DPTR
MOV DPTR #data16
MOVC A, @A+DPTR
MOVX A, @DPTR
MOVX @DPTR, A
```

The DS89C430 also offers a programmable option that automatically increases (or decreases) the contents of the selected data pointer by 1 *after* the execution of a DPTR-related instruction. The actual function (increment or decrement) is dependent on the setting of the ID1 and ID0 bits. This option is enabled by setting the automatic increment/decrement enable (AID–DPS.4) to a logic 1 and is affected by the following three instructions:

```
MOVC A, @A+DPTR
MOVX A, @DPTR
MOVX @DPTR, A
```

Windows is a registered trademark of Microsoft Corporation.

External Memory

The DS89C430 executes external memory cycles for code fetches and read/writes of external program and data memory. A nonpage external memory cycle is four times slower than the internal memory cycles (i.e., an external memory cycle contains four system clocks). However, a page mode external memory cycle can be completed in one, two, or four system clocks for a page hit and two, four, or eight system clocks for a page miss, depending on user selection. The DS89C430 also supports a second page mode operation with a different external bus structure that provides for fast external code fetches but uses four system clock cycles for data memory access.

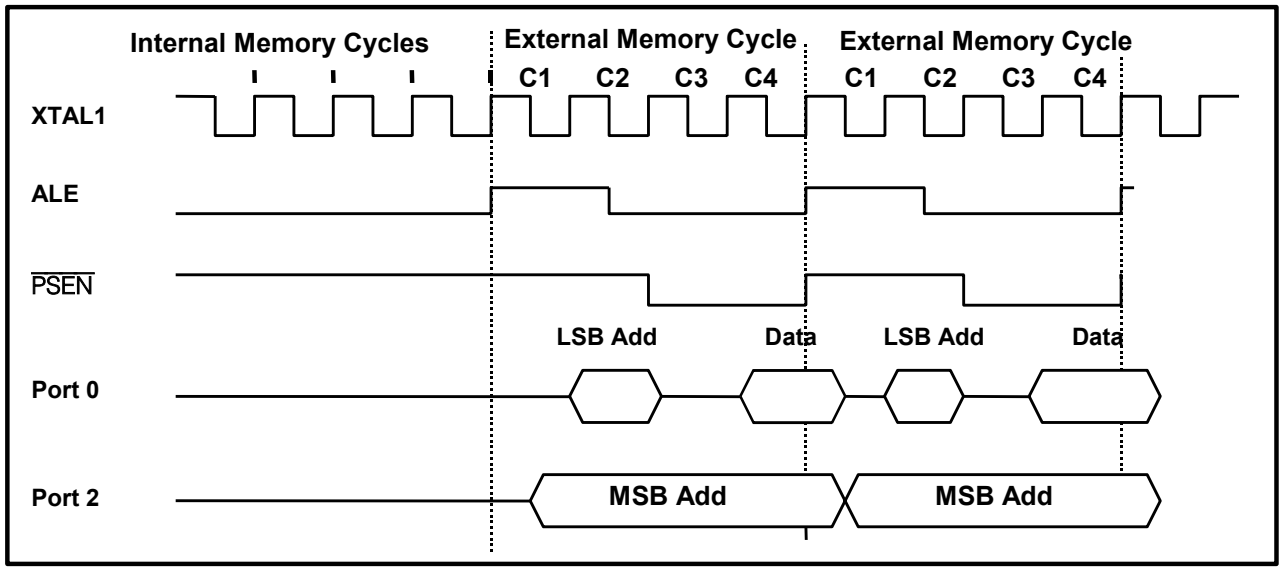
External Program Memory Interface (Nonpage Mode)

Figure 7 shows the timing relationship for internal and external code fetches when CD1 and CD0 are set to 10b, assuming the microcontroller is in nonpage mode for external fetches. Note that an external program fetch takes four system clocks, and an internal program fetch requires only one system clock.

As illustrated in Figure 7, ALE is deasserted when executing an internal memory fetch. The DS89C430 provides a programmable user option to turn on ALE during internal program memory operation. ALE is automatically enabled for code fetch externally, independent of the setting of this option.

$\overline{\text{PSEN}}$ is only asserted for external code fetches, and is inactive during internal execution.

Figure 7. External Program Memory Access (Nonpage Mode, CD1:CD0 = 10)



External Data Memory Interface in Nonpage Mode Operation

Just like the program memory cycle, the external data memory cycle is four times slower than the internal data memory cycle in nonpage mode. A basic internal memory cycle contains one system clock and a basic external memory cycle contains four system clocks for nonpage mode operation.

The DS89C430 allows software to adjust the speed of external data memory access by stretching the memory bus cycle. CKCON (8Eh) provides an application-selectable stretch value for this purpose. Software can change the stretch value dynamically by changing the setting of CKCON.2–CKCON.0. Table 5 shows the data memory cycle stretch values and their effect on the external MOVX memory bus cycle and the control signal pulse width in terms of the number of oscillator clocks. A stretch machine cycle always contains four system clocks.

Table 5. Data Memory Cycle Stretch Values

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.5	1	2	2048
001	1	1	2	4	4096
010	2	2	4	8	8192
011	3	3	6	12	12,288
100	7	4	8	16	16,384
101	8	5	10	20	20,480
110	9	6	12	24	24,576
111	10	7	14	28	28,672

As Table 5 shows, the stretch feature supports eight stretched external data memory access cycles, which can be categorized into three timing groups. When the stretch value is cleared to 000b, there is no stretch on external data memory access and a MOVX instruction is completed in two basic memory cycles. When the stretch value is set to 1, 2, or 3, the external data memory access is extended by 1, 2, or 3 stretch machine cycles, respectively. Note that the first stretch value does not result in adding four system clocks to the $\overline{RD}/\overline{WR}$ control signals. This is because the first stretch uses one system clock to create additional setup time and one system clock to create additional address hold time. When using very slow RAM and peripherals, a larger stretch value (4–7) can be selected. In this stretch category, one stretch machine cycle (4 system clocks) is used to stretch the ALE pulse width, one stretch machine cycle is used to create additional setup, one stretch machine cycle is used to create additional hold time, and one stretch machine cycle is added to the $\overline{RD}$ or $\overline{WR}$ strobes.

The following diagrams illustrate the timing relationship for external data memory access in full speed (stretch value = 0), in the default stretch setting (stretch value = 1), and slow data memory accessing (stretch value = 4), when the system clock is in divide-by-1 mode (CD1:CD0 = 10b).

Figure 8. Nonpage Mode, External Data Memory Access (Stretch = 0, CD1:CD2 = 10)

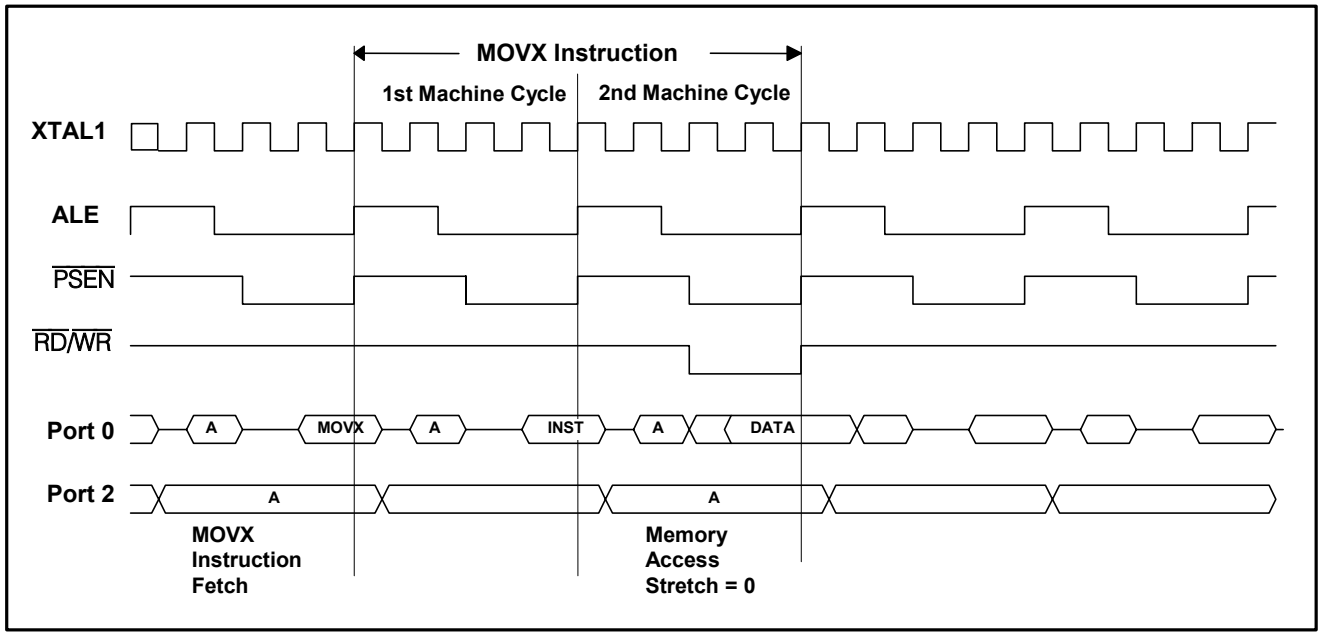
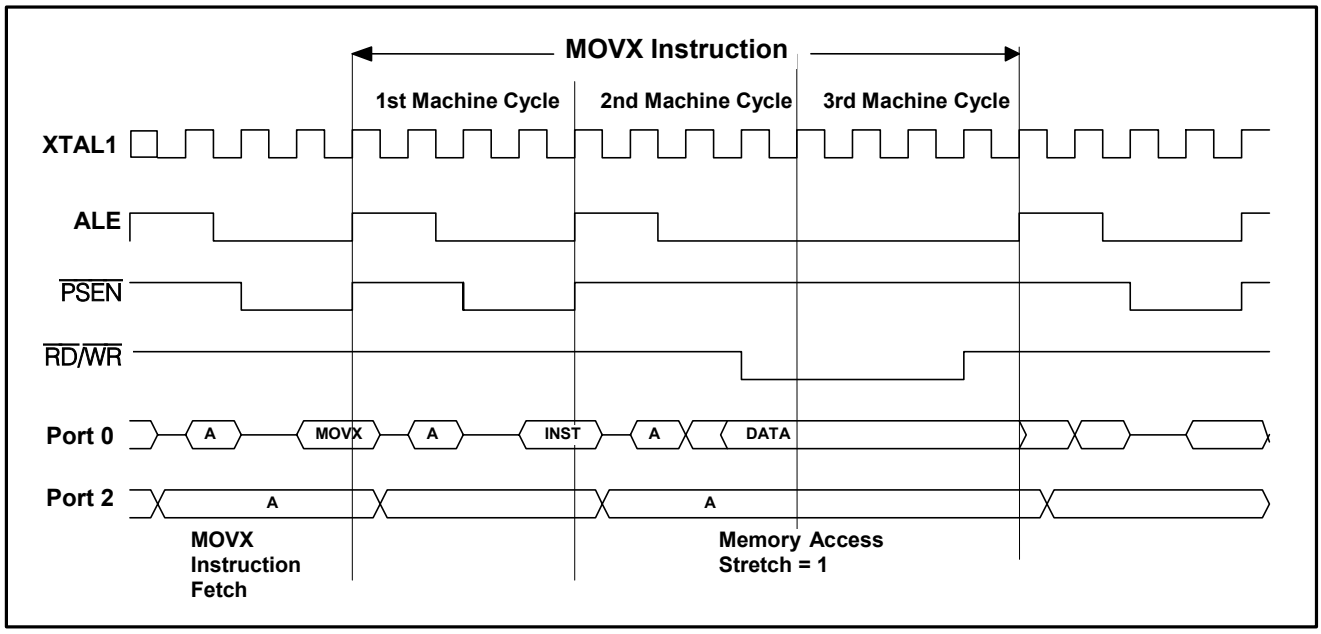


Figure 9. Nonpage Mode, External Data Memory Access (Stretch = 1, CD1:CD2 = 10)



Page Mode, External Memory Cycle

Page mode retains the basic circuitry requirement for an original 8051 external memory interface, but alters the configuration of P0 and P2 for the purposes of address output and data I/O during external memory cycles. Additionally, the functions of ALE and $\overline{PSEN}$ are altered to support this mode of operation.

Setting the PAGEE (ACON.7) bit to logic 1 enables page mode. Clearing the PAGEE bit to logic 0 disables the page mode and the external bus structure defaults to the original 8051 expanded bus configuration (nonpage mode). The DS89C430 supports page mode in two external bus structures. The logic value of the page-mode-select bits in the ACON register determines the external bus structure and the basic memory cycle in number of system clocks. Table 6 summarizes this option. The first three selections use the same bus structure but with different memory cycle time. Setting the select bits to 11b selects another bus structure. Write access to the ACON register requires a timed access.

Table 6. Page Mode Select

PAGES1:PAGES0	CLOCKS PER MEMORY CYCLE		EXTERNAL BUS STRUCTURE
	PAGE-HIT	PAGE-MISS	
00	1	2	P0: Primary data bus. P2: Primary address bus, multiplexing both the upper byte and lower byte of address.
01	2	4	P0: Primary data bus. P2: Primary address bus, multiplexing both the upper byte and lower byte of address.
10	4	8	P0: Primary data bus. P2: Primary address bus, multiplexing both the upper byte and lower byte of address.
11	2	4	P0: Lower address byte. P2: The upper address byte is multiplexed with the data byte. Note: This setting affects external code fetches only; accessing the external data memory requires four clock cycles, regardless of page hit or miss.

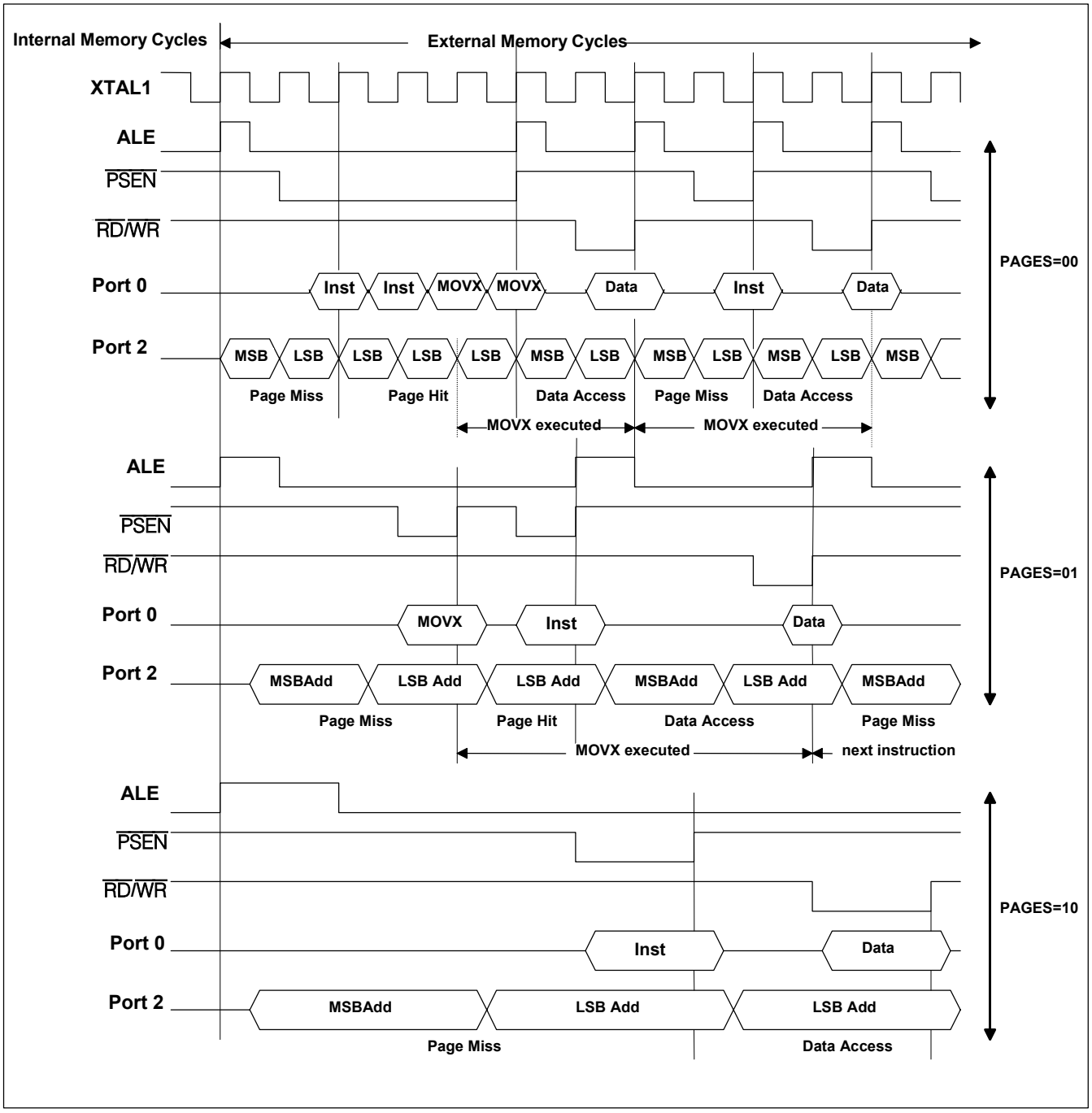
The first page mode's (page mode 1) external bus structure uses P2 as the primary address bus, (multiplexing both the most significant byte and least significant byte of the address for each external memory cycle) and P0 is used as the primary data bus. During external code fetches, P0 is held in a high-impedance state by the processor. Op codes are driven by the external memory onto P0 and latched at the end of the external fetch cycle at the rising edge of $\overline{PSEN}$. During external data read/write operations, P0 functions as the data I/O bus. It is held in a high-impedance state for external reads from data memory and driven with data during external writes to data memory.

- A page miss occurs when the most significant byte of the subsequent address is different from the last address. The external memory machine cycle can be 2, 4, or 8 system clocks in length for a page miss.

- A page hit occurs when the most significant byte of the subsequent address does not change from the last address. The external memory machine cycle can be 1, 2, or 4 system clocks in length for a page hit.

During a page hit, P2 drives Addr [0–7] of the 16-bit address, while the most significant address byte is held in the external address latches. $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}$ strobes accordingly for the appropriate operation on the P0 data bus. There is no ALE assertion for page hits.

Figure 10. Page Mode 1, External Memory Cycle (CD1:CD0 = 10)



During a page miss, P2 drives the Addr [8:15] of the 16-bit address and holds it for the duration of the first half of the memory cycle to allow the external address latches to latch the new most significant address byte. ALE is asserted to strobe the external address latches. During this operation, $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}$ are held in inactive states and P0 is in a high-impedance state. The following half-memory cycle is executed as a page hit cycle and the appropriate operation takes place.

A page miss can occur at set intervals or during external operations that require a memory access into a page of memory that has not been accessed during the last external cycle. Generally, the first external memory access causes a page miss. The new page address is stored internally and is used to detect a page miss for the current external memory cycle.

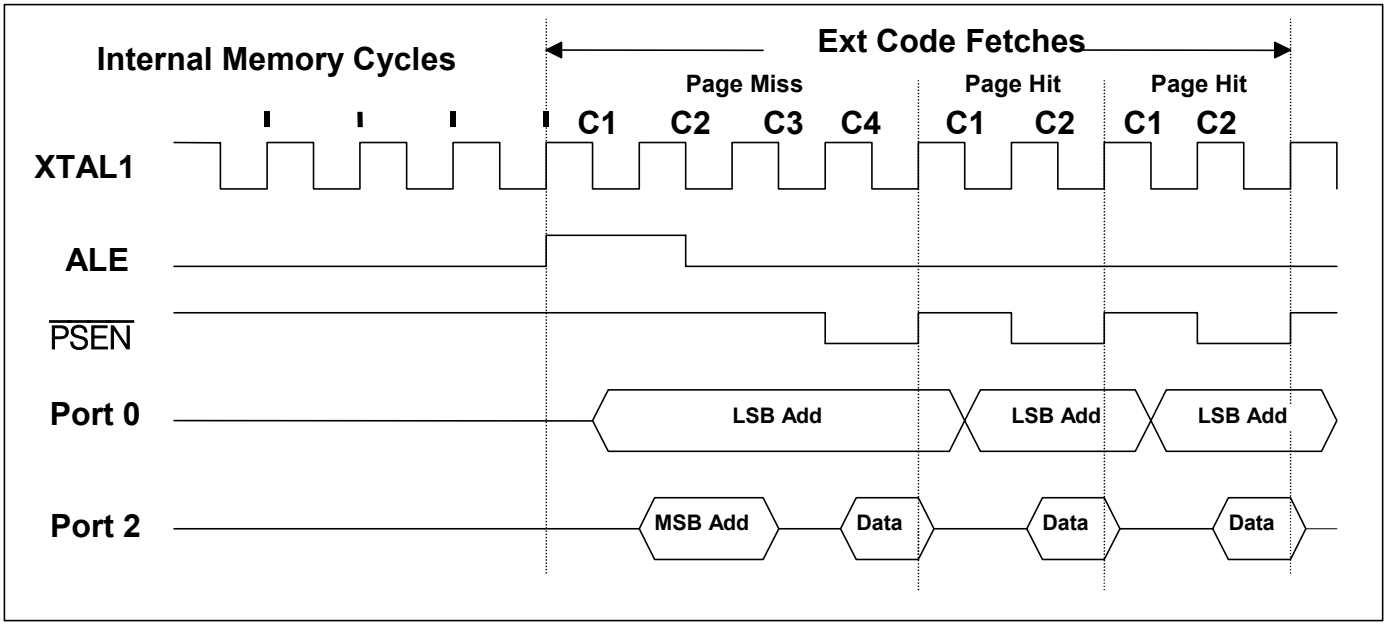
Note that there are a few exceptions for this mode of operation when PAGES1 and PAGES2 are set to 00b:

- $\overline{\text{PSEN}}$ is asserted for both a page hit and a page miss for a full clock cycle.
- The execution of external MOVX instruction causes a page miss.
- A page miss occurs when fetching the next external instruction following the execution of an external MOVX instruction.

Figure 10 shows the external memory cycle for this bus structure. The first case illustrates a back-to-back execution sequence for the one-cycle page mode (PAGES1 = PAGES0 = 0b). $\overline{\text{PSEN}}$ remains active during page hit cycles, and page misses are forced during and after MOVX executions, independent of the most significant byte of the subsequent addresses. The second case illustrates a MOVX execution sequence for two-cycle page mode (PAGES1 = 0 and PAGES0 = 1). $\overline{\text{PSEN}}$ is active for a full clock cycle in code fetches. Note that changing the most significant byte of the data address causes the page misses in this sequence. The third case illustrates a MOVX execution sequence for four-cycle page mode (PAGES1 = 1 and PAGES0 = 0). There is no page miss in this execution cycle as the most significant byte of the data address is assumed to match the last program address.

The second page mode (page mode 2) external bus structure multiplexes the most significant address byte with data on P2 and uses P0 for the least significant address byte. This bus structure is used to speed up external code fetches only. External data memory access cycles are identical to the nonpage mode except for the different signals on P0 and P2. Figure 11 illustrates the memory cycle for external code fetches.

Figure 11. Page Mode 2, External Code Fetch Cycle (CD1:CD0 = 10)



Stretch External Data Memory Cycle in Page Mode

The DS89C430 allows software to adjust the speed of external data memory access by stretching the memory bus cycle in page mode operation just like nonpage mode operation. The following tables summarize the stretch values and their effect on the external MOVX memory bus cycle and the control signals' pulse width in terms of the number of oscillator clocks. A stretch machine cycle always contains four system clocks, independent of the logic value of the page mode select bits.

Table 7. Page Mode 1, Data Memory Cycle Stretch Values (PAGES1:PAGES0 = 00)

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.25	0.5	1	1024
001	1	0.75	1.5	3	3072
010	2	1.75	3.5	7	7168
011	3	2.75	5.5	11	11,264
100	7	3.75	7.5	15	15,360
101	8	4.75	9.5	19	19,456
110	9	5.75	11.5	23	23,552
111	10	6.75	13.5	27	27,648

Table 8. Page Mode 1, Data Memory Cycle Stretch Values (PAGES1:PAGES0 = 01)

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.25	0.5	1	1024
001	1	0.75	1.5	3	3072
010	2	1.75	3.5	7	7168
011	3	2.75	5.5	11	11,264
100	7	3.75	7.5	15	15,360
101	8	4.75	9.5	19	19,456
110	9	5.75	11.5	23	23,552
111	10	6.75	13.5	27	27,648

Table 9. Page Mode 1, Data Memory Cycle Stretch Values (PAGES1:PAGES0 = 10)

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.5	1	2	2048
001	1	1	2	4	4096
010	2	2	4	8	8192
011	3	3	6	12	12,288
100	7	4	8	16	16,384
101	8	5	10	20	20,480
110	9	6	12	24	24,576
111	10	7	14	28	28,672

Table 10. Page Mode 2, Data Memory Cycle Stretch Values (PAGES1:PAGES0 = 11)

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.5	1	2	2048
001	1	1	2	4	4096
010	2	2	4	8	8192
011	3	3	6	12	12,288
100	7	4	8	16	16,384
101	8	5	10	20	20,480
110	9	6	12	24	24,576
111	10	7	14	28	28,672

As shown in the previous tables, the stretch feature supports eight stretched external data-memory access options, which can be categorized into three timing groups. When the stretch value is cleared to 000b, there is no stretch on external data memory access, and a MOVX instruction is completed in two basic memory cycles. When the stretch value is set to 1, 2, or 3, the external data memory access is extended by 1, 2, or 3 stretch memory cycles, respectively. Note that the first stretch value does not result in adding four system clocks to the control signals. This is because the first stretch uses one system clock to create additional address setup and data bus float time and one system clock to create additional address and data hold time. When using very slow RAM and peripherals, a larger stretch value (4–7) can be selected. In this stretch category, two stretch cycles are used to create additional setup (the ALE pulse width is also stretched by one stretch cycle for page miss) and one stretch cycle is used to create additional hold time. The following timing diagrams illustrate the external data memory access at divide-by-1 system clock mode (CD1:CD0 = 10b).

Figure 12 illustrates the external data-memory stretch-cycle timing relationship when PAGEE = 1 and PAGES1:PAGES0 = 01. The stretch cycle shown is for a stretch value of 1 and is coincident with a page miss. Note that the first stretch value does not result in adding four system clocks to the $\overline{RD}/\overline{WR}$ control signals. This is because the first stretch uses one system clock to create additional setup and one system clock to create additional hold time.

Figure 13 shows the timing relationship for a slow peripheral interface (stretch value = 4). Note that a page hit data memory cycle is shorter than a page miss data memory cycle. The ALE pulse width is also stretched by a stretch cycle in the case of a page miss.

The stretched data memory bus cycle timing relationship for PAGES = 11 is identical to nonpage mode operation since the basic data memory cycle always contains four system clocks in this page mode operation.

Figure 12. Page Mode 1, External Data Memory Access (PAGES = 01, STRETCH = 1, CD = 10)

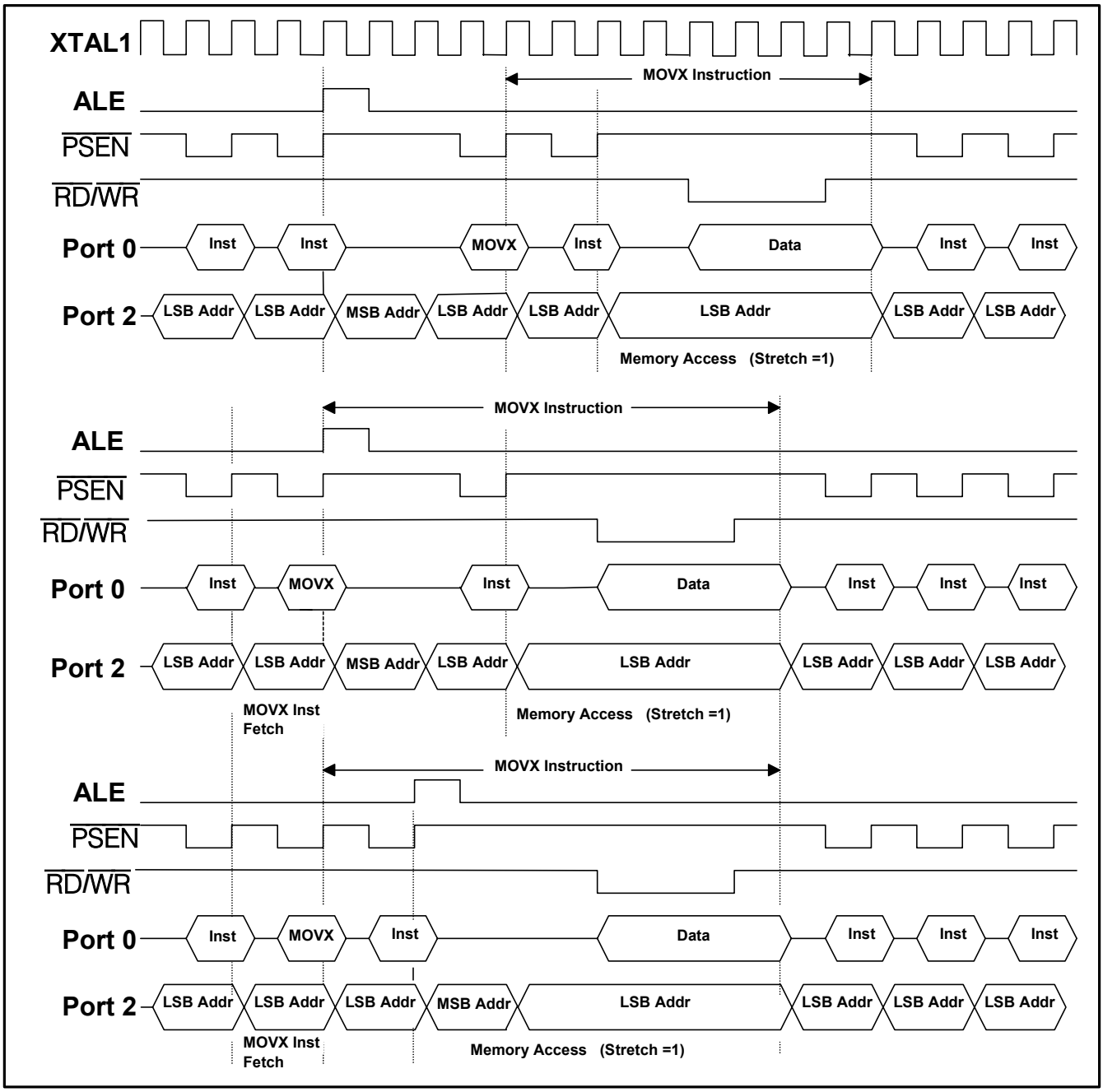
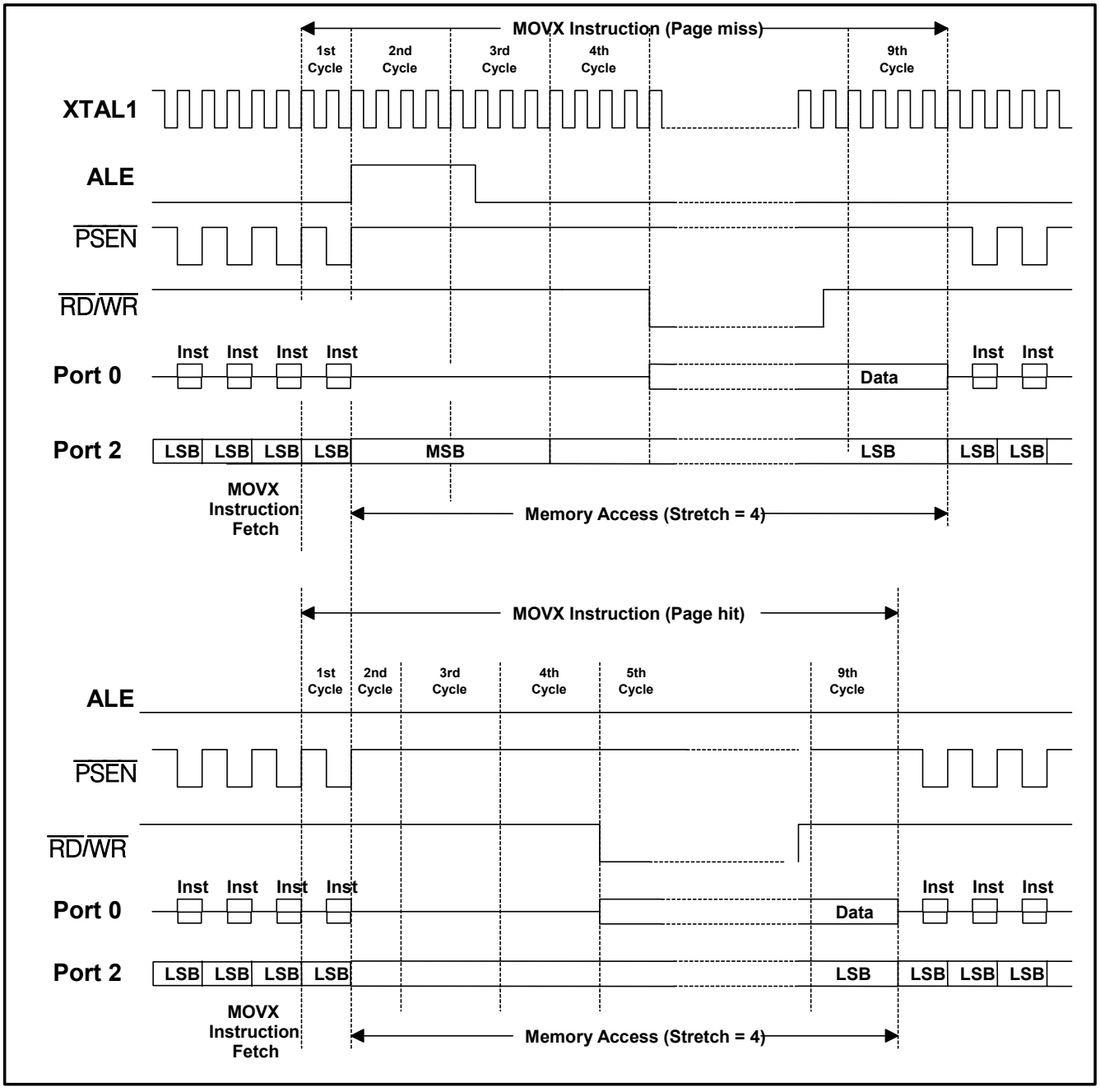


Figure 13. Page Mode 1, External Data Memory Access (PAGES = 01, Stretch = 4, CD = 10)



Interrupts

The DS89C430 provides 13 interrupt sources. All interrupts, with the exception of the power fail, are controlled by a series combination of individual enable bits and a global enable (EA) in the interrupt-enable register (IE.7). Setting EA to a logic 1 allows individual interrupts to be enabled. Setting EA to a logic 0 disables all interrupts regardless of the individual interrupt-enable settings. The power-fail interrupt is controlled by its individual enable only.

The interrupt enables and priorities are functionally identical to those of the 80C52, except that the DS89C430 supports five levels of interrupt priorities instead of the original two.

Interrupt Priority

There are five levels of interrupt priority: Level 4 to 0. The highest interrupt priority is level 4, which is reserved for the power-fail interrupt. All other interrupts have individual priority bits in the interrupt priority registers to allow each interrupt to be assigned a priority level from 3 to 0. The power-fail interrupt always has the highest priority if it is enabled. All interrupts also have a natural hierarchy. In this manner, when a set of interrupts has been assigned the same priority, a second hierarchy determines which interrupt is allowed to take precedence. The natural hierarchy is determined by analyzing potential interrupts in a sequential manner with the order listed in Table 11.

The processor indicates that an interrupt condition occurred by setting the respective flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Unless marked in Table 11, all these flags must be cleared by software.

Table 11. Interrupt Summary

INTERRUPT	VECTOR	NATURAL ORDER	FLAG	ENABLE	PRIORITY CONTROL
Power Fail	33h	0 (Highest)	PFI (WDCON.4)	EPFI(WDCON.5)	N/A
External Interrupt 0	03h	1	IE0 (TCON.1) (Note 1)	EX0 (IE.0)	LPX0 (IP0.0); MPX0 (IP1.0)
Timer 0 Overflow	0Bh	2	TF0 (TCON.5) (Note 2)	ET0 (IE.1)	LPT0 (IP0.1); MPT0 (IP1.1)
External Interrupt 1	13h	3	IE1 (TCON.3) (Note 1)	EX1 (IE.2)	LPX1 (IP0.2); MPX1 (IP1.2)
Timer 1 Overflow	1Bh	4	TF1 (TCON.7) (Note 2)	ET1 (IE.3)	LPT1 (IP0.3); MPT1 (IP1.3)
Serial Port 0	23h	5	RI_0 (SCON0.0); TI_0 (SCON0.1)	ES0 (IE.4)	LPS0 (IP0.4); MPS0 (IP1.4)
Timer 2 Overflow	2Bh	6	TF2 (T2CON.7); EXF2 (T2CON.6)	ET2 (IE.5)	LPT2 (IP0.5); MPT2 (IP1.5)
Serial Port 1	3Bh	7	RI_1 (SCON1.0); TI_1 (SCON1.1)	ES1 (IE.6)	LPS1 (IP0.6); MPS1 (IP1.6)
External Interrupt 2	43h	8	IE2 (EXIF.4)	EX2 (EIE.0)	LPX2 (EIP0.0); MPX2 (EIP1.0)
External Interrupt 3	4Bh	9	IE3 (EXIF.5)	EX3 (EIE.1)	LPX3 (EIP0.1); MPX3 (EIP1.1)
External Interrupt 4	53h	10	IE4 (EXIF.6)	EX4 (EIE.2)	LPX4 (EIP0.2); MPX4 (EIP1.2)
External Interrupt 5	5Bh	11	IE5 (EXIF.7)	EX5 (EIE.3)	LPX5 (EIP0.3); MPX5 (EIP1.3)
Watchdog	63h	12 (Lowest)	WDIF (WDCON.3)	EWDI (EIE.4)	LPWDI (EIP0.4); MPWDI (EIP1.4)

Note 1: If the interrupt is edge triggered, the flag is cleared automatically by hardware when the service routine is vectored to. If the interrupt is level triggered, the flag follows the state of the pin.
Note 2: The flag is cleared automatically by hardware when the service routine is vectored to.

Timer/Counters

The DS89C430 incorporates three 16-bit timers. All three timers can be used as either counters of external events, where 1-to-0 transitions on a port pin are monitored and counted, or timers that count oscillator cycles. Table 12 summarizes the timer functions.

Timers 0 and 1 both have three modes of operations. They can each be used as a 13-bit timer/counter, a 16-bit timer/counter, or an 8-bit timer/counter with autoreload. Timer 0 has a fourth operating mode as two 8-bit timer/counters without autoreload. Each timer can also be used as a counter of external pulses on the corresponding T0/T1 pin for 1-to-0 transitions. The timer mode (TMOD) register controls the mode of operation. Each timer consists of a 16-bit register in 2 bytes, which can be found in the SFR map as TL0, TH0, TL1, and TH1. The timer control (TCON) register enables timers 0 and 1.

Table 12. Timer Functions

FUNCTIONS	TIMER 0	TIMER 1	TIMER 2
Timer/Counter	13/16/8*/2x8 bit	13/16/8* bit	16 bit
Timer with Capture	No	No	Yes
External Control Pulse Counter	Yes	Yes	No
Up/Down Autoreload Timer/Counter	No	No	Yes
Baud Rate Generator	No	Yes	Yes
Timer Output Clock Generator	No	No	Yes

**8-bit timer/counter includes autoreload feature. 2x8-bit mode does not.*

Each timer has a selectable time base (Table 14). Following a reset, the timers default to divide by 12 to maintain drop-in compatibility with the 8051. If timer 2 is used as a baud rate generator or clock output, its time base is fixed at divide by 2, regardless of the setting of its timer mode bits.

Timer 2 is a true 16-bit timer/counter that, with a 16-bit capture (RCAP2L and RCAP2H) register, is able to provide some unique functions like up/down autoreload timer/counter and timer output-clock generation. Timer 2 (registers TL2 and TH2) is enabled by the T2CON register. Its mode of operation is selected by the T2MOD register.

For operation details, refer to *Section 11: Programmable Timers* in the *Ultra-High-Speed Flash Microcontroller User's Guide.*

Timed Access

The timed-access function prevents an errant CPU from making accidental changes to certain SFR bits that are considered vital to proper system operation. This is achieved by using software control when accessing the following SFR control bits:

SFR	BIT	FUNCTION
WDCON.0	RWT	Reset Watchdog Timer
WDCON.1	EWT	Watchdog Reset Enable
WDCON.3	WDIF	Watchdog Interrupt Flag
WDCON.6	POR	Power-On Reset Flag
EXIF.0	BGS	Bandgap Select
ACON.5	PAGES0	Page Mode Select Bit 0
ACON.6	PAGES1	Page Mode Select Bit 1
ACON.7	PAGEE	Page Mode Enable
ROMSIZE.0	RMS0	Program Memory Size Select Bit 0
ROMSIZE.1	RMS1	Program Memory Size Select Bit 1
ROMSIZE.2	RMS2	Program Memory Size Select Bit 2
ROMSIZE.3	PRAME	Program RAM Enable
FCNTL.0	FC0	Flash Command Bit 0
FCNTL.1	FC1	Flash Command Bit 1
FCNTL.2	FC2	Flash Command Bit 2
FCNTL.3	FC3	Flash Command Bit 3

Before these bits can be altered, the processor must execute the timed-access sequence. This sequence consists of writing an AAh to the timed access (TA, C7h) register, followed by writing a 55h to the same register within three machine cycles. This timed sequence of steps allows any of the timed access-protected SFR bits to be altered

during the three machine cycles following the writing of the 55h. Writing to a timed-access-protected bit outside of these three machine cycles has no effect on the bit.

The timed-access process is address, data, and time dependent. A processor running out of control and not executing system software statistically is not able to perform this timed sequence of steps, and as such, does not accidentally alter the protected bits. It should be noted that this method should be used in the main body of the system software and *never* used in an interrupt routine in conjunction with the watchdog reset. Interrupt routines using the timed-access watchdog-reset bit (RWT) can recover a lost system and allow the resetting of the watchdog, but the system returns to a lost condition once the RETI is executed, unless the stack is modified. Also, it is advisable that interrupts be disabled (EA = 0) when executing the timed-access sequence, since an interrupt during the sequence adds time, making the timed-access attempt fail.

Power Management and Clock-Divide Control

Power-management features are available that monitor the power-supply voltage levels and support low-power operation with three power-saving modes. Such features include a bandgap voltage monitor, watchdog timer, selectable internal ring oscillator, and programmable system clock speed. The SFRs that provide control and application software access are the watchdog control (WDCON, D8h), extended interrupt enable (EIE, E8h), extended interrupt flag (EXIF, 91h) and power control (PCON, 87h) registers.

System Clock-Divide Control

The programmable clock-divide control bits (CD1 and CD0) provide the processor with the ability to adapt to different crystals and to slow the system clocks, providing lower power operation when required. An on-chip crystal multiplier allows the DS89C430 to operate at two or four times the crystal frequency by setting the 4X/$\overline{2X}$ bit, and is enabled by setting the CTM bit to a logic 1. An additional circuit provides a clock source at divide by 1024. When used with a 7.372MHz crystal, for example, the processor executes the machine cycle in times ranging from 33.9ns (mulitply-by-4 mode) to 138.9µs (divide-by-1024 mode) and maintains a highly accurate serial port baud rate, while allowing the use of more cost-effective lower frequency crystals. Although the clock-divide control bits can be written at any time, certain hardware features enhance the use of these clock controls to guarantee proper serial port operation and to allow for a high-speed response to an external interrupt. The 01b setting of CD1 and CD0 is reserved. It has the same effect as the setting of 10b, which forces the system clock into a divide-by-1 mode. The DS89C430 defaults to divide-by-1 clock mode on all forms of reset.

When in divide-by-1024 mode, in order to allow a quick response to incoming data on a serial port, the system uses the switchback mode to automatically revert to divide-by-1 mode whenever a start bit is detected. This automatic switchback is only enabled in divide-by-1024 mode when the switchback bit (PMR.5:SWB) is set. All other clock modes are unaffected by interrupts and serial port activity.

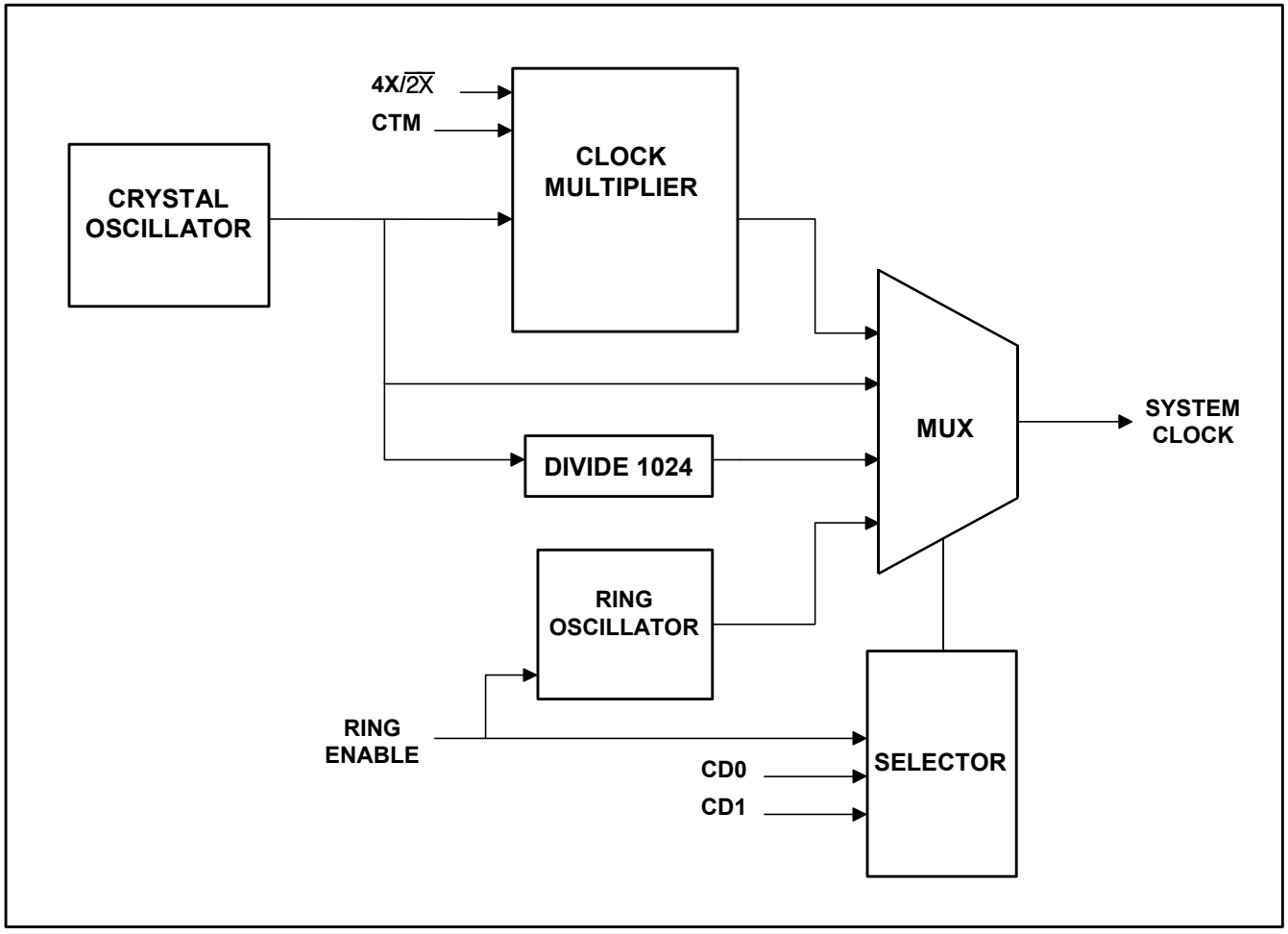
The oscillator multiply ratios of 4, 2, and 1 are also used to provide standard baud-rate generation for the serial ports through a forced divide-by-12 input clock (TxMH,TxM = 00b, x = 1, 2, or 3) to the timers.

Use of the multiply-by-4 or multiply-by-2 options through the clock-divide control bits requires that the crystal multiplier be enabled and the specific system-clock-multiply value be established by the 4X/$\overline{2X}$ bit in the PMR register. The multiplier is enabled through the CTM (PMR.4) bit but cannot be automatically selected until a startup delay has been established through the CKRY bit in the status register. The 4X/$\overline{2X}$ bit can only be altered when the CTM bit is cleared to a logic 0. This prevents the system from changing the multiplier until the system has moved back to the divide-by-1 mode and the multiplier has been disabled by the CTM bit. The CTM bit can only be altered when the CD1 and CD0 bits are set to divide-by-1 mode and the RGMD bit is cleared to 0. Setting the CTM to a logic 1 from a previous logic 0 automatically clears the CKRY bit in the status register and starts the multiplier startup timeout in the multiplier startup counter. During the multiplier startup period, the CKRY bit remains cleared and the CD1 and CD0 clock controls cannot be set to 00b. The CTM bit is cleared to a logic 0 on all resets.

Note that the rated maximum speed of operation applies to the speed of the microcontroller core, not the external clock source. When using the clock multiplier feature, the external clock source frequency, multiplied by the clock multiplier (2X or 4X) can never be faster than the maximum rated speed of the device. Thus, if a designer wished to use the 4X clock multiplier on a device rated at 33MHz, the maximum external clock speed would be 8.25MHz.

Figure 14 gives a simplified description of the generation of the system clocks. Specifics of hardware restrictions associated with the use of the 4X/$\overline{2X}$ CTM, CKRY, CD1, and CD0 bits are outlined in the *SFR* section.

Figure 14. System Clock Sources



Bandgap-Monitored Interrupt and Reset Generation

The power monitor in the DS89C430 monitors the V_{CC} pin in relation to the on-chip bandgap voltage reference. Whenever V_{CC} falls below V_{PFW}, an interrupt is generated if the corresponding power-fail interrupt-enable bit EPFI (WDCON.5) is set, causing the device to vector to address 33h. The power-fail interrupt status bit PFI (WDCON.4) is set any time V_{CC} transitions below V_{PFW}, and can only be cleared by software once set. Similarly, as V_{CC} falls below V_{RST}, a reset is issued internally to halt program execution. Following power-up, a power-on reset initiates a power-on reset timeout before starting program execution. When V_{CC} is first applied to the DS89C430, the processor is held in reset until $V_{CC} > V_{RST}$ and a delay of 65,536 oscillator cycles has elapsed, to ensure that power is within tolerance and the clock source has had time to stabilize. Once the reset timeout period has elapsed, the reset condition is removed automatically and software execution begins at the reset vector location of 0000h. The power-on reset flag POR (WDCON.6) is set to logic 1 to indicate a power-on reset has occurred, and can only be cleared by software.

When the DS89C430 enters stop mode, the bandgap, reset comparator, and power-fail interrupt comparator are automatically disabled to conserve power if the BGS (EXIF.0) bit is set to logic 0. This is the lowest power mode. If BGS is set to logic 1, the bandgap reference, reset comparator, and the power-fail comparator are powered up, although in a mode that reduces their power consumption.

Watchdog Timer

The watchdog timer functions as the source of both the watchdog interrupt and the watchdog reset. When the clock divider is set to 10b, the interrupt timeout has a default divide ratio of 2^{17} of the crystal oscillator clock, with the watchdog reset set to time out 512 system clock cycles later. This results in a 33MHz crystal oscillator producing an interrupt timeout every 3.9718ms, followed 15.5µs later by a watchdog reset. The watchdog timer is reset to the default divide ratio following any reset. Using the WD0 and WD1 bits in the clock control (CKCON.6 and 7) register, other divide ratios can be selected for longer watchdog interrupt periods. Table 13 summarizes the watchdog bits settings and the timeout values. **Note:** All watchdog timer reset timeouts follow the programmed interrupt timeouts by 512 system clock cycles, which equates to varying numbers of oscillator cycles depending on the clock divide (CD1:0) and crystal multiplier settings.

Table 13. Watchdog Timeout Value (In Number of Oscillator Clocks)

4X/$\overline{2X}$	CD1:0	WATCHDOG INTERRUPT TIMEOUT				WATCHDOG RESET TIMEOUT			
		WD1:0 = 00	WD1:0 = 01	WD1:0 = 10	WD1:0 = 11	WD1:0 = 00	WD1:0 = 01	WD1:0 = 10	WD1:0 = 11
1	00	2^{15}	2^{18}	2^{21}	2^{24}	2^{15} + 128	2^{18} + 128	2^{21} + 128	2^{24} + 128
0	00	2^{16}	2^{19}	2^{22}	2^{25}	2^{16} + 256	2^{19} + 256	2^{22} + 256	2^{25} + 256
x	01	2^{17}	2^{20}	2^{23}	2^{26}	2^{17} + 512	2^{20} + 512	2^{23} + 512	2^{26} + 512
x	10	2^{17}	2^{20}	2^{23}	2^{26}	2^{17} + 512	2^{20} + 512	2^{23} + 512	2^{26} + 512
x	11	2^{27}	2^{30}	2^{33}	2^{36}	2^{27} + 524,288	2^{30} + 524,288	2^{33} + 524,288	2^{36} + 524,288

A watchdog control (WDCON) SFR is used for programming the functions. EWT (WDCON.1) is the enable for the watchdog timer-reset function and RWT (WDCON.0) is the bit used to restart the watchdog timer. Setting the RWT bit restarts the timer for another full interval. If the watchdog timer-reset function is masked by the EWT bit and no resets are issued to the timer through the RWT bit, the watchdog timer generates interrupt timeouts at a rate determined by the programmed divide ratio. WDIF (WDCON.3) is the interrupt flag set at timer termination and WTRF (WDCON.2) is the reset flag set following a watchdog reset timeout. Setting the EWDI bit (EIE.4) enables the watchdog interrupt. The watchdog timer reset and interrupt timeouts are measured by counting system clock cycles.

An independent watchdog timer functions as the crystal startup counter to count 65,536 crystal clock cycles before allowing the crystal oscillator to function as the system clock. This warmup time is verified by the watchdog timer following each power-up as well as each time the crystal is restarted following a stop mode. The watchdog is also used to establish a startup time whenever the CTM in the PMR register is set to enable the crystal multiplier (4X/$\overline{2X}$).

One of the watchdog timer applications is for the watchdog to wake up the system from idle mode. The watchdog interrupt can be programmed to allow a system to wake up periodically to sample the external world.

Internal System Reset

A software reset can be initiated by writing a system reset command to the flash control SFR. The reset state is maintained for approximately 90 external clock cycles. During this time, the RST pin is driven to a logic high. Once the reset is removed, the RST pin is driven low, and operation begins from address 0000h.

External/Hardware Reset

A hardware reset can be initiated by asserting the RST pin high for at least three external clock cycles while the external clock is running. The reset is asserted immediately.

When the RST pin is taken to a logic low, the microcontroller exits the reset state within a delay that depends on the state of the flash memory at the time the reset was asserted. If a flash write or erase operation was in progress, the reset state is a 4ms maximum. If no flash write or erase operations were in progress, there is a delay of 90 external clock cycles. Operation resumes at address 0000h. If taking RST to a logic low causes the device to exit stop mode, an additional delay of 65,536 clock cycles is experienced before operation begins.

Reset Output

If a reset is caused by a power-fail reset, a watchdog timer reset, or an internal system reset, a logic high output-reset pulse is also generated at the bidirectional RST pin. This reset pulse is asserted as long as an internal reset is asserted. Although the microcontroller generates its own power-on delay for crystal warmup, legacy designs may employ an external RC circuit. Large values of “C” may load the pin enough that the RST output may not achieve a logic high, but the state of the external RST pin does not affect the internal reset condition.

Oscillator-Fail Detect and Reset

The DS89C430 incorporates an oscillator-fail-detect circuit that, when enabled, causes a reset if the crystal oscillator frequency falls below 20kHz and holds the chip in reset with the ring oscillator operating. Setting the OFDE (PCON.4) bit to logic 1 enables the circuit. The OFDE bit is only cleared from logic 1 to logic 0 by a power-fail reset or by software. A reset caused by an oscillator failure also sets the OFDF (PCON.5) to logic 1. This flag is cleared by software or power-on reset. This circuit does not force a reset when the oscillator is stopped by the software-enabled stop mode.

Power-Management Mode

The power-management mode offers a software-controllable power-saving scheme by providing a reduced instruction cycle speed, which allows the microcontroller to continue operating while using an internally divided version of the clock source to save power. Power-management mode is invoked by software setting the clock-divide control bits CD1 and CD0 (PMR.7–6) bits to 11b, which sets an operating rate of 1024 oscillator cycles for one machine cycle. On all forms of reset, the clock-divide control bits default to 10b, which selects one oscillator cycle per machine cycle.

Since the clock speed choice affects all functional logic, including timers, several hardware switchback features allow the clock speed to automatically return to the divide-by-1 mode from a reduced cycle rate. Setting the SWB (PMR.5) bit to 1 in software enables this switchback function.

When CD1 and CD0 are programmed to the divide-by-1024 mode and the SWB bit is also enabled, the system forces the clock-divide control bits to automatically reset to the divide-by-1 mode whenever the system detects an externally enabled (and allowed by nesting priorities) interrupt. The switchback occurs whenever one of the two following conditions occurs. The first switchback condition is initiated by the detection of a low on either $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$, or $\overline{\text{INT5}}$ or a high on INT2 or INT4 when the respective pin has been programmed and allowed (by nesting priorities) to issue an interrupt. The second switchback condition occurs when either serial port is enabled to receive data and is found to have an active-low transition on the respective receive-input pin. Serial port transmit activity also forces a switchback if the SWB is set. Note that the serial port activity, as related to the switchback, is independent of the serial port interrupt relationship. Any attempt to change the clock divider to the divide-by-1024 mode while the serial port is either transmitting or receiving has no effect, leaving the clock control in the divide-by-1 mode. Note also that the switchback interrupt relationship requires that the respective external interrupt source is allowed to actually generate an interrupt, as defined by the priority of the interrupt and the state of the nested interrupts, before the switchback can actually occur. An interrupt by the serial port is not required, nor is the setting of serial port enable. Disabling external interrupts and serial port receive/transmission mode disables the automatic switchback mode. Clearing the SWB bit also disables the switchback, and all interrupt and serial port controls of the clock divider are disabled. All other clock modes ignore the switchback relationship and are unaffected by interrupts and serial port activity.

The basic divide-by-12 mode for the timers (TxMH, TxM = 00b) as well as the divide by 32 and 64 for mode 2 on the serial ports has been maintained when running the processor with the oscillator divide ratio of 0.25, 0.5, and 1.

Serial ports and timers track the oscillator cycles per machine cycle when the higher divide ratio of 1024 is selected, and require the switchback function to automatically return to the divide-by-1 mode for proper operation when a qualified event occurs. Table 14 summarizes the effect of clock mode on timer operation.

It is possible to enable a receive function on a serial port when incoming data is not present and then change to the higher divide ratio. An inactive serial port receive/transmission mode requires the receive input pin to remain high and all outgoing transmissions to be completed. During this inactive receive mode it is possible to change the clock-divide control bits from a divide by 1 to a 1024 divide ratio. In the case when the serial port is being used to receive or transmit data, it is very important to validate an attempted change in the clock-divide control bits (read CD1 and CD0 to verify write was allowed) before proceeding with low-power program functions.

Table 14. Effect of Clock Mode on Timer Operation (In Number of Oscillator Clocks)

4X/$\overline{2X}$, CD1, CD0	OSC CYCLES PER MACHINE CYCLE	OSC CYCLES PER TIMERS 0, 1, 2 CLOCK TxMH,TxM =			OSC CYCLES PER TIMER 2 CLOCK BAUD RATE GENERATION	OSC CYCLES PER SERIAL PORT CLOCK MODE 0		OSC CYCLES PER SERIAL PORT CLOCK MODE 2	
		00	01	1x	T2MH,T2M = xx	SM2 = 0	SM2 = 1	SMOD = 0	SMOD = 1
100	0.25	12	1	0.25	2	3	1	64	32
000	0.5	12	2	0.5	2	6	2	64	32
x01	1 (reserved)								
x10	1 (default)	12	4	1	2	12	4	64	32
x11	1024	12,288	4096	1024	2048	12,288	4096	65,536	32,768

x = Don't care.

Ring Oscillator

When the system is in stop mode the crystal is disabled. When stop mode is removed, the crystal requires a period of time to start up and stabilize. To allow the system to begin immediate execution of software following the removal of the stop mode, the ring oscillator is used to supply a system clock until the crystal startup time is satisfied. Once this time has passed, the ring oscillator is switched off and the system clock is switched to the crystal oscillator. This function is programmable and is enabled by setting the RGSL bit (EXIF.1) to logic 1. When it is logic 0, the processor delays software execution until after the 65,536 crystal clock periods. To allow the processor to know whether it is being clocked by the ring or by the crystal oscillator, an additional bit—RGMD—indicates which clock source is being used. When the processor is running from the ring, the clock-divide control bits (CD1 and CD0 in the PMR register) are locked into the divide-by-1 mode (CD1:CD0 = 10b). The clock-divide control bits cannot be changed from this state until after the system clock transitions to the crystal oscillator (RGMD = 0).

Note: The watchdog is connected to the crystal oscillator and continues to run at the external clock rate. The ring oscillator does not drive it.

Idle Mode

Idle mode suspends the processor by holding the program counter in a static state. No instructions are fetched and no processing occurs. Setting the IDLE bit (PCON.0) to logic 1 invokes idle mode. The instruction that executes this step is the last instruction prior to freezing the program counter. Once in idle mode, all resources are preserved, but all peripheral clocks remain active and the timers, watchdog, serial ports, and power monitor functions continue to operate, so that the processor can exit the idle mode using any interrupt sources that are enabled. The oscillator-detect circuit also continues to function when enabled. The IDLE bit is cleared automatically once the idle mode is exited. On returning from the interrupt vector using the RETI instruction, the next address is the one that immediately follows the instruction that invoked the idle mode. Any reset of the processor also removes the idle mode.

Stop Mode

Stop mode disables all circuits within the processor. All on-chip clocks, timers, and serial port communication are stopped, and no processing is possible.

Stop mode is invoked by setting the stop bit (PCON.1) to logic 1. The processor enters stop mode on the instruction that sets the bit. The processor can exit stop mode by using any of the six external interrupts that are enabled.

An external reset through the RST pin unconditionally exits the processor from stop mode. If the BGS bit is set to logic 1, the bandgap provides a reset while in stop mode if V_{CC} should drop below the V_{RST} level. If BGS is 0, no reset is generated if V_{CC} drops below V_{RST}.

When the stop mode is removed, the processor waits for 65,536 clock cycles for the internal flash memory to warm up before starting normal execution. Also, the processor waits for the crystal warmup period if it is not using the ring oscillator.

Serial I/O

The microcontroller provides a serial port (UART) that is identical to the 80C52. In addition, it includes a second hardware serial port that is a full duplicate of the standard one. This port optionally uses pins P1.2 (RXD1) and P1.3 (TXD1) and has duplicate control functions included in new SFR locations.

Both ports can operate simultaneously but can be at different baud rates or modes. The second serial port has similar control registers (SCON1 at C0h, SBUF1 at C1h) to the original. The new serial port can only use timer 1 for timer-generated baud rates.

Control for serial port 0 is provided by the SCON0 register, while its I/O buffer is SBUF0. The registers SCON1 and SBUF1 provide the same functions for the second serial port. A full description of the use and operation of both serial ports can be found in the *Ultra-High-Speed Flash Microcontroller User's Guide.*

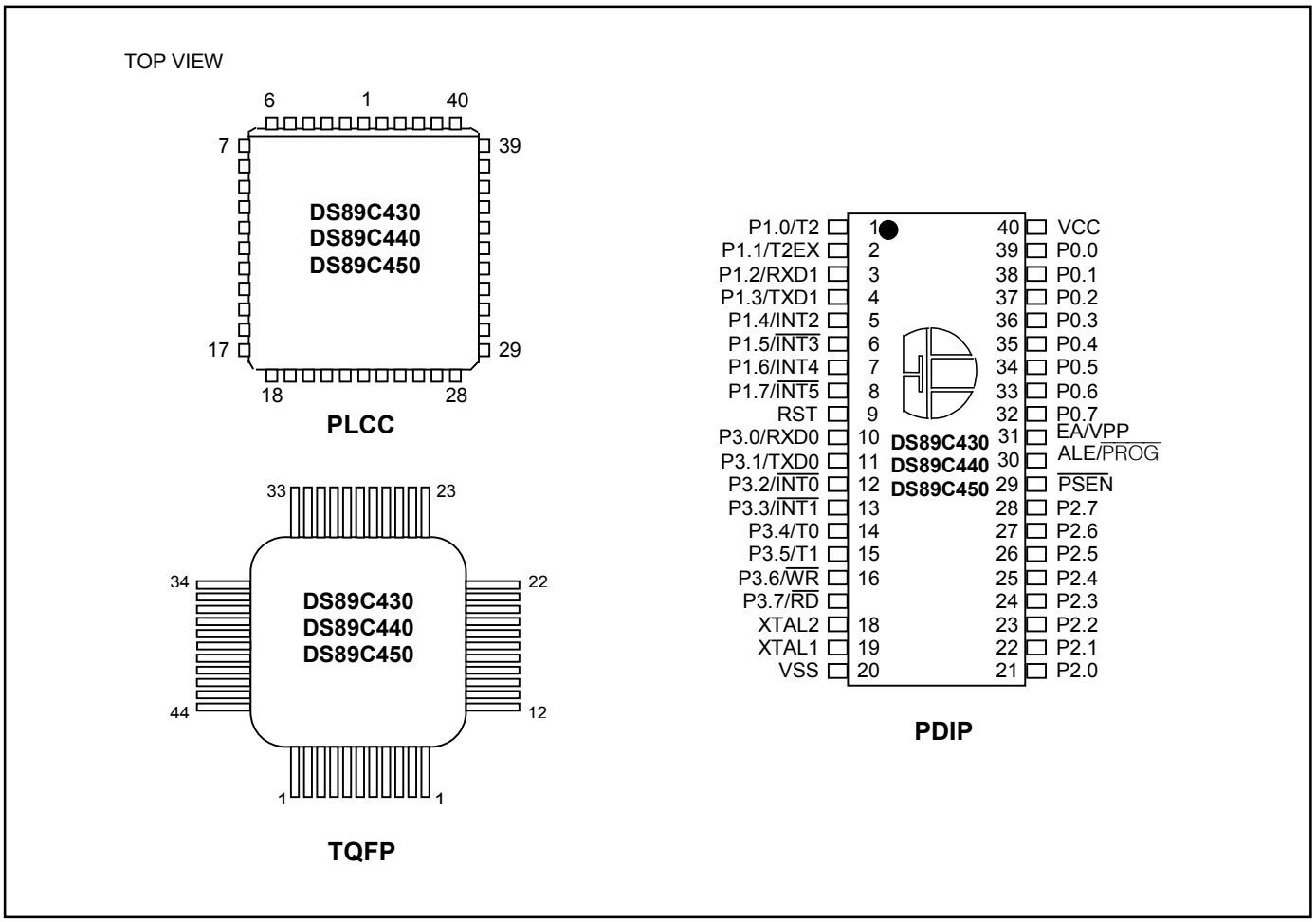
Instruction Set

All instructions are 100% binary compatible with the industry-standard 8051, and are only different in the number of machine cycles used for the instructions. There are some special conditions and features to be considered when analyzing the DS89C430 instruction set. Full details are available in the *Ultra-High-Speed Flash Microcontroller User's Guide.*

SELECTOR GUIDE

PART	TEMP RANGE	FLASH MEMORY SIZE	MAX CLOCK SPEED (MHz)	PIN-PACKAGE
DS89C430-MNL	-40°C to +85°C	16kB x 8	33	40 PDIP
DS89C430-QNL	-40°C to +85°C	16kB x 8	33	44 PLCC
DS89C430-ENL	-40°C to +85°C	16kB x 8	33	44 TQFP
DS89C440-MNL	-40°C to +85°C	32kB x 8	33	40 PDIP
DS89C440-QNL	-40°C to +85°C	32kB x 8	33	44 PLCC
DS89C440-ENL	-40°C to +85°C	32kB x 8	33	44 TQFP
DS89C450-MNL	-40°C to +85°C	64kB x 8	33	40 PDIP
DS89C450-QNL	-40°C to +85°C	64kB x 8	33	44 PLCC
DS89C450-ENL	-40°C to +85°C	64kB x 8	33	44 TQFP
DS89C430-MNG	-40°C to +85°C	16kB x 8	25	40 PDIP
DS89C430-QNG	-40°C to +85°C	16kB x 8	25	44 PLCC
DS89C430-ENG	-40°C to +85°C	16kB x 8	25	44 TQFP
DS89C440-MNG	-40°C to +85°C	32kB x 8	25	40 PDIP
DS89C440-QNG	-40°C to +85°C	32kB x 8	25	44 PLCC
DS89C440-ENG	-40°C to +85°C	32kB x 8	25	44 TQFP
DS89C450-MNG	-40°C to +85°C	64kB x 8	25	40 PDIP
DS89C450-QNG	-40°C to +85°C	64kB x 8	25	44 PLCC
DS89C450-ENG	-40°C to +85°C	64kB x 8	25	44 TQFP

PIN CONFIGURATIONS

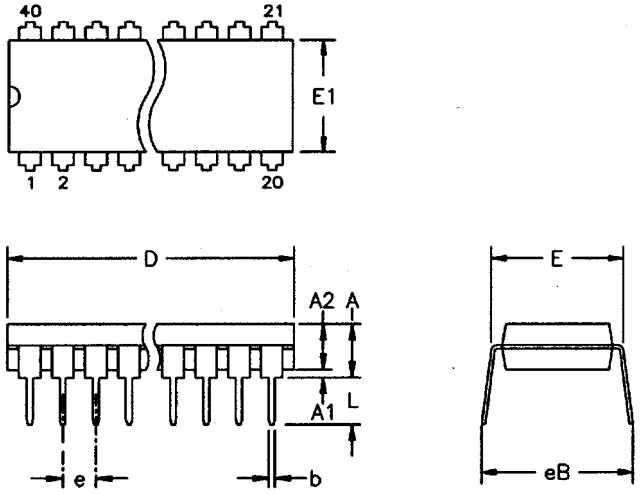


REVISION HISTORY

DATE	DESCRIPTION
111003	New product release.
032204	*DC Electrical Characteristics* table: Corrected typo—Under Supply Current for Active and Idle Mode, changed Units from "μA" to "mA." Note 15: Changed number of external clock cyles per system clock and minimum external clock speeds. *Flash Memory Programming Characteristics* table: Removed Note 20 (room temperature only) from the Data Retention parameter.
060204	Changed Write/Erase Endurance parameter from 20,000 cycles to 10,000 cycles. Removed original Table 5. *Parallel Programming Instruction Set*, and replaced it with a paragraph introducing the subject and advising interested parties to contact the factory for more information. Clarified IAP programming sequence.

PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)



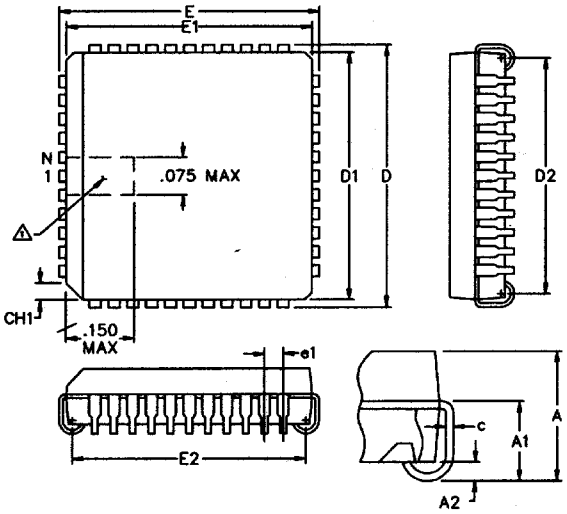
Note: *Dimensions are in inches.*

PKG	40-PIN PDIP	
DIM	**MIN**	**MAX**
A	—	0.200
A1	0.015	—
A2	0.140	0.160
B	0.014	0.022
C	0.008	0.012
D	1.980	2.085
E	0.600	0.625
E1	0.530	0.555
E	0.090	0.110
L	0.115	0.145
EB	0.600	0.700

56-G5000-000

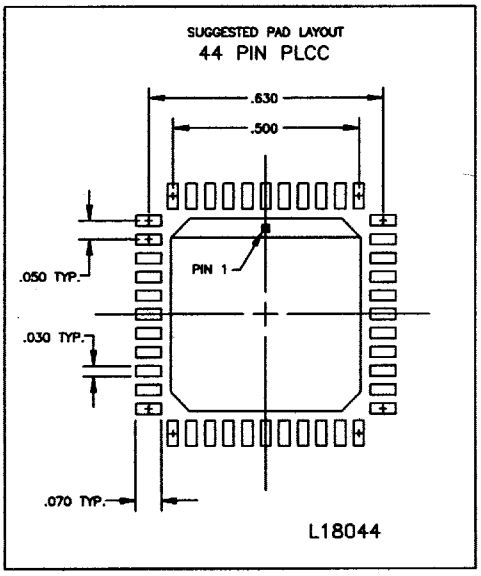
PACKAGE INFORMATION (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)



PKG	44–PIN	
DIM	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A2	0.020	–
B	0.026	0.033
B1	0.013	0.021
c	0.009	0.012
CH1	0.042	0.048
D	0.685	0.695
D1	0.650	0.656
D2	0.590	0.630
E	0.685	0.695
E1	0.650	0.656
E2	0.590	0.630
e1	0.050 BSC	
N	44	–

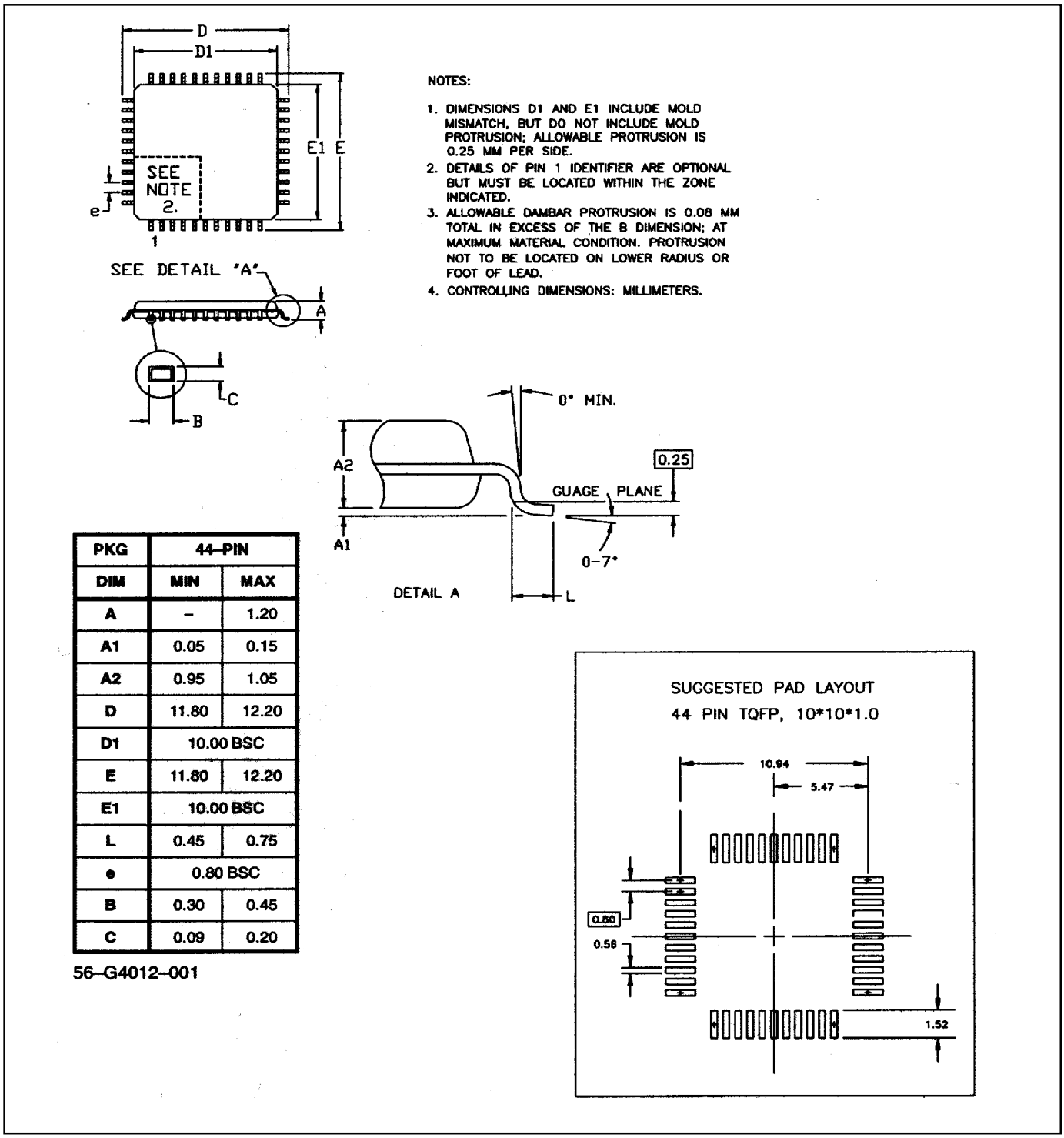
56–G4003–001



NOTE 1: PIN 1 IDENTIFIER TO BE LOCATED IN ZONE INDICATED.
NOTE 2: CONTROLLING DIMENSION ARE IN INCHES.

PACKAGE INFORMATION (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)



PKG	44-PIN	
DIM	MIN	MAX
A	–	1.20
A1	0.05	0.15
A2	0.95	1.05
D	11.80	12.20
D1	10.00 BSC	
E	11.80	12.20
E1	10.00 BSC	
L	0.45	0.75
e	0.80 BSC	
B	0.30	0.45
C	0.09	0.20

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