AWT6314R

Dual-band CDMA/PCS 3.4 V/28 dBm
Linear Power Amplifier Module

Data Sheet - Rev 2.0

FEATURES

- Single Mode Operation: $P_{OUT} \leq +28$ dBm
- High Efficiency: 39 %
- 25 % Package Size Reduction
- Common V_{MODE} Control Line
- Simplified V_{CC} Bus PCB routing
- Reduced External Component Count
- Low Profile Surface Mount Package: 1.1 mm
- RoHS Compliant Package, 250 °C MSL-3

APPLICATIONS

- CDMA/EVDO Cell & PCS dual-band Wireless Handouts and Data Devices

M23 Package
12 Pin 3 mm x 5 mm x 1 mm
Surface Mount Module

PRODUCT DESCRIPTION

The AWT6314R meets the increasing demands for higher levels of integration in dual-band CDMA/PCS 1X handsets, while reducing board area requirements by 25 %. The package pinout was chosen to enable handset manufacturers to easily route V_{CC} to both power amplifiers and simplify control with a common V_{MODE} pin. The device is manufactured on an advanced InGaP HBT MMIC technology offering state-of-the-art reliability, temperature stability, and ruggedness. Selectable bias modes that optimize efficiency for different output power levels, and a shutdown mode with low leakage current, serve to increase handset talk and standby time. The self contained 3 mm x 5 mm x 1 mm surface mount package incorporates matching networks optimized for output power, efficiency and linearity in a 50 Ω system.

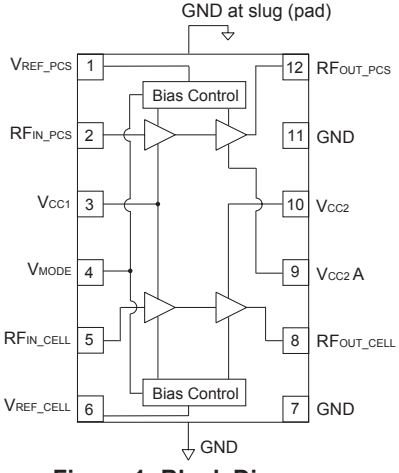


Figure 1: Block Diagram

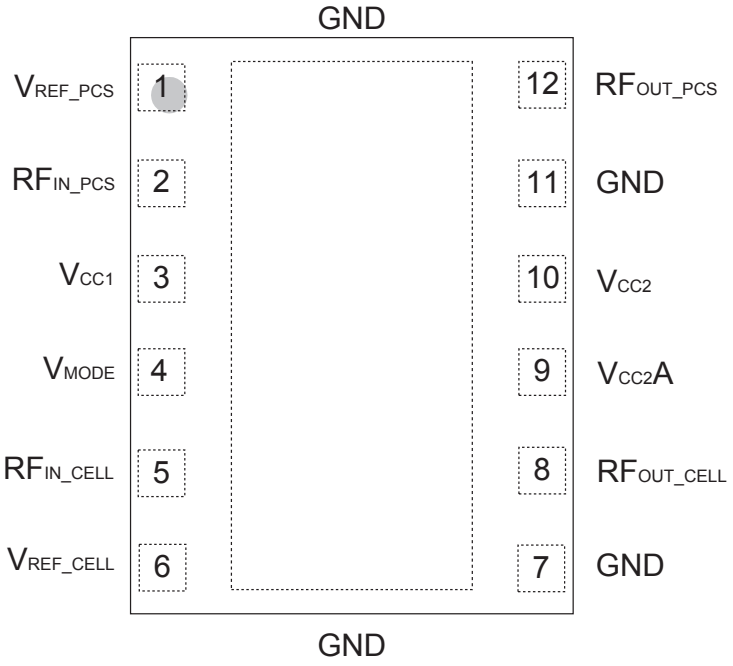


Figure 2: Pinout

Table 1: Pin Description Table

PIN	NAME	DESCRIPTION
1	V_{REF_PCS}	Reference Voltage for PCS Band
2	RF_{IN_PCS}	RF Input for PCS Band
3	V_{CC1}	Supply Voltage
4	V_{MODE}	Mode Control Voltage
5	RF_{IN_CELL}	RF Input for Cell Band
6	V_{REF_CELL}	Reference Voltage for Cell Band
7	GND	Ground
8	RF_{OUT_CELL}	RF Output for Cell Band
9	$V_{CC2}A$	Supply Voltage
10	V_{CC2}	Supply Voltage
11	GND	Ground
12	RF_{OUT_PCS}	RF Output for PCS Band

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Supply Voltage (V_{CC}) With RF Drive DC Only	 0 0	 +5 +8	V
Mode Control Voltage (V_{MODE})	0	+3.5	V
Reference Voltage (V_{REF})	0	+3.5	V
RF Input Power (P_{IN})	-	+10	dBm
Storage Temperature (T_{STG})	-40	+150	°C

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (f)	824 1850	-	849 1910	MHz	Cellular PCS
Supply Voltage (V_{CC})	+3.2	+3.4	+4.2	V	
Reference Voltage (V_{REF})	+2.75 0	+2.85 -	+3.1 +0.5	V	PA "on" PA "shut down"
Mode Control Voltage (V_{MODE})	+2.5 0	+2.85 -	+3.1 +0.5	V	Low Bias Mode High Bias Mode
RF Output Power (P_{OUT})	30.5(1) 27.5(1)	31.0 28.0	- -	dBm	AMPS CDMA
Case Temperature (T_C)	-30	-	+85	°C	

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Notes:
(1) For operation at V_{CC} = +3.2 V, P_{OUT} is derated by 0.5 dB.

Table 4: Electrical Specifications - Cellular CDMA Operation
(T_C = +25 °C, V_{CC} = +3.4 V, V_{REF} = +2.85 V, 50 Ω system)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Gain	25 24 23.5	27.0 26.5 25.5	30 29 28	dB	P_{OUT} = +28 dBm, V_{MODE} = 0 V P_{OUT} = +28 dBm, V_{MODE} = +2.85 V P_{OUT} = +16 dBm, V_{MODE} = +2.85 V
Adjacent Channel Power at ±885 kHz offset (1) Primary Channel BW = 1.23 MHZ Adjacent Channel BW = 30 kH	 - - -	 -50 -50 -49	 -47 -47 -47	dBc	 P_{OUT} = +28 dBm, V_{MODE} = 0 V P_{OUT} = +28 dBm, V_{MODE} = +2.85 V P_{OUT} = +16 dBm, V_{MODE} = +2.85 V
Adjacent Channel Power at ±1.98 MHz offset (1) Primary Channel BW = 1.23 MHZ Adjacent Channel BW = 30 kHz	 - - -	 -62 -60 -65	 -57 -57 -57	dBc	 P_{OUT} = +28 dBm, V_{MODE} = 0 V P_{OUT} = +28 dBm, V_{MODE} = +2.85 V P_{OUT} = +16 dBm, V_{MODE} = +2.85 V
Power-Added Efficiency (1)	37 37 8	39 40 9	- - -	%	P_{OUT} = +28 dBm, V_{MODE} = 0 V P_{OUT} = +28 dBm, V_{MODE} = +2.85 V P_{OUT} = +16 dBm, V_{MODE} = +2.85 V
Quiescent Current (Icq)	-	50	68	mA	V_{MODE} = +2.85 V, Low Bias
Reference Current	-	1.5	3	mA	through V_{REF} pin, PA "ON"
Mode Control Current	-	0.6	1.0	mA	through V_{MODE} pin, V_{MODE} = +2.85 V
Leakage Current	-	<1	5	μA	V_{CC} = +4.3 V, V_{REF} = 0 V, V_{MODE} = 0 V
Noise in Receive Band	-	-133	-131	dBm/Hz	869 MHz to 894 MHz
Harmonics 2fo 3fo, 4fo	 - -	 -44 -46	 -30 -30	dBc	
Input Impedance	-	-	2:1	VSWR	
Spurious Output Level (all spurious outputs)	-	-	-65	dBc	$P_{OUT} \leq$ +28 dBm In-band Load VSWR < 5:1 Out-of-band Load VSWR < 10:1 Applies over all operating conditions
Load mismatch stress with no permanent degradation or failure	10:1	-	-	VSWR	Applies over all operating conditions

Notes:
(1) PAE and ACP limit applies at 836.5 MHz.

Table 5: PCS Electrical Specifications
(T_C = +25 °C, V_{CC} = +3.4 V, V_{REF} = +2.85 V, 50 Ω system)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Gain	24.5 24 23	26.5 26.0 25.5	29 28 27.5	dB	P_{OUT} = +28 dBm, V_{MODE} = 0 V P_{OUT} = +28 dBm, V_{MODE} = +2.85 V P_{OUT} = +16 dBm, V_{MODE} = +2.85 V
Adjacent Channel Power at ±1.25 MHz offset Primary Channel BW - 1.23 MHz Adjacent Channel BW = 30 kHz	 - - -	 -49 -50 -54	 -46.5 -47 -47	dBc	 P_{OUT} = +28 dBm, V_{MODE} = 0 V P_{OUT} = +28 dBm, V_{MODE} = +2.85 V P_{OUT} = +16 dBm, V_{MODE} = +2.85 V
Adjacent Channel Power at ±2.25 MHz offset Primary Channel BW - 1.23 MHz Adjacent Channel BW = 30 kHz	 - - -	 -62 -61 -67	 -57 -57 -57	dBc	 P_{OUT} = +28 dBm, V_{MODE} = 0 V P_{OUT} = +28 dBm, V_{MODE} = +2.85 V P_{OUT} = +16 dBm, V_{MODE} = +2.85 V
Power-Added Efficiency	36 36 7.5	38 39 9	- - -	%	P_{OUT} = +28 dBm, V_{MODE} = 0 V P_{OUT} = +28 dBm, V_{MODE} = +2.85 V P_{OUT} = +16 dBm, V_{MODE} = +2.85 V
Quiescent Current (Icq)	-	53	70	mA	V_{MODE} = +2.85 V
Reference Current	-	2.3	4	mA	through V_{REF} pin, PA "on"
Mode Control Current	-	0.6	1.0	mA	through V_{MODE} pin, V_{MODE} = +2.85 V
Leakage Current	-	<1	5	µA	V_{CC} = +4.3 V, V_{REF} = 0 V, V_{MODE} = 0 V
Noise in Receive Band	-	-133	-131	dBm/Hz	1930 MHz to 1990 MHz
Harmonics 2fo 3fo, 4fo	 - -	 -47 -55	 -30 -30	dBc	
Input Impedance	-	-	2:1	VSWR	
Spurious Output Level (all spurious outputs)	-	-	-65	dBc	P_{OUT} ≤ +28 dBm In-band load VSWR < 5:1 Out-of-band load VSWR < 10:1 Applies over all operating ranges
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating range

Notes:
(1) ACPRs and efficiency limits at mid-band only.

APPLICATION INFORMATION

To ensure proper performance, refer to all related Application Notes on the ANADIGICS web site: http://www.anadigics.com

Shutdown Mode

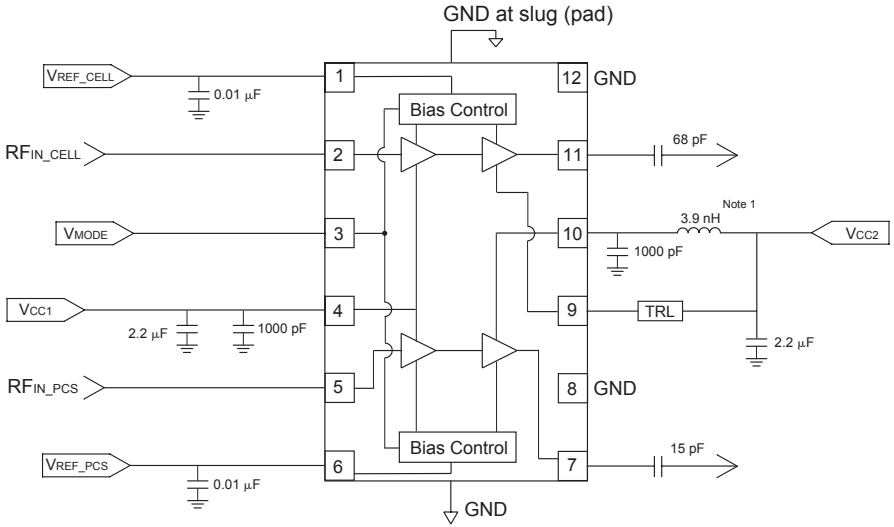
The power amplifier may be placed in a shutdown mode by applying a logic low levels (see Operating Ranges table) to both the V_{REF} and V_{MODE} voltages.

Bias Modes

The power amplifier may be placed in either a Low Bias mode or a High Bias mode by applying the appropriate logic level (see Operating Ranges table) to the V_{MODE} voltage. The Bias Control table lists the recommended modes of operation for various applications.

Table 6: Bias Control

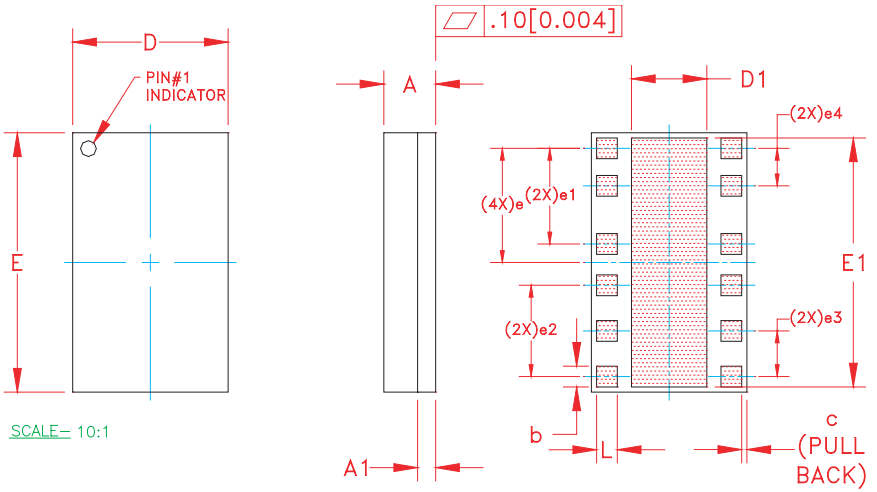
APPLICATION	P_{OUT} LEVELS	BIAS MODE	V_{REF}	V_{MODE}
CDMA - All power	≤28 dBm	Low	+2.85 V	+2.85 V
CDMA - All power	≤28 dBm	High	+2.85 V	0 V
Shutdown	-	Shutdown	0 V	0 V



Note:
1. 3.9 nH Inductor should be rated for >1 Amp.

Figure 3: Application Circuit

PACKAGE OUTLINE



SYMBOL	MILLIMETERS			INCHES			NOTE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.90	1.00	1.10	0.035	0.039	0.043	–
A1	–	0.35	–	–	0.014	–	–
b	0.35	–	0.60	0.014	–	0.024	3
c	–	0.10	–	–	0.004	–	–
D	2.88	3.00	3.12	0.113	0.118	0.122	–
D1	1.40	–	1.60	0.055	–	0.063	–
E	4.88	5.00	5.12	0.192	0.196	0.201	–
E1	4.75	–	4.85	0.187	–	0.190	–
e		2.20			0.087		3
e1		1.85			0.073		3
e2		1.75			0.069		3
e3		0.88			0.035		3
e4		0.71			0.028		3
L	0.35	–	0.60	0.014	–	0.024	3

NOTES:

1. CONTROLLING DIMENSIONS: MILLIMETERS
2. UNLESS SPECIFIED TOLERANCE=±0.076[0.003].
3. PADS (INCLUDING CENTER) SHOWN UNIFORM SIZE FOR REFERENCE ONLY. ACTUAL PAD SIZE AND LOCATION WILL VARY WITHIN MIN. AND MAX. DIMENSIONS ACCORDING TO SPECIFIC LAMINATE DESIGN.
4. UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.

Figure 4: Package Outline - 12 Pin 3 mm x 5 mm x 1 mm Surface Mount Module

TOP BRAND

NOTES:

1. ANADIGICS LOGO SIZE: NONE
2. PART NUMBER: FOUR DIGIT NUMERICAL
3. WAFER LOT NUMBER: LLLLL = LOT NUMBER
   NN = WAFER I.D.
4. PIN 1 INDICATOR: LASER DOT
5. B.O.M. #: BBBB
6. Year and Work Week: YY = Year, WW = Work Week
7. COUNTRY CODE: CC = TH–for–THAILAND, TW–for–TAIWAN
   CC = PH–for–PHILIPPINES, CH–for–CHINA
8. TYPE : ARIAL
   SIZE : 1.5–POINT
   COLOR : LASER

Figure 5: Branding Specification

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
AWT6314RM23Q7	-30 °C to +85 °C	RoHS Compliant 12 Pin 3 mm x 5 mm x 1 mm Surface Mount Module	Tape and Reel, 2500 pieces per Reel
AWT6314RM23P9	-30 °C to +85 °C	RoHS Compliant 12 Pin 3 mm x 5 mm x 1 mm Surface Mount Module	Partial Tape and Reel

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