AsahiKASEI
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AKD4648-C

Evaluation board Rev.1 for AK4648

GENERAL DESCRIPTION

AKD4648 is an evaluation board for the AK4648, stereo CODEC with MIC/HP/SPK amplifier. The AKD4648 can evaluate A/D converter and D/A converter separately in addition to loopback mode (A/D → D/A). The AKD4648 also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD4648 --- Evaluation board for AK4648
(Cable, USB interface board for connecting with USB port, and control software are packed with this. This control software does not support Windows NT.)

FUNCTION

- **DIT/DIR with optical input/output**
- **10pin Header for digital audio interface**
- **10pin Header for serial control mode**

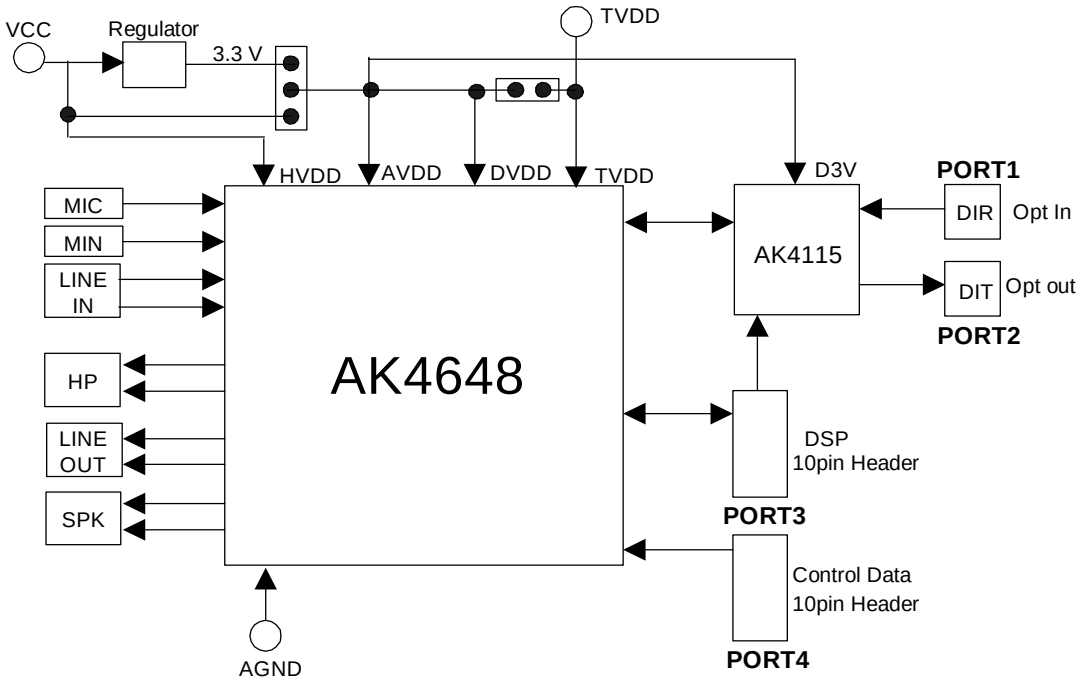


Figure 1. AKD4648-C Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual

Evaluation Board Manual

■ Operation sequence

(1) Set up the power supply lines.

(1-1) In case of using the regulator.

(1-1-1) TVDD is supplied from the regulator.

Set up the jumper pins.

JP	JP22	JP23
	REG_SEL	TVDD_SEL
State	REG	Short

Set up the power supply lines.

[VCC] (red) = 4.3 ~ 5.0V : typ. 4.5V for regulator and HVDD of AK4648
(regulator 3.3V output : AVDD, DVDD and TVDD of the AK4648 and logic)
[TVDD] (orange) = Open
[AGND] (black) = 0V : for analog ground
[DGND] (black) = 0V : for logic ground

(1-1-2) TVDD is supplied from the power supply connector of "TVDD".

Set up the jumper pins.

JP	JP22	JP23
	REG_SEL	TVDD_SEL
State	REG	Open

Set up the power supply lines.

[VCC] (red) = 4.3 ~ 5.0V : typ. 4.5V for regulator and HVDD of AK4648
(regulator 3.3V output : AVDD and DVDD of the AK4648 and logic)
[TVDD] (orange) = 1.6 ~ 3.6V : typ. 3.3V for TVDD of AK4648 (TVDD ≤ DVDD)
[AGND] (black) = 0V : for analog ground
[DGND] (black) = 0V : for logic ground

(1-2) When the regulator is not used.

Set up the jumper pins.

JP	JP22	JP23
	REG_SEL	TVDD_SEL
State	VCC	Open

Set up the power supply lines.

[VCC] (red) = 2.6 ~ 3.6V : typ. 3.3V for AVDD, DVDD and HVDD of AK4648 and logic
[TVDD] (orange) = 1.6 ~ 3.6V : typ. 3.3V for TVDD of AK4648 (TVDD ≤ DVDD)
[AGND] (black) = 0V : for analog ground
[DGND] (black) = 0V : for logic ground

* Each supply line should be distributed from the power supply unit.

(2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

(3) Power on.

The AK4648 and AK4115 should be reset once bringing SW1 (PDN) "L" upon power-up.

■ Evaluation mode

In case of AK4648 evaluation using AK4115, it is necessary to correspond to audio interface format for AK4648 and AK4115. About AK4648's audio interface format, refer to datasheet of AK4648. About AK4115's audio interface format, refer to Table 2 on page 11 in this manual.
Sampling frequency (fs) of AK4115 is 22kHz or more. If the fs is slower than 22kHz, please use other mode. In addition, MCLK of AK4115 supports 256fs and 512fs. When evaluating it in a condition except this, please use other mode.

(1) External Slave Mode
- (1-1) Evaluation of A/D using DIT of AK4115
- (1-2) Evaluation of D/A using DIR of AK4115
- (1-3) Evaluation of Loop-back using AK4115 <Default>
- (1-4) All interface signals are fed externally

(2) External Master Mode
- (2-1) Evaluation of A/D using DIT of AK4115
- (2-2) Evaluation of D/A using DIR of AK4115
- (2-3) Evaluation of Loop-back using AK4115
- (2-4) All interface signals are fed externally

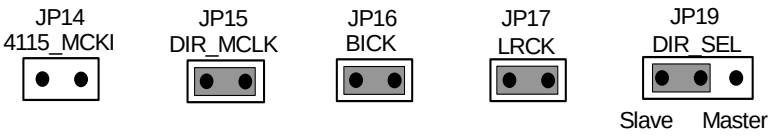
(3) PLL Slave Mode
- (3-1) Reference Clock : MCKI pin
  - (3-1-1) Evaluation of A/D using DIT of AK4115
  - (3-1-2) Evaluation of Loop-back using AK4115
  - (3-1-3) All interface signals are fed externally
- (3-2) Reference Clock : BICK or LRCK pin
  - (3-2-1) Evaluation of A/D using DIT of AK4115
  - (3-2-2) Evaluation of D/A using DIR of AK4115
  - (3-2-3) Evaluation of Loop-back using AK4115
  - (3-2-4) All interface signals are fed externally

(4) PLL Master Mode
- (4-1) Evaluation of A/D using DIT of AK4115
- (4-2) Evaluation of Loop-back using AK4115
- (4-3) All interface signals are fed externally

(1) External Slave Mode

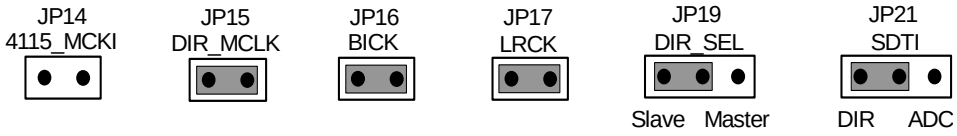
(1-1) Evaluation of A/D using DIT of AK4115

PORT2 (DIT) and X1 (X'tal) are used. DIT generates audio bi-phase signal from received data and which is output through optical connector (TOTX141). Nothing should be connected to PORT1 (DIR) and PORT3 (DSP). The jumper pins should be set as follows.



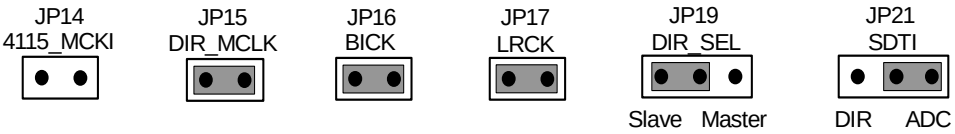
(1-2) Evaluation of D/A using DIR of AK4115

PORT1 (DIR) is used. Nothing should be connected to PORT2 (DIT) and PORT3 (DSP).
The jumper pins should be set as follows.



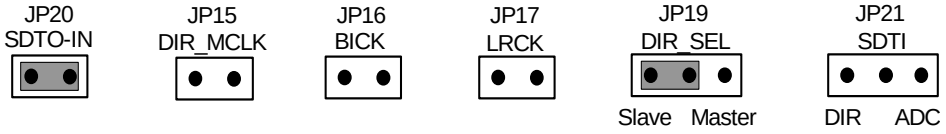
(1-3) Evaluation of Loop-back using AK4115 <Default>

X1 (X'tal) is used. Nothing should be connected to PORT1 (DIR) and PORT3 (DSP).
The jumper pins should be set as follows.



(1-4) All interface signals are fed externally

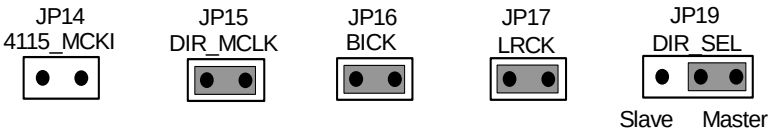
PORT3 (DSP) is used. Nothing should be connected to PORT1 (DIR) and PORT2 (DIT).
The jumper pins should be set follows.



(2) External Master Mode

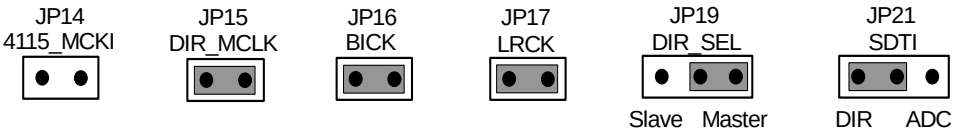
(2-1) Evaluation of A/D using DIT of AK4115

PORT2 (DIT) and X1 (X'tal) are used. Nothing should be connected to PORT1 (DIR) and PORT3 (DSP).
In Master Mode, BICK and LRCK of AK4648 should be input to AK4115. Please refer to Table2 on page 11.
The jumper pins should be set as follows.



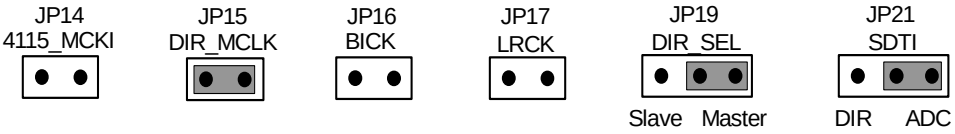
(2-2) Evaluation of D/A using DIR of AK4115

PORT1 (DIR) is used. Nothing should be connected to PORT2 (DIT) and PORT3 (DSP).
In Master Mode, BICK and LRCK of AK4648 should be input to AK4115. Please refer to Table2 on page 11.
The jumper pins should be set as follows.



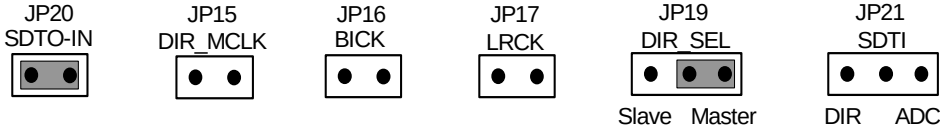
(2-3) Evaluation of Loop-back using AK4115

X1 (X'tal) is used. Nothing should be connected to PORT1 (DIR) and PORT3 (DSP).
The jumper pins should be set as follows.



(2-4) All interface signals are fed externally

PORT3 (DSP) is used. Nothing should be connected to PORT1 (DIR) and PORT2 (DIT).
The jumper pins should be set as follows.

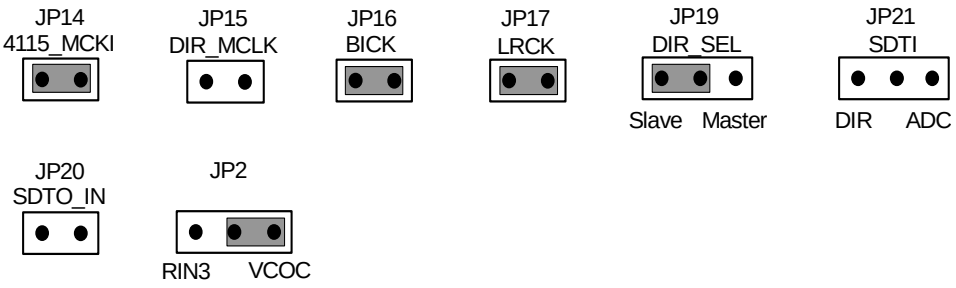


(3) PLL Slave Mode

(3-1) Reference Clock : MCKI pin

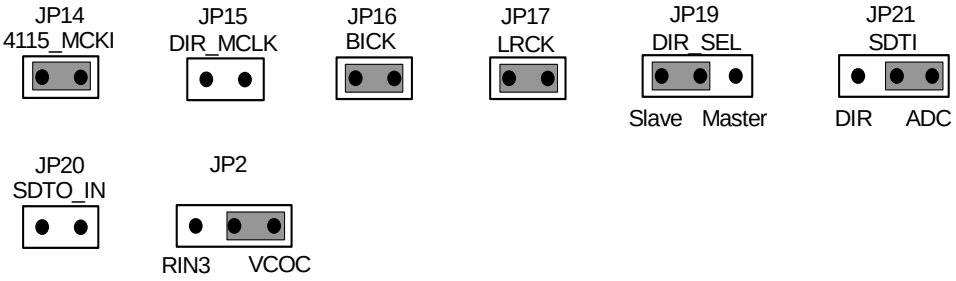
(3-1-1) Evaluation of A/D using DIT of AK4115

PORT2 (DIT) and PORT3 (DSP) are used. Nothing should be connected to PORT1 (DIR).
The system clock (PLL reference clock) should be connected to MCLK of PORT3. MCKO of AK4648 should be input to AK4115's XTI. X'tal oscillator should be removed from X1.
The jumper pins should be set as follows.



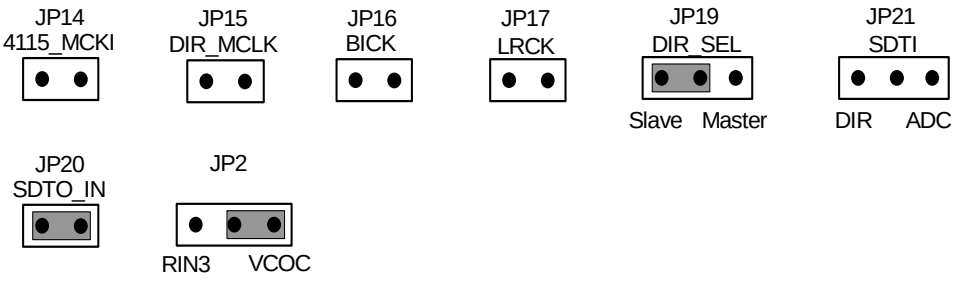
(3-1-2) Evaluation of Loop-back using AK4115

PORT2 (DIT) and PORT3 (DSP) are used. Nothing should be connected to PORT1 (DIR).
The system clock (PLL reference clock) should be connected to MCLK of PORT3. MCKO of AK4648 should be input to AK4115's XTI. X'tal oscillator should be removed from X1.
The jumper pins should be set as follows.



(3-1-3) All interface signals are fed externally

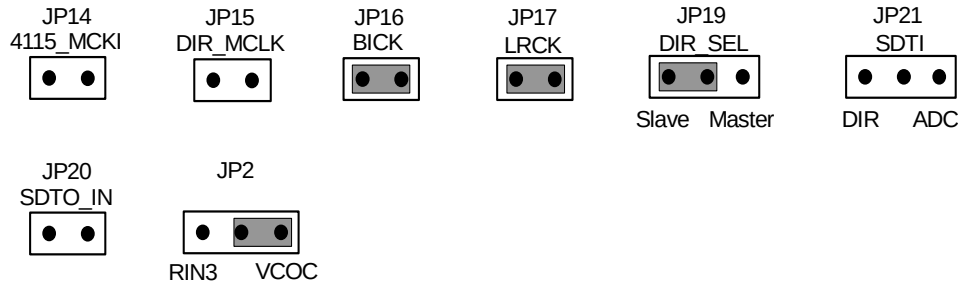
PORT3 (DSP) is used. Nothing should be connected to PORT1 (DIR) and PORT2 (DIT).
BICK and LRCK inputs should be synchronized with MCKO of AK4648.
MCLK (PLL reference clock), BICK, LRCK and SDTI are supplied from PORT3. The JP14 (4115_MCKI)'s lower side (MCKO of AK4648) should be connected to MCLK of DSP.
The jumper pins should be set as follows.



(3-2) Reference Clock : BICK or LRCK pin

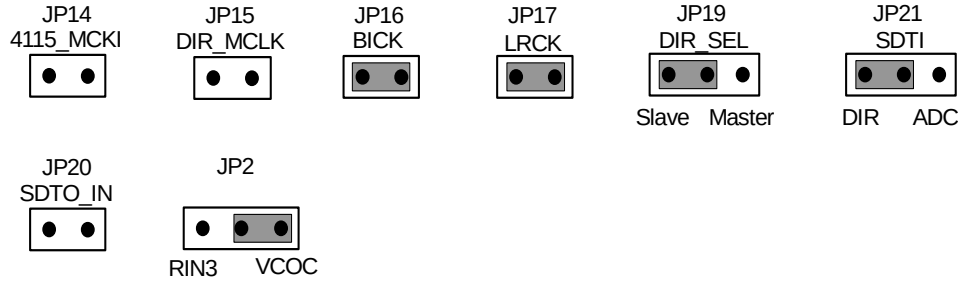
(3-2-1) Evaluation of A/D using DIT of AK4115

X1 (X'tal) and PORT2 (DIT) are used. Nothing should be connected to PORT1 (DIR).
The jumper pins should be set as follows.



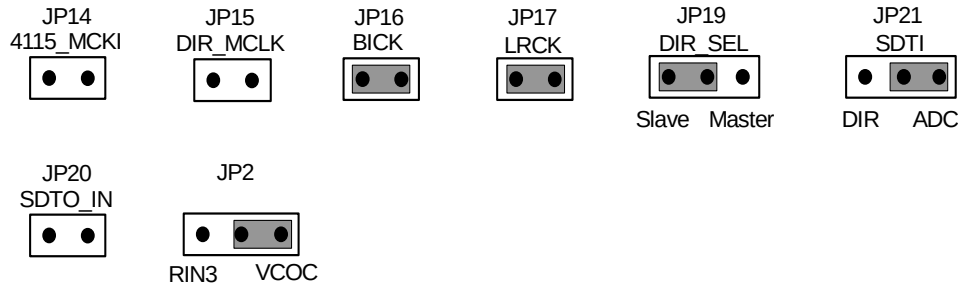
(3-2-2) Evaluation of D/A using DIR of AK4115

PORT1 (DIR) is used. Nothing should be connected to PORT2 (DIT) and PORT3 (DSP).
The jumper pins should be set as follows.



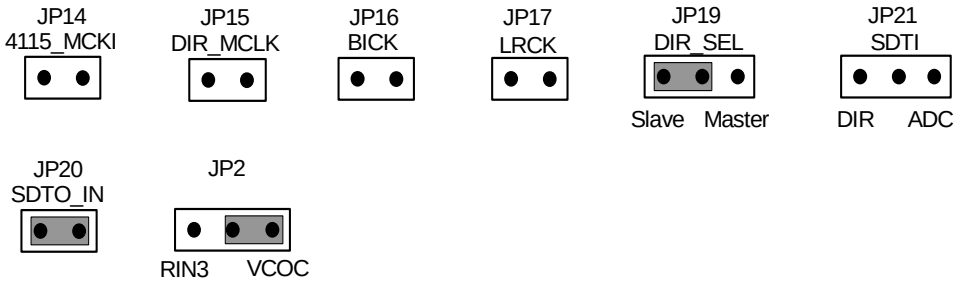
(3-2-3) Evaluation of Loop-back using AK4115

X1 (X'tal) is used. Nothing should be connected to PORT1 (DIR), PORT2 (DIT), and PORT3 (DSP).
The jumper pins should be set as follows.



(3-2-4) All interface signals are fed externally

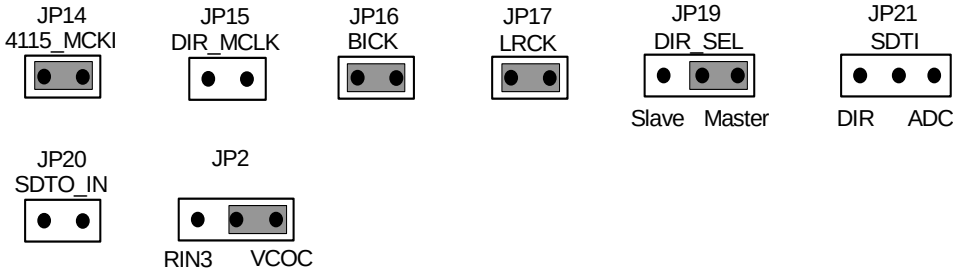
PORT3 (DSP) is used. Nothing should be connected to PORT1 (DIR) and PORT2 (DIT).
BICK, LRCK, and SDTI are supplied from PORT3.
The jumper pins should be set as follows.



(4) PLL Master Mode

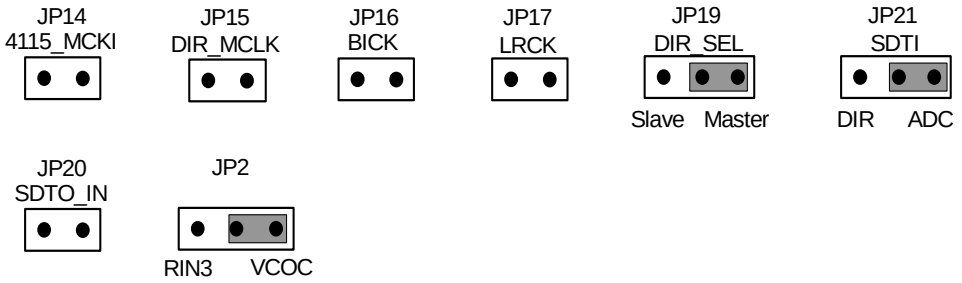
(4-1) Evaluation of A/D using DIT of AK4115

PORT2 (DIT) and PORT3 (DSP) are used. Nothing should be connected to PORT1(DIR).
The system clock (PLL reference clock) should be connected to MCLK of PORT3.
In case of supplying MCKO to DSP, the JP14 (4115_MCKI)'s lower side should be connected to MCLK of DSP.
X'tal oscillator should be removed from X1.
In Master Mode, BICK and LRCK of AK4648 should be input to AK4115. Please refer to Table2 on page 11.
The jumper pins should be set as follows.



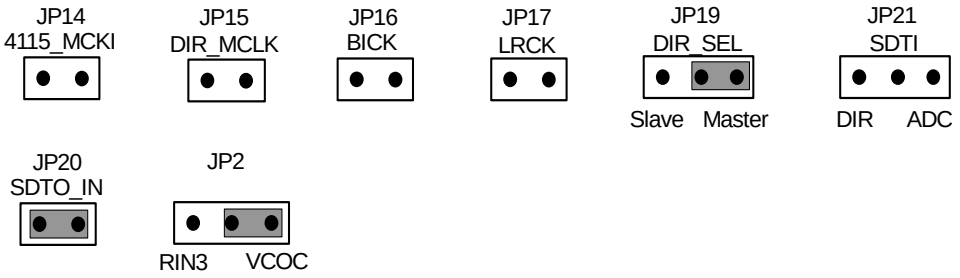
(4-2) Evaluation of Loop-back

PORT2 (DIT) and PORT3 (DSP) are used. Nothing should be connected to PORT1(DIR).
The system clock (PLL reference clock) should be connected to MCLK of PORT3.
In case of supplying MCKO to DSP, the JP14 (4115_MCKI)'s lower side should be connected to MCLK of DSP.
X'tal oscillator should be removed from X1.
The jumper pins should be set as follows.



(4-3) All interface signals are fed externally

PORT3 (DSP) is used. Nothing should be connected to PORT1 (DIR) and PORT2 (DIT).
The system clock (PLL reference clock) should be connected to MCLK of PORT3.
In case of supplying MCKO to DSP, the JP14 (4115_MCKI)'s lower side should be connected to MCLK of DSP.
X'tal oscillator should be removed from X1.
The jumper pins should be set as the follows.



■ DIP Switch set up

[S1] (SW DIP1-4): Mode setting for AK4648 and AK4115.

No.	Name	ON ("H")	OFF ("L")	Default
1	CAD0	AK4648 Chip Address Setting: (See Table 4)		OFF
2	OCKS1	AK4115 Master Clock Setting: (See Table 3)		OFF
3	DIF0	AK4115 Audio Format Setting See Table 2		OFF
4	DIF1			OFF

Table 1. Mode Setting for AK4648 and AK4115

Mode	DIF1	DIF0	DAUX	SDTO	LRCK		BICK	
						I/O		I/O
1	0	0	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O
2	0	1	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O
3	1	0	24bit, Left justified	24bit, Left justified	H/L	I	64-128fs	I
4	1	1	24bit, I^2S	24bit, I^2S	L/H	I	64-128fs	I

Table 2. Setting for AK4115 Audio Interface Format

Mode	OCKS1	MCKO1 pin	X'tal
0	0	256fs	256fs
1	1	512fs	512fs

Table 3. Setting for AK4115 Master Clock

■ Other jumper pins set up

[JP1] (GND) : Analog ground and Digital ground.
SHORT : Common. (The connector "DGND" can be open.)
OPEN : Separated. <Default>

[JP2] : Selection of RIN3 path or PLL Mode.
RIN3 : RIN3 path.
VCOC : PLL Mode. <Default>

[JP4] (LIN1) : Selection of using MIC-power supply for LIN1.
SHORT : MIC-power is supplied.
OPEN : MIC-power is not supplied. <Default>

[JP7] (RIN1) : Selection of using MIC-power supply for RIN1.
SHORT : MIC-power is supplied.
OPEN : MIC-power is not supplied. <Default>

[JP8] (LIN2) : Selection of using MIC-power supply for LIN2.
SHORT : MIC-power is supplied.
OPEN : MIC-power is not supplied. <Default>

[JP9] (RIN2) : Selection of using MIC-power supply for RIN2.
SHORT : MIC-power is supplied.
OPEN : MIC-power is not supplied. <Default>

[JP12] : Selection of LIN3 path or MIN path.
SHORT : LIN3 path.
OPEN: MIN path. <Default>

[JP14] (4114_MCKI) : AK4115 Clock Source.
OPEN : X'tal of AK4115 is used. <Default>
SHORT : MCKO of AK4648 (X'tal oscillator should be removed from X1).

[JP18] (Signal V_select) : Selection of power supply for logic(U4).
D3V : It is supplied from D3V. <Default>
TVDD : It is supplied from TVDD.

[JP20] (SDTO_IN) : SDTO of PORT3.
SHORT : It supply SDTO to PORT3.
OPEN : It does not supply SDTO to PORT3. <Default>

■ The function of the toggle SW

[SW1] (PDN): Power down of AK4648. Keep "H" during normal operation.

[SW2] (DIR): Power down of AK4115. Keep "H" during normal operation.
Keep "L" when AK4115 is not used.

*Upper-side is "H" and lower-side is "L".

■ Indication for LED

[LED1] (ERF): Monitor INT0 pin for the AK4115. LED turns on when some error has occurred to AK4115.

■ Serial Control

The AKD4648-C can be connected via the USB port with attached USB interface board. Connect PORT4 (CTRL) with PC by 10 wire flat cable packed with the AKD4648-C. Table 4 shows switch and jumper settings for serial control.

Note) When I^2C-bus is controlled by µP via PORT4, resistor value of R100 should be properly selected.

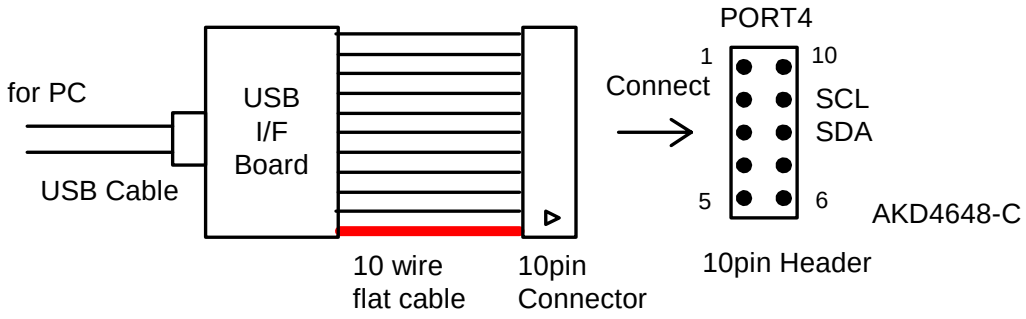


Figure 2. Connect of 10 wire flat cable

Mode		S1	
		CAD0	
I2C	CAD0=0	OFF	Default
	CAD0=1	ON	

Table 2. Serial Control Setting

■ Analog Input/Output Circuits

(1) Input Circuits

Input Circuits of LIN1/RIN1, LIN2/RIN2, LIN3/RIN3, LIN4/RIN4, and MIN.

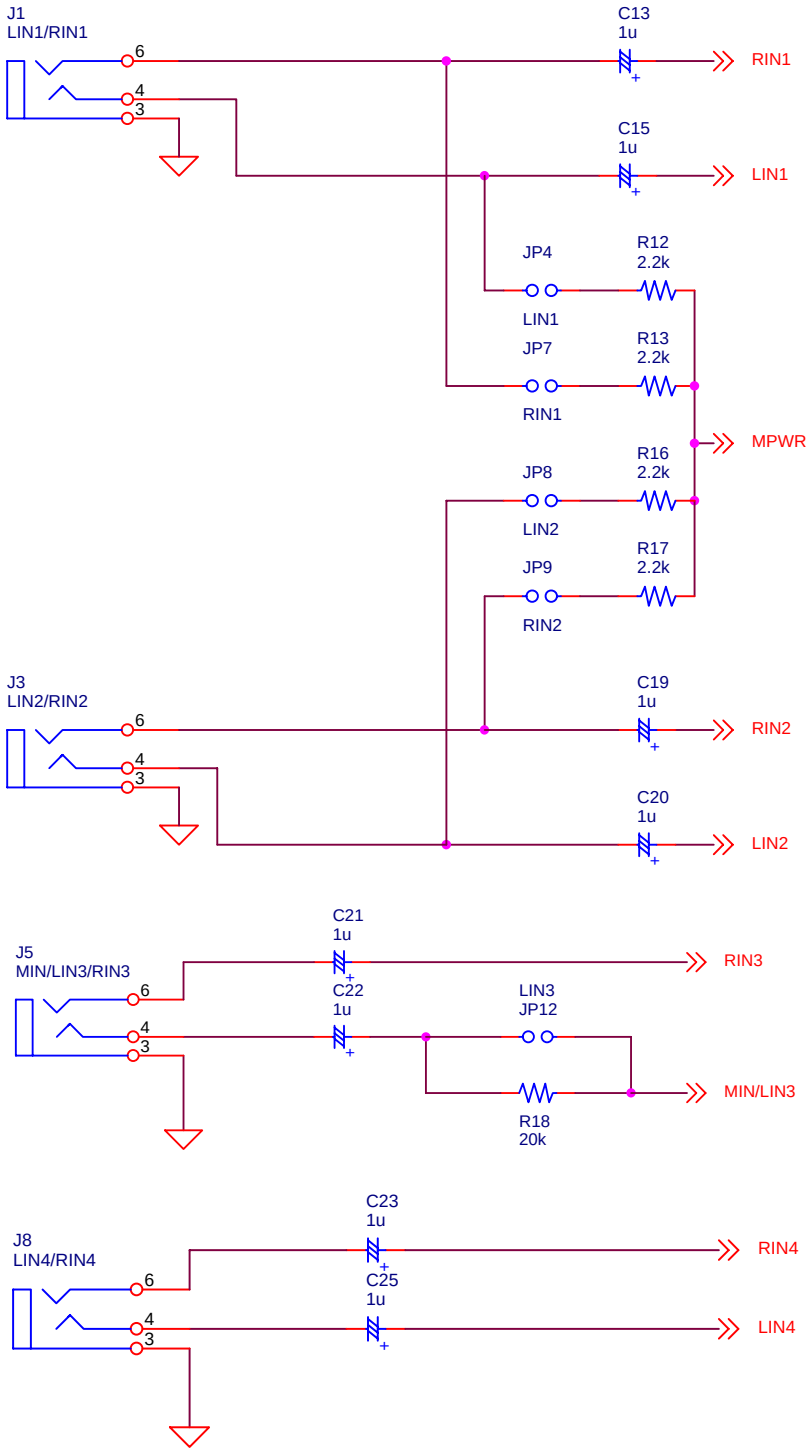
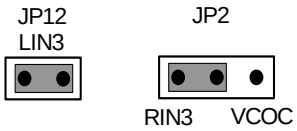
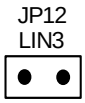


Figure 3. Input circuits LIN1/RIN1, LIN2/RIN2, LIN3/RIN3, LIN4/RIN4, and MIN

When LIN3/RIN3 paths of AK4648 are used, JP2 and JP12 should be set as follows.
AIN3 bit = "1" (Register Address 21H)



When MIN path of AK4648 is used, JP12 should be set as follows.
AIN3 bit = "1" (Register Address 21H)



When MIC- power output (MPWR pin) of AK4648 is used, JP4 (LIN1) / JP7 (RIN1) and / or JP8 (LIN2) / JP9 (RIN2) should be short.

(2) Output Circuits

(2-1) HP Output Circuit

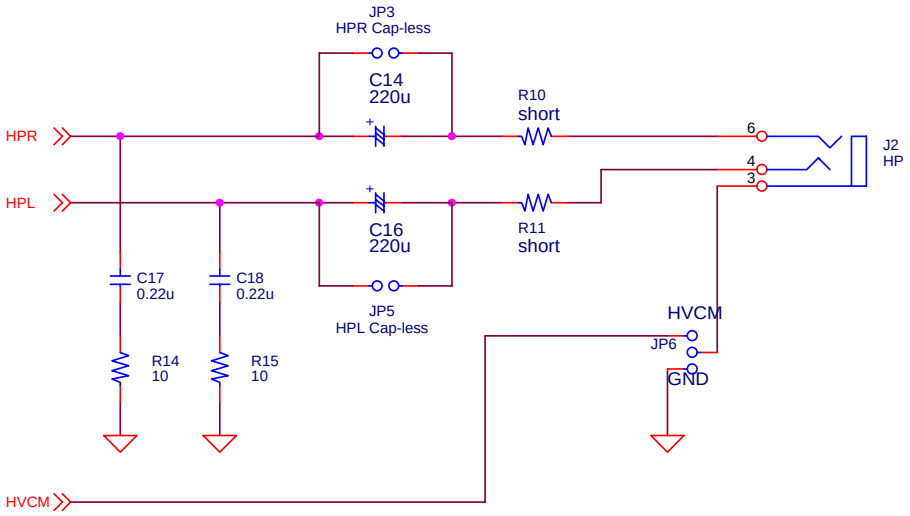
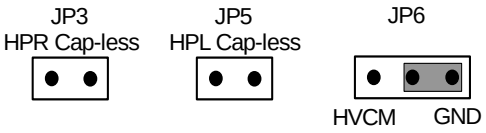


Figure 4. HP Output Circuit

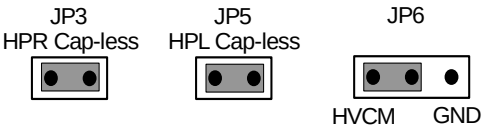
(2-1-1) Single-ended Mode

The jumper pins should be set as follows.



(2-1-2) Pseudo Cap-less Mode

The jumper pins should be set as follows.



(2-2) LOUT/ROUT Output Circuit

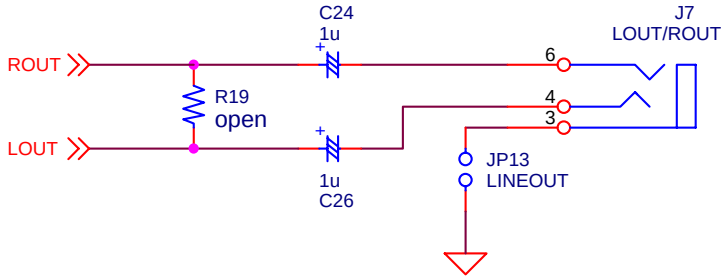
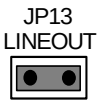


Figure 5. LOUT/ROUT Output Circuit

The jumper pins should be set as follows.



(2-3) SPK Output Circuit

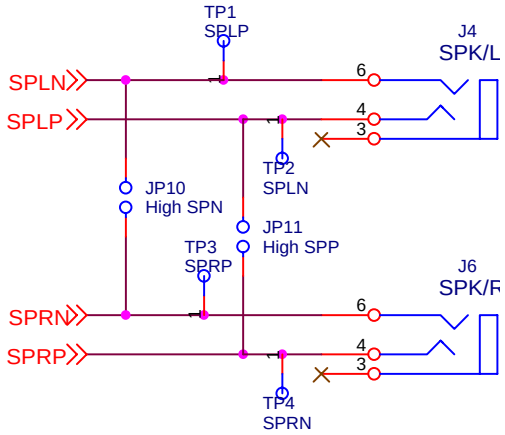
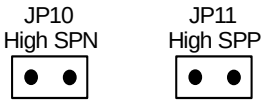


Figure 6. SPK Output Circuit

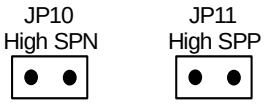
(2-3-1) Stereo SPK Mode

The jumper pins should be set as follows.



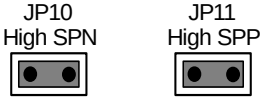
(2-3-2) Mono SPK Mode

The jumper pins should be set as follows.



(2-3-3) High Power SPK Mode

The jumper pins should be set as follows.



∗ AKM assumes no responsibility for the trouble when using the above circuit examples.

Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4648-C according to previous term.

2. Connect IBM-AT compatible PC with AKD4648-C by 10-line type flat cable via the USB port with attached USB interface board (packed with AKD4648-C). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled "AKD4648-C Evaluation Kit" into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of "AKD4648.exe" to set up the control program.

5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click "Port Reset" button.

■ Explanation of each buttons

[Port Reset] :	Set up the USB interface board (AKDUSBIF-A) .
[Write default] :	Initialize the register of AK4648.
[All Write] :	Write all registers that is currently displayed.
[Function1] :	Dialog to write data by keyboard operation.
[Function2] :	Dialog to write data by keyboard operation.
[Function3] :	The sequence of register setting can be set and executed.
[Function4] :	The sequence that is created on [Function3] can be assigned to buttons and executed.
[Function5]:	The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
[SAVE] :	Save the current register setting.
[OPEN] :	Write the saved values to all register.
[Write] :	Dialog to write data by mouse operation.
[Filter] :	Set Programmable Filter (FIL1, FIL3, EQ) of AK4648.
[5 Band EQ] :	Set 5-Band Equalizer of AK4648.

■ Indication of data

Input data is indicated on the register map. Red letter indicates "H" or "1" and blue one indicates "L" or "0". Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes “H” or “1”. If not, “L” or “0”.

If you want to write the input data to AK4648, click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog] : Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.
Data Box: Input registers data in 2 figures of hexadecimal.

If you want to write the input data to AK4648, click [OK] button. If not, click [Cancel] button.

3. [Function2 Dialog] : Dialog to evaluate IVOL and DVOL

Address Box: Input registers address in 2 figures of hexadecimal.
Start Data Box: Input starts data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to AK4648 by this interval.
Step Box: Data changes by this step.
Mode Select Box:

If you check this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

If you do not check this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

If you want to write the input data to AK4648, click [OK] button. If not, click [Cancel] button.

4. [Save] and [Open]

4-1. [Save]

Save the current register setting data. The extension of file name is “akr”.

(Operation flow)
(1) Click [Save] Button.
(2) Set the file name and push [Save] Button. The extension of file name is “akr”.

4-2. [Open]

The register setting data saved by [Save] is written to AK4648. The file type is the same as [Save].

(Operation flow)
(1) Click [Open] Button.
(2) Select the file (*.akr) and Click [Open] Button.

5. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button.

(2) Set the control sequence.
Set the address, Data and Interval time. Set "-1" to the address of the step where the sequence should be paused.

(3) Click [Start] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step.

This sequence can be saved and opened by [Save] and [Open] button on the Function3 window. The extension of file name is "aks".

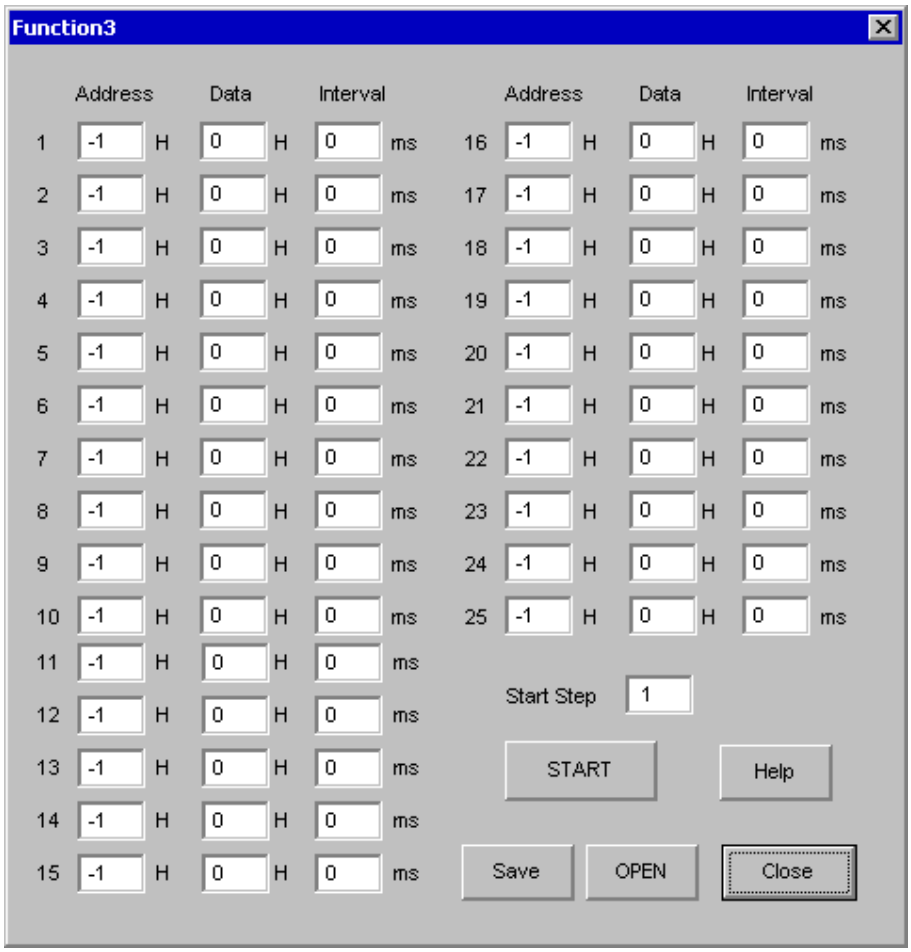


Figure 7. Window of [F3]

6. [Function4 Dialog]

The sequence that is created on [Function3] can be assigned to buttons and executed. When [F4] button is clicked, the window as shown in Figure 8 opens.

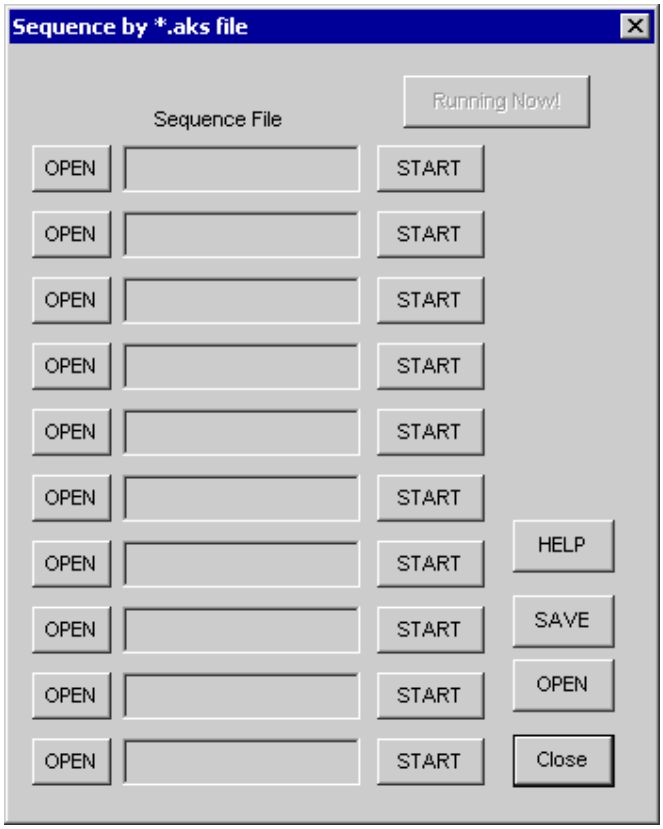


Figure 8. [F4] window

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks).

The sequence file name is displayed as shown in Figure 9.

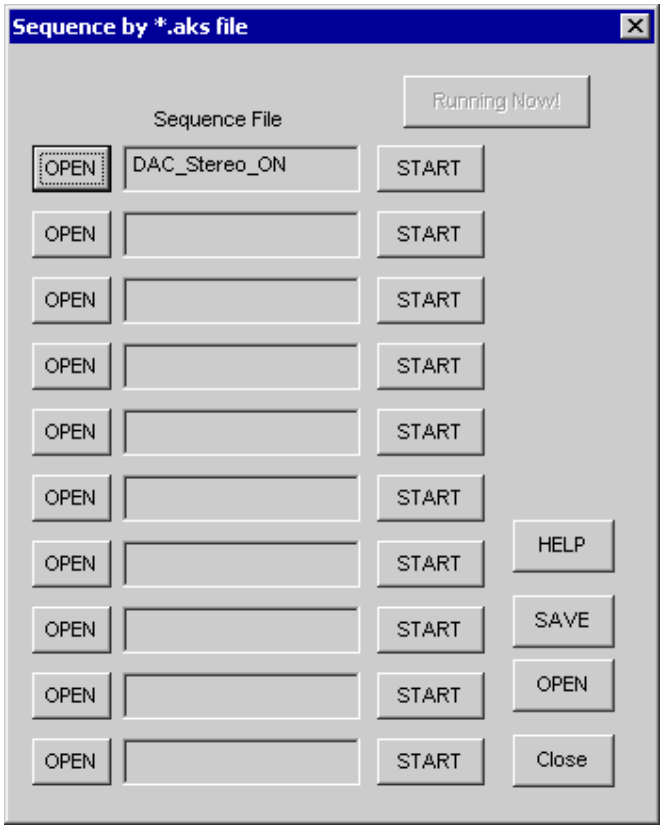


Figure 9. [F4] window(2)

(2) Click [START] button, then the sequence is executed.

3-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The sequence file names can assign be saved. The file name is *.ak4.

[OPEN] : The sequence file names assign that are saved in *.ak4 are loaded.

3-3. Note

(1) This function doesn't support the pause function of sequence function.

(2) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(3) When the sequence is changed in [Function3], the file should be loaded again in order to reflect the change.

7. [Function5 Dialog]

The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed. When [F5] button is clicked, the following window as shown in Figure 10 opens.

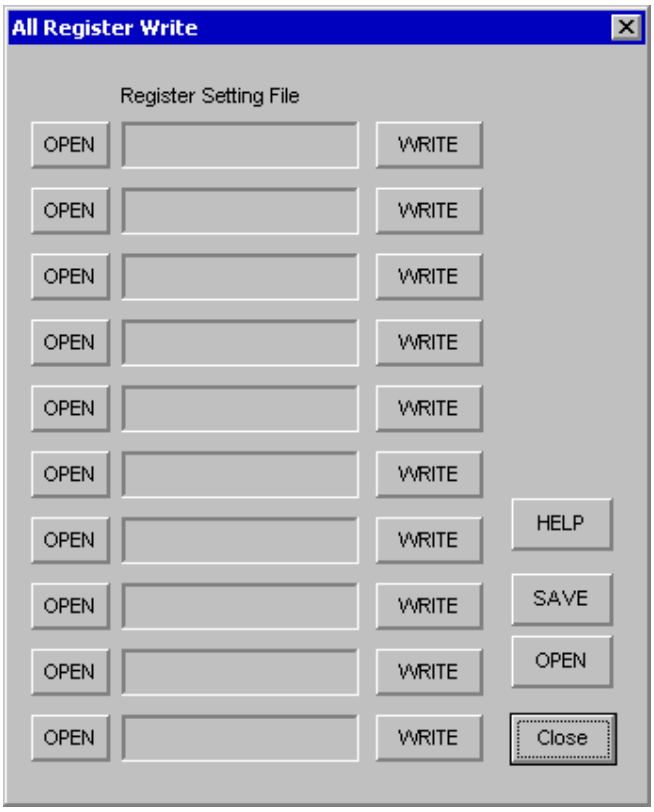


Figure 10. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

The register setting file name is displayed as shown in Figure 11.

(2) Click [WRITE] button, then the register setting is executed.

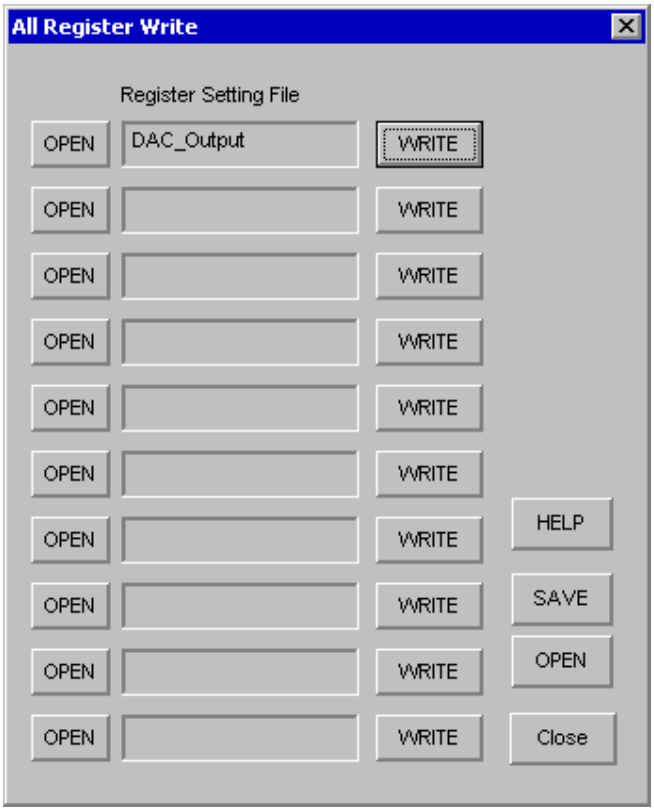


Figure 11. [F5] windows(2)

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The register setting file names assign can be saved. The file name is *.ak5.

[OPEN] : The register setting file names assign that are saved in *.ak5 are loaded.

7-3. Note

(1) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(2) When the register setting is changed by [Save] Button in main window, the file should be loaded again in order to reflect the change.

8. [Filter Dialog]

This dialog can easily set the AK4648's programmable filter.

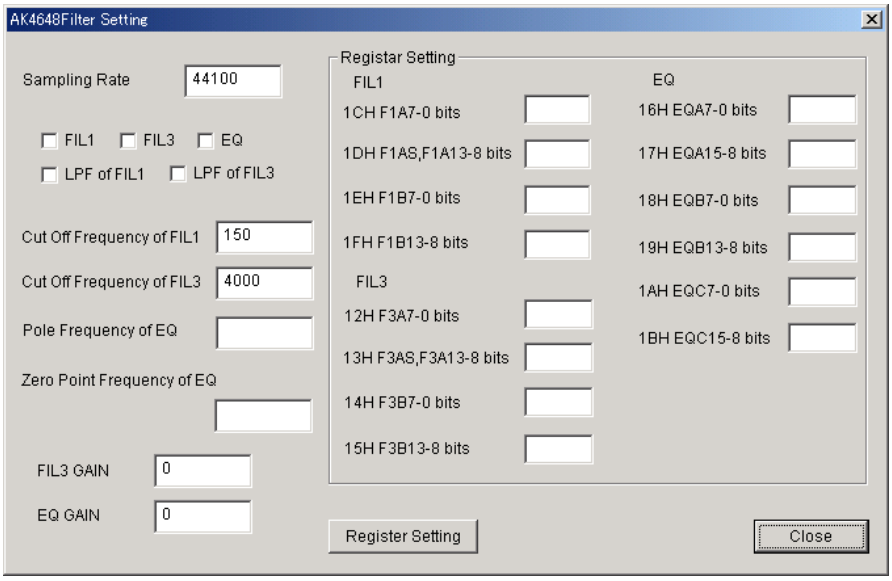


Figure 12. [Filter] window

8-1. Value input columns on left side

[Sampling Rate] → Input value of sampling frequency [unit : Hz] <default : 44100>
[Cut Off Frequency of FIL1] → Input value of cut off frequency of FIL1 [unit : Hz] <default : 150>
[Cut Off Frequency of FIL3] → Input value of cut off frequency of FIL3 [unit : Hz] <default : 4000>
[Pole Frequency of EQ] → Input value of pole frequency of EQ [unit : Hz]
[Zero Frequency of EQ] → Input value of zero frequency of EQ [unit : Hz]
[FIL3 GAIN] → Input value of gain of FIL3 (0~−10dB) [unit : dB]
[EQ GAIN] → Input value of gain of EQ (+12~0dB) [unit : dB]

8-2. Check box on left side

Check Box	Check	Check off
FIL1	FIL1 bit ="1"	FIL1 bit ="0"
FIL3	FIL3 bit ="1"	FIL3 bit ="0"
EQ	EQ bit ="1"	EQ bit ="0"
LPF of FIL1	F1AS bit ="1"(LPF)	F1AS bit ="0"(HPF)
LPF of FIL3	F3AS bit ="1"(LPF)	F3AS bit ="0"(HPF)

8-2. [Register Setting] panel and [Register Setting] button on right side

Click [Register setting] button, then filter coefficient set by 8-1 and 8-2 is written on [Register setting] panel. (It is also written to the actual control register of the AK4648.)

9. [5 Band EQ Dialog]

This dialog can easily set the AK4648's 5-Band Equalizer.

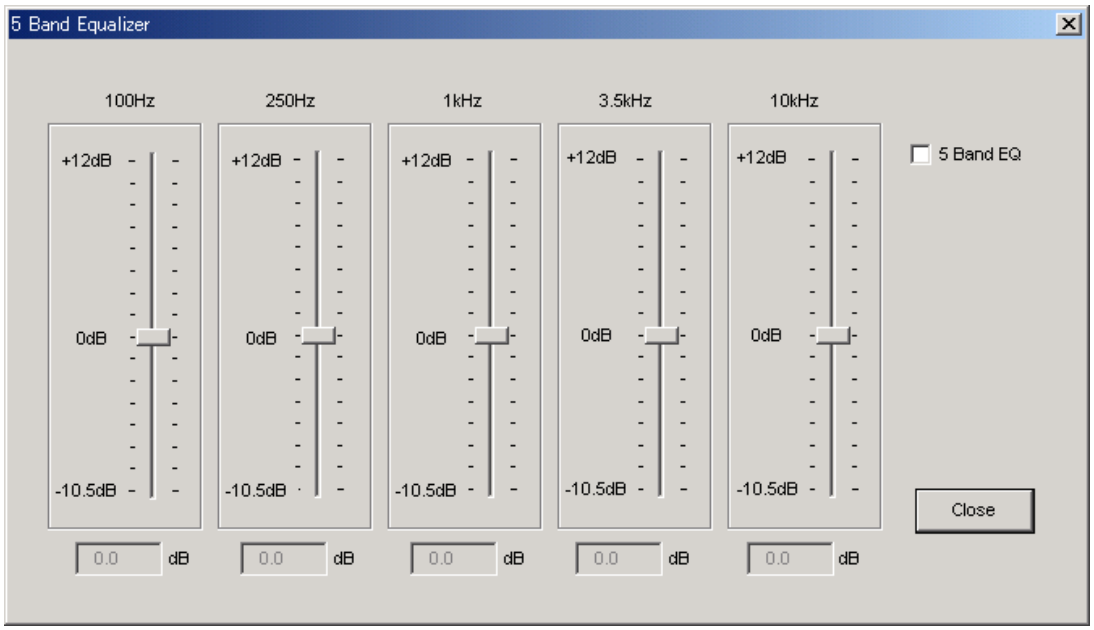


Figure 13. [5 Band EQ] window

When the check box of "5 Band EQ" is checked, 5-Band Equalizer is ON (FBEQ bit = "1").
When the slide button is changed, its value is written to the internal register immediately.

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit: Audio Precision, System two Cascade Dual Domain
- EXT Slave Mode
- BICK: 64fs
- Bit: 16bit
- Measurement Frequency: <10Hz ~ 20kHz (ADC)
  <10Hz ~ 22kHz (DAC)
- Power Supply: AVDD=DVDD=TVDD=3.3V, HVDD=4.5V
- Temperature: Room
- Input Frequency: 1kHz
- Sampling Frequency: 44.1kHz

1. TABLE DATA

ADC (LIN2/RIN2) characteristics (IVOL=0dB, ALC = OFF, LIN2/RIN2 → ADC → IVOL)

Parameter		Lch [dB]		Rch [dB]	
MIC-Amp Gain		0dB	+20dB	0dB	+20dB
S/(N+D)	20kHzLPF (–1dB)	88.6	83.2	88.5	83.2
D-range	20kHzLPF + A-weighted	95.2	86.5	95.2	86.5
S/N	20kHzLPF + A-weighted	95.3	86.5	95.3	86.5

DAC (LOUT/ROUT) characteristics (DAC → LOUT/ROUT)

Parameter		Lch [dB]	Rch [dB]
S/(N+D)	20kHzLPF (–3dB)	87.5	87.4
S/N	A-weighted	92.3	92.3

DAC (HP(Single-ended Mode)) characteristics (DAC-->HP(Single-ended Mode)), R_L=16Ω

Parameter		Lch [dB]	Rch [dB]
S/(N+D)	20kHzLPF (–3dB) (HPG=0dB)	69.4	69.5
S/N	A-weighted	91.1	91.1

DAC (HP(Pseudo Cap-less Mode)) characteristics (DAC-->HP(Pseudo Cap-less Mode)), R_L=16Ω

Parameter		Lch [dB]	Rch [dB]
S/(N+D)	20kHzLPF (–3dB) (HPG=0dB)	64.7	65.0
S/N	A-weighted	90.1	90.1

DAC (SP(Stereo)) characteristics (DAC-->SP(Stereo)), R_L=8Ω

Parameter		Lch [dB]	Rch [dB]
S/(N+D)	20kHzLPF (-0.5dBFS) (SPKG2-0:+4.43dB)	61.5	61.6
S/N	A-weighted	90.4	90.3

DAC (SP(High Power Mode)) characteristics (DAC-->SP(High Power Mode)), R_L=8Ω

Parameter		[dB]
S/(N+D)	20kHzLPF (-0.5dBFS) (SPKG2-0:+4.43dB)	61.5
S/N	A-weighted	91.4

2. PLOT DATA

2-1 ADC (LIN2/RIN2 → ADC)(MIC-Amp Gain:+20dB)

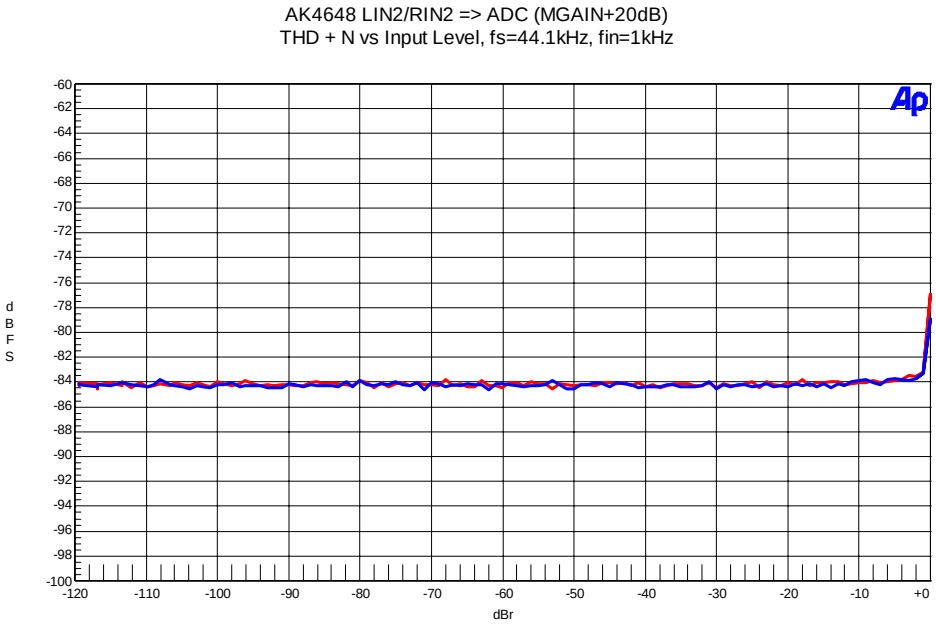


Figure 14. THD+N vs. Input Level

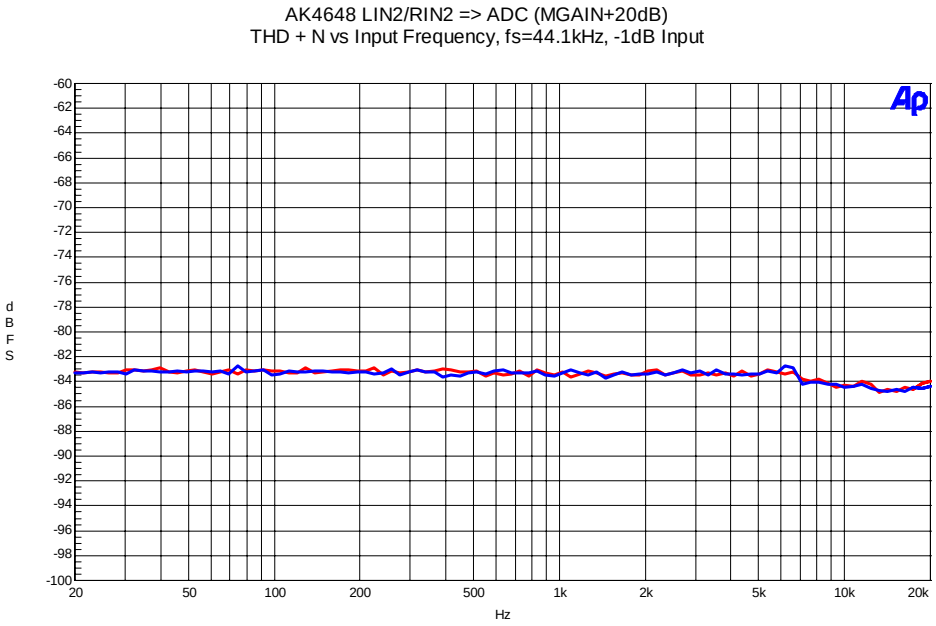


Figure 15. THD+N vs. Input Frequency

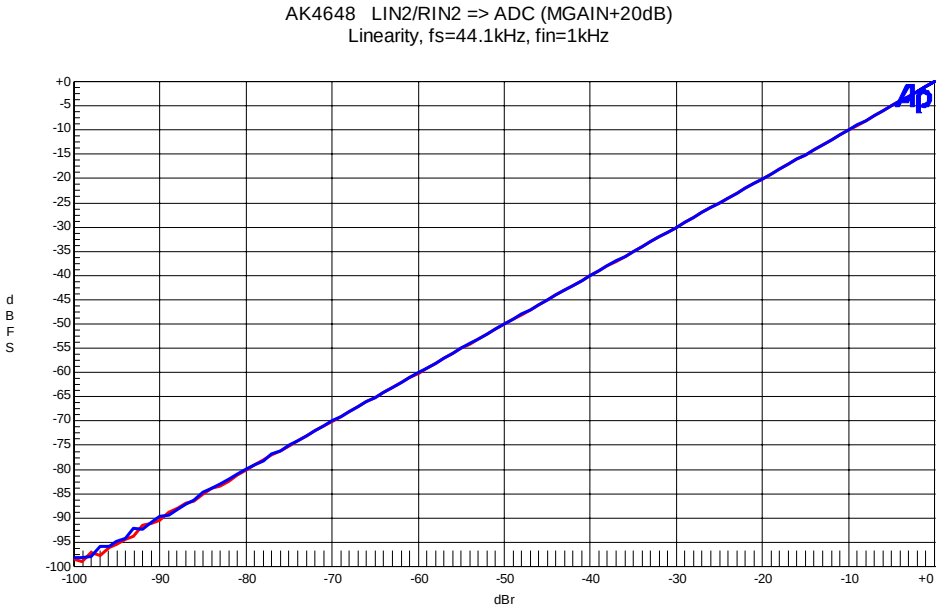


Figure 16. Linearity

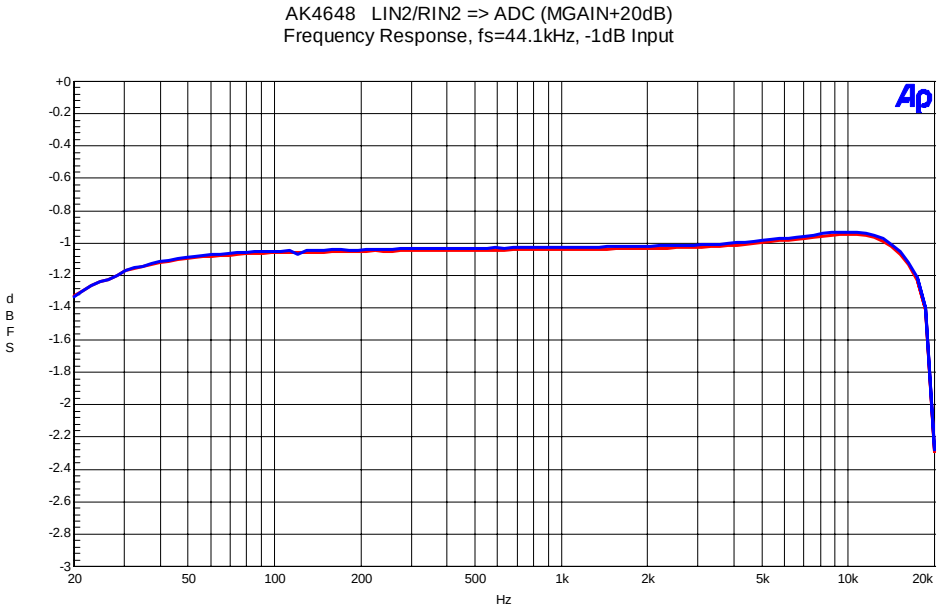


Figure 17. Frequency Response

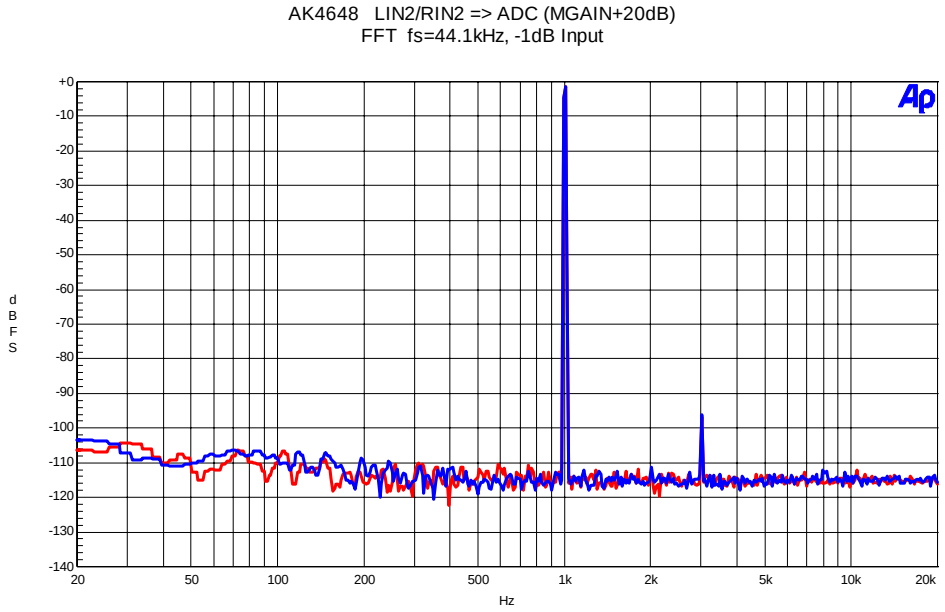


Figure 18. FFT Plot (Input level= -1dBFS)

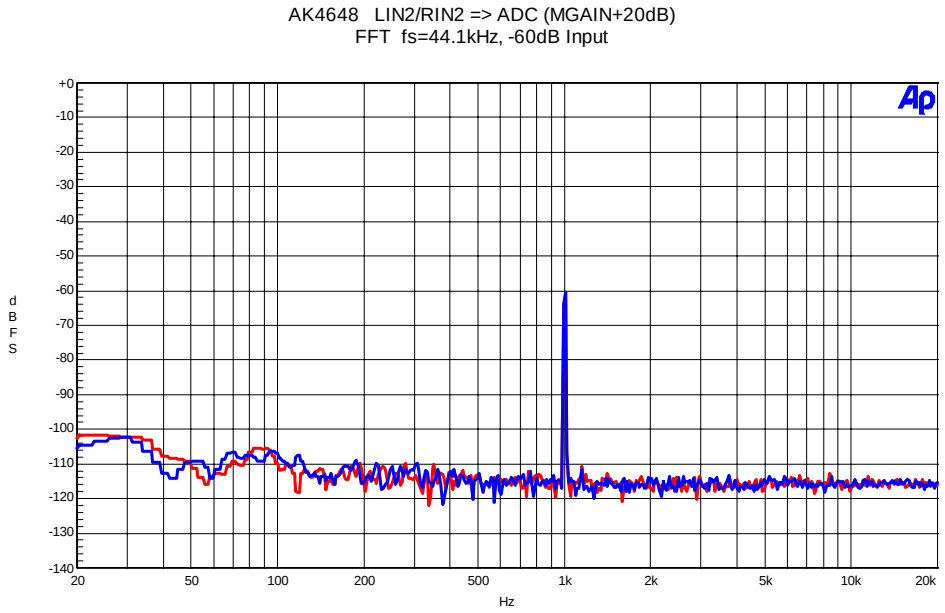


Figure 19. FFT Plot (Input level= -60dBFS)

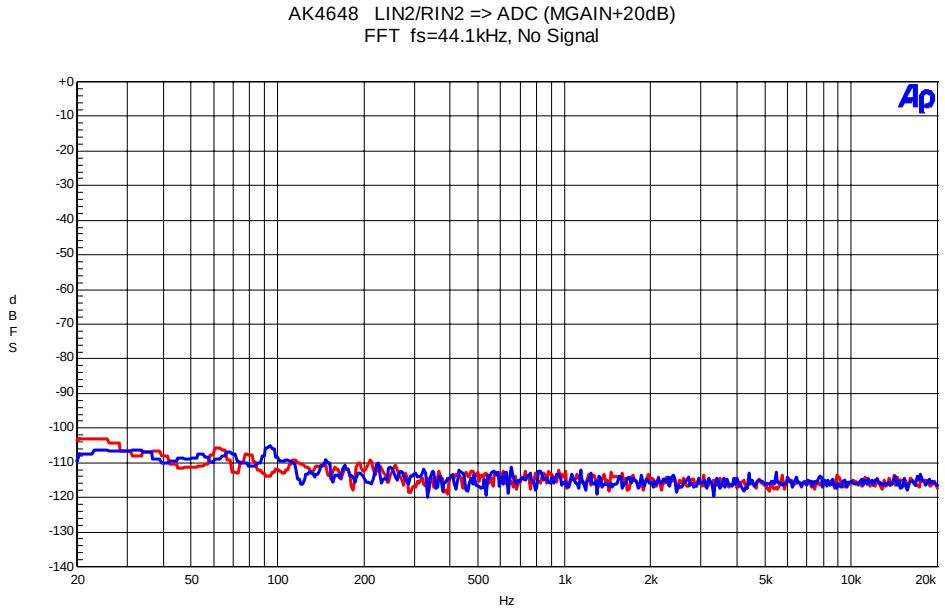


Figure 20. FFT Plot (No signal)

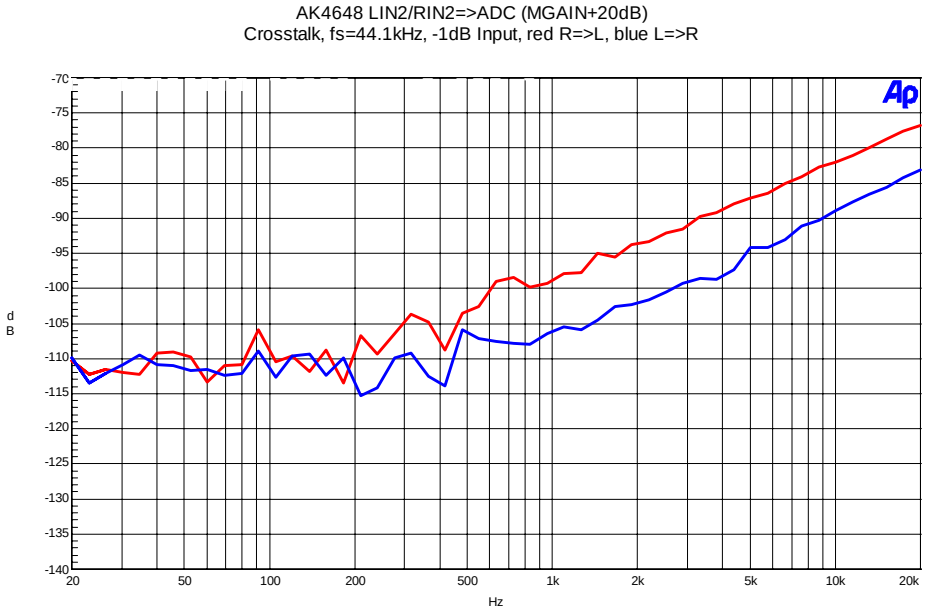


Figure 21. Crosstalk Plot

2-2 ADC (LIN2/RIN2 → ADC)(MIC-Amp Gain:0dB)

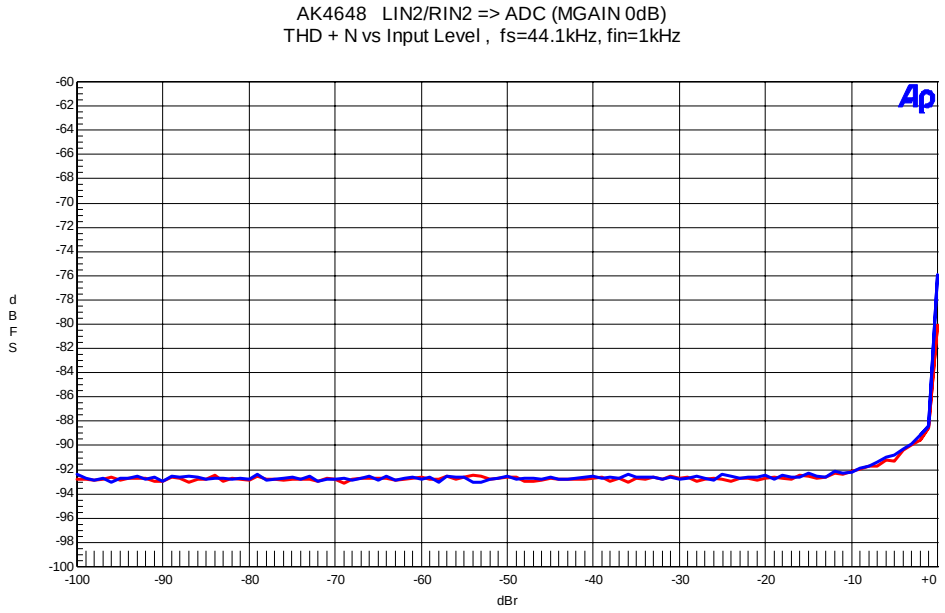


Figure 22. THD+N vs. Input Level

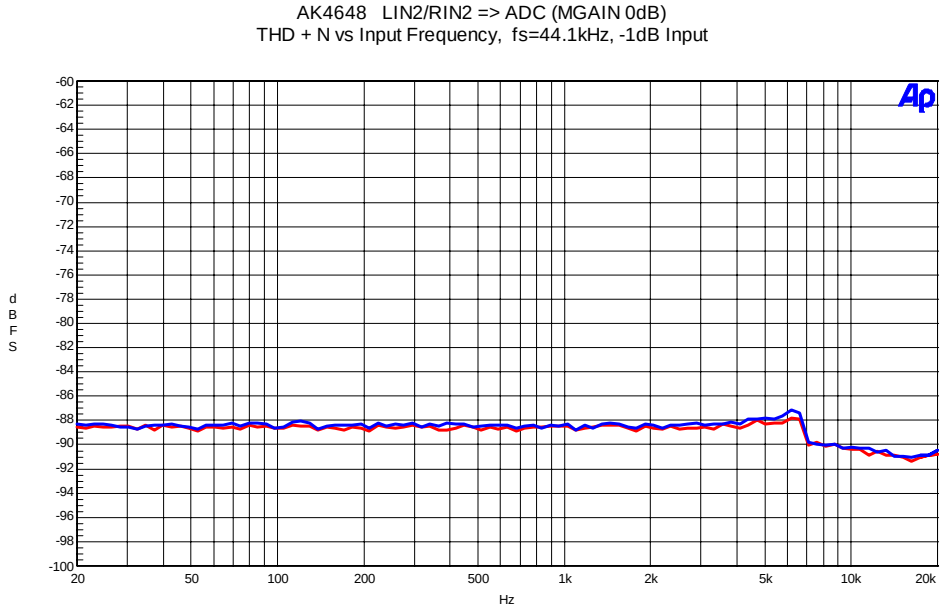


Figure 23. THD+N vs. Input Frequency

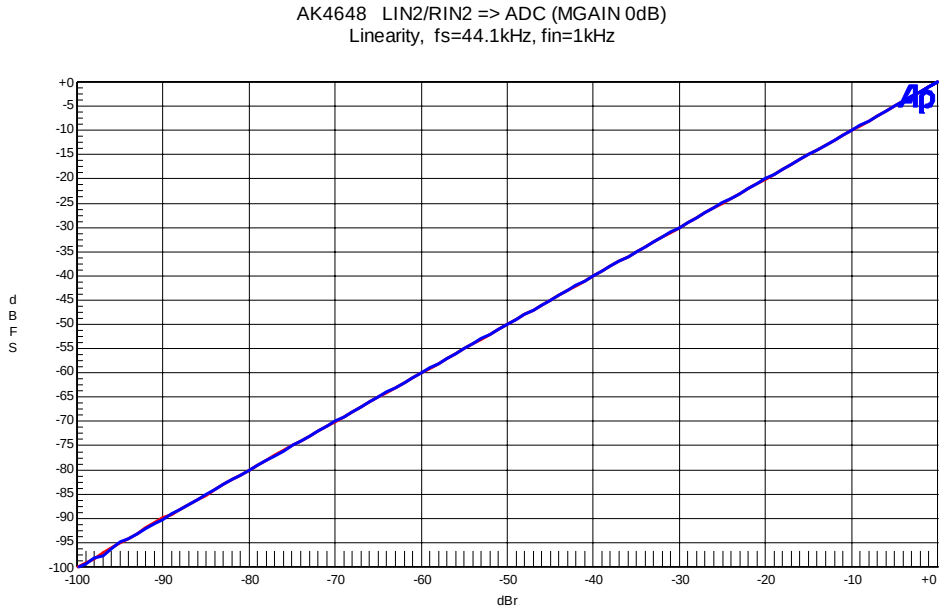


Figure 24. Linearity

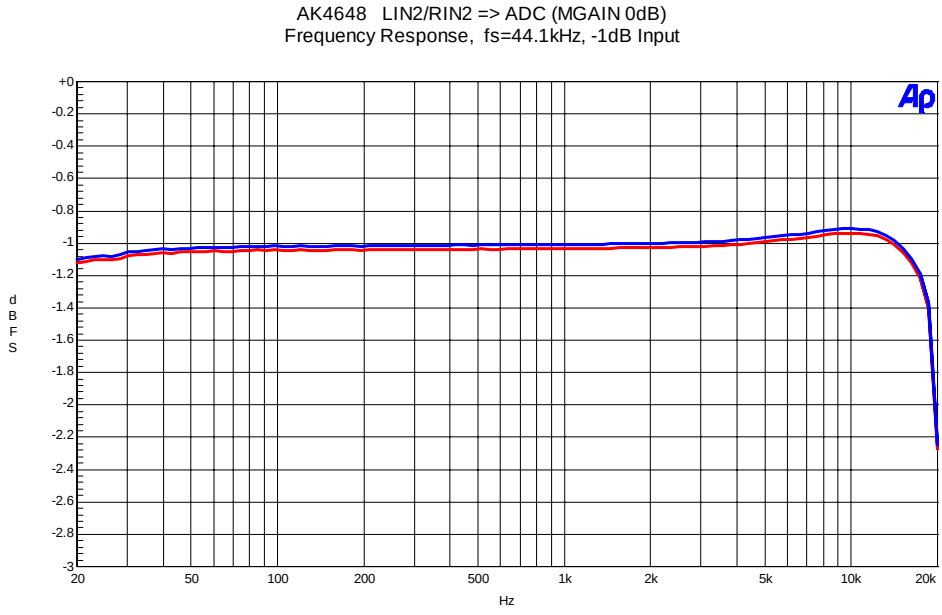


Figure 25. Frequency Response

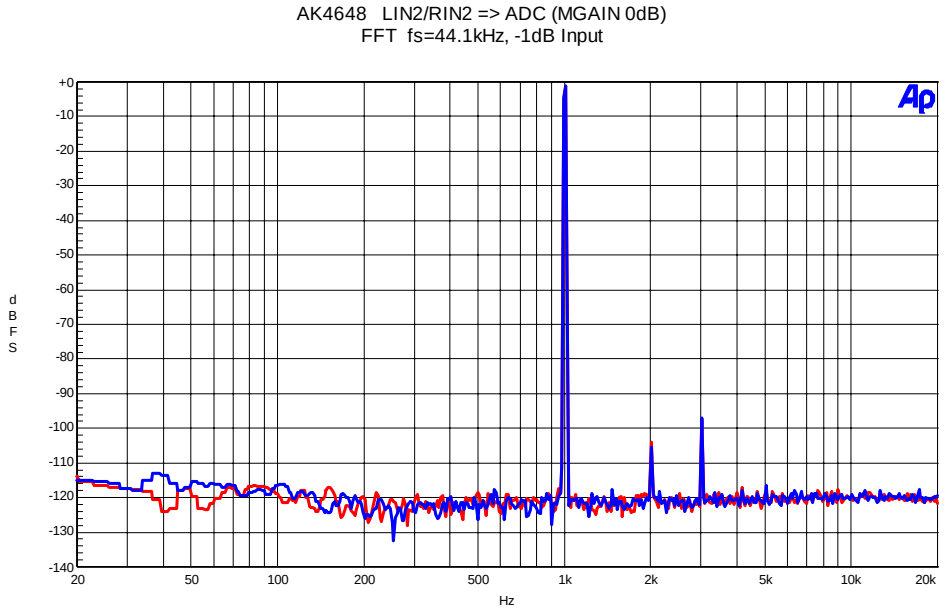


Figure 26. FFT Plot (Input level= -1dBFS)

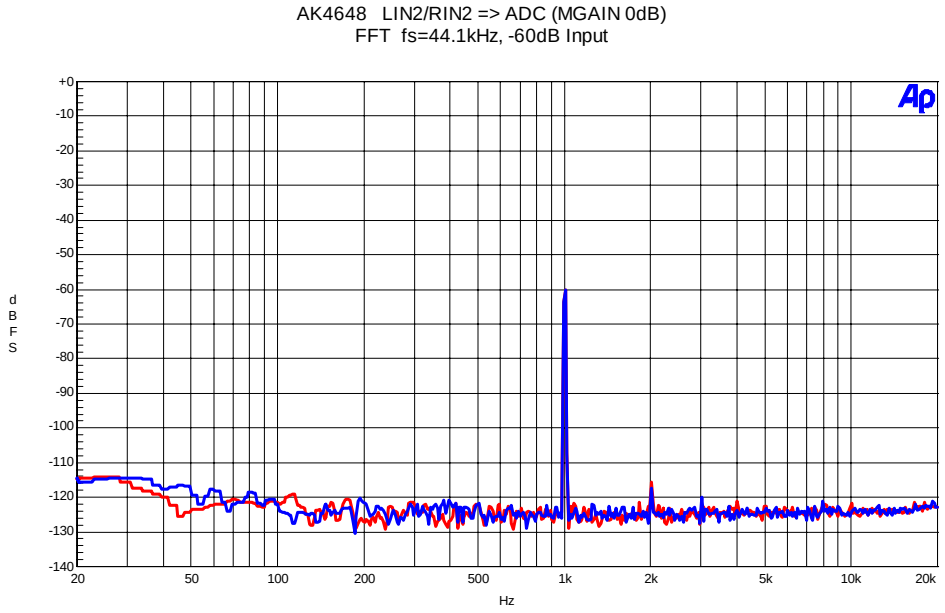


Figure 27. FFT Plot (Input level = -60dBFS)

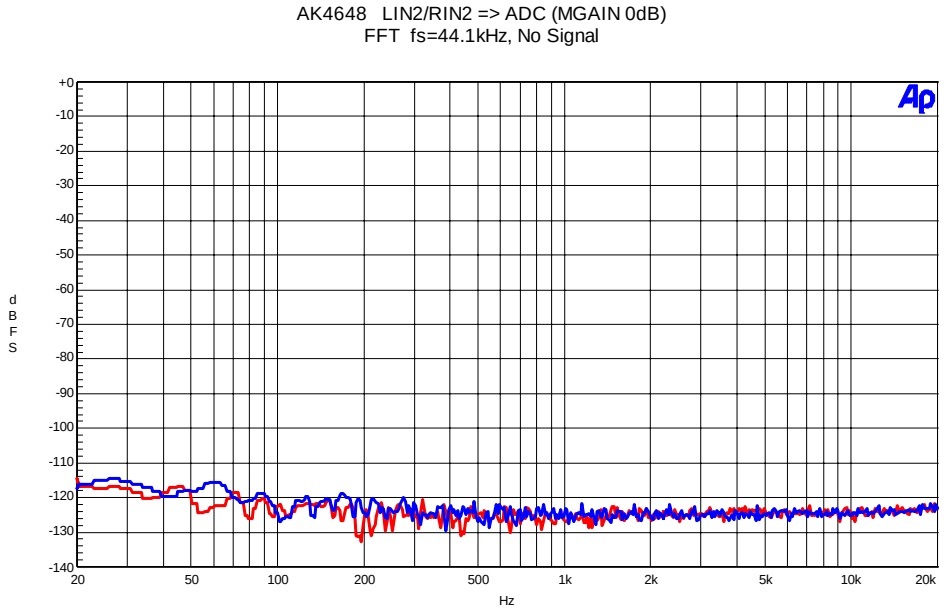


Figure 28. FFT Plot (No signal)

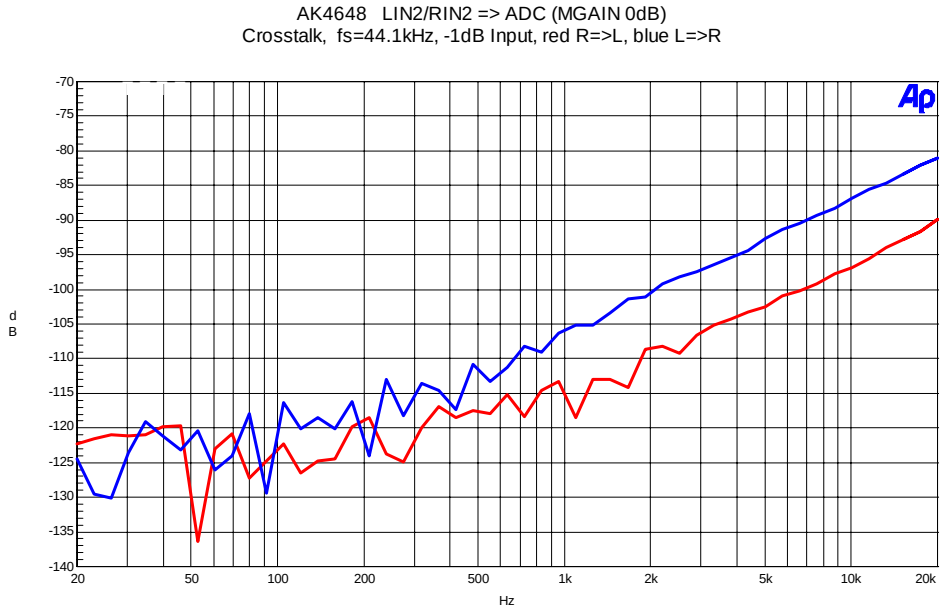


Figure 29. Crosstalk Plot

2-3 DAC (DAC→ LOUT/ROUT)

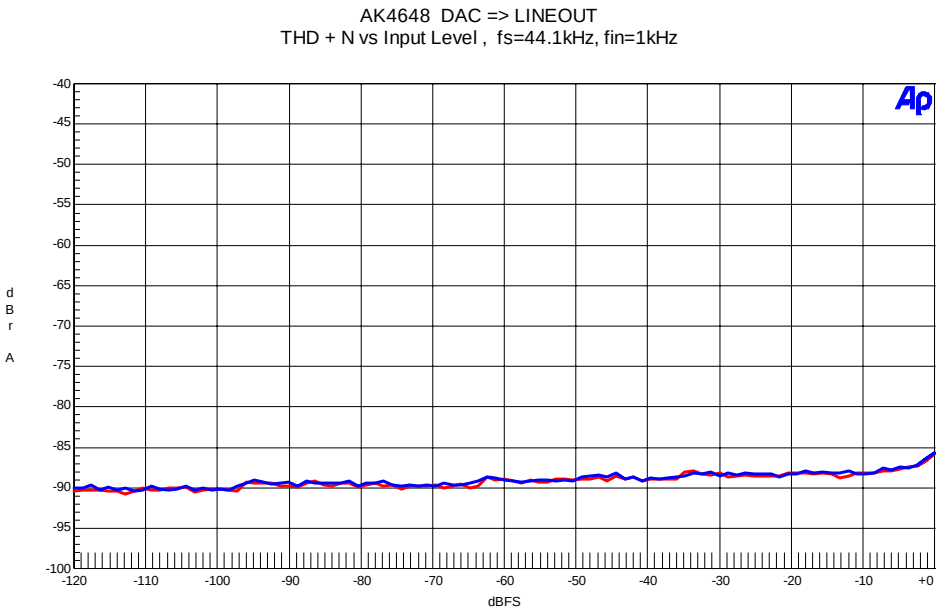


Figure 30. THD+N vs. Input Level

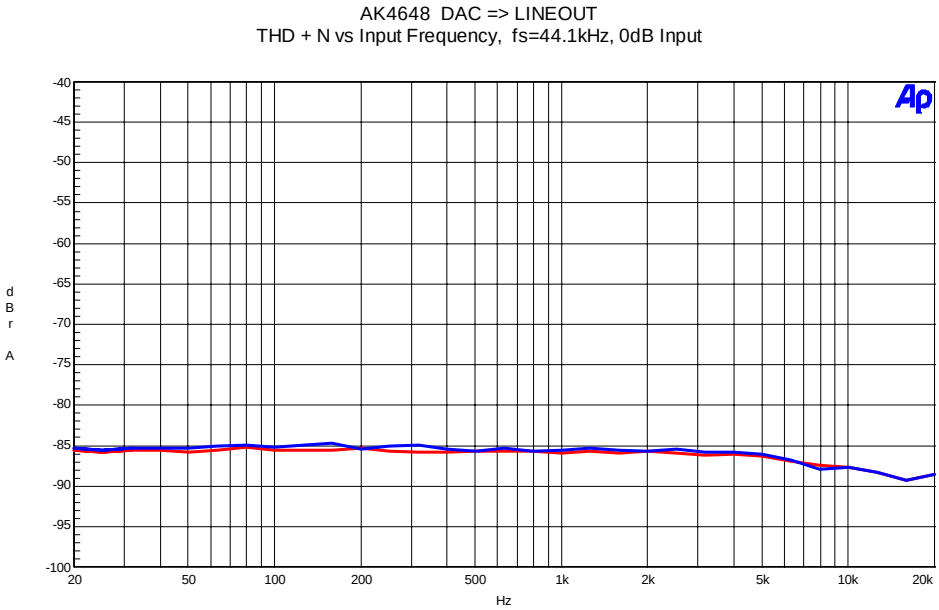


Figure 31. THD+N vs. Input Frequency

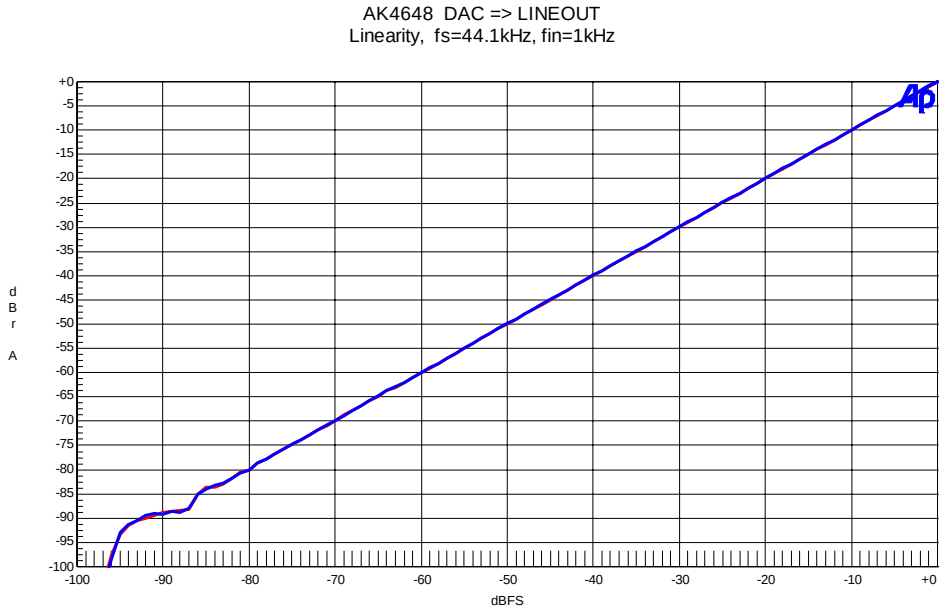


Figure 32. Linearity

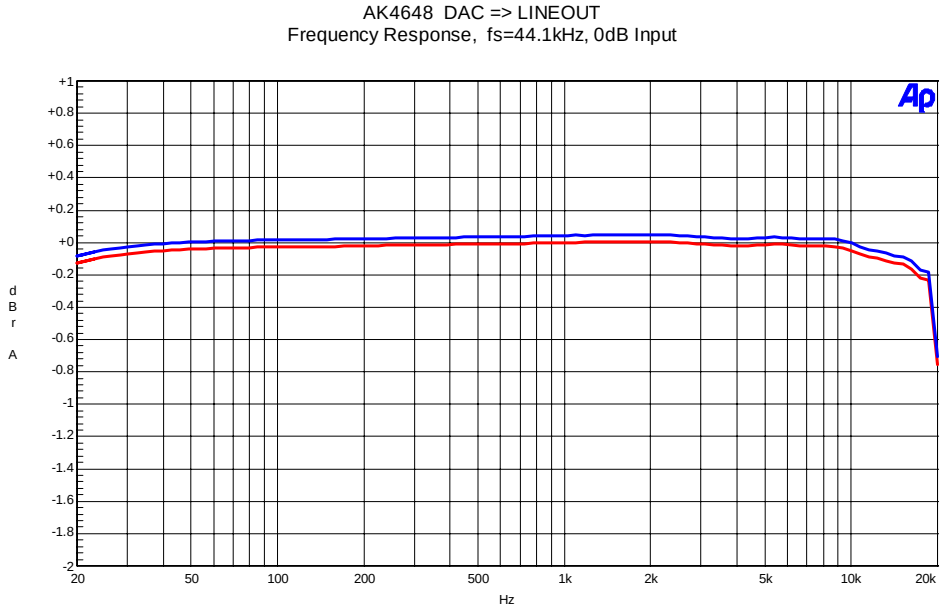


Figure 33. Frequency Response

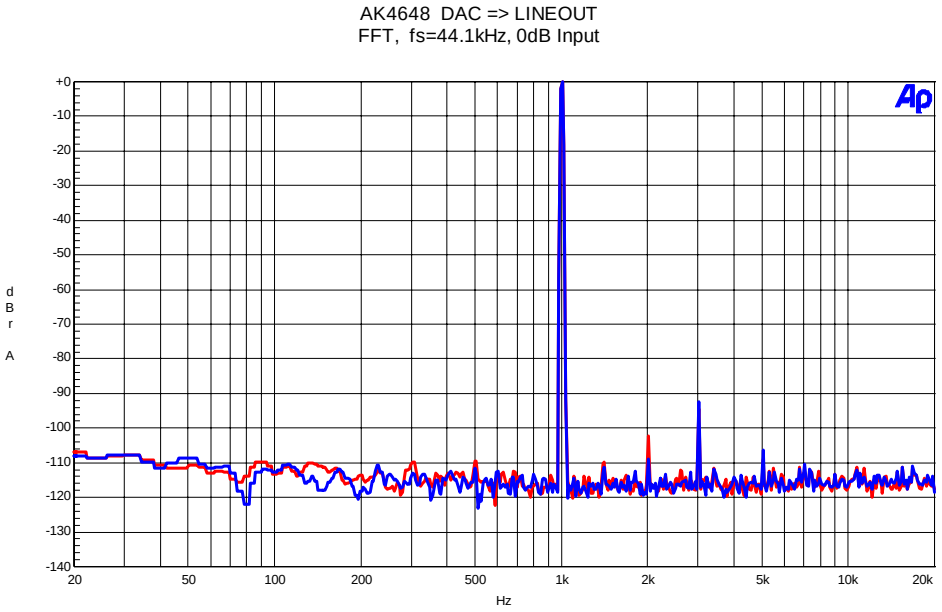


Figure 34. FFT Plot (Input level= 0dBFS)

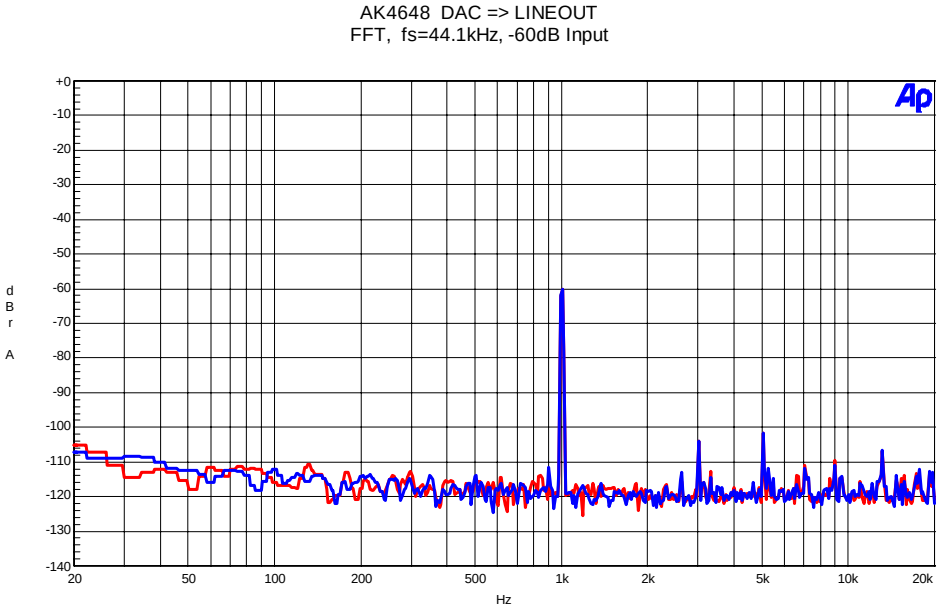


Figure 35. FFT Plot (Input level = -60dBFS)

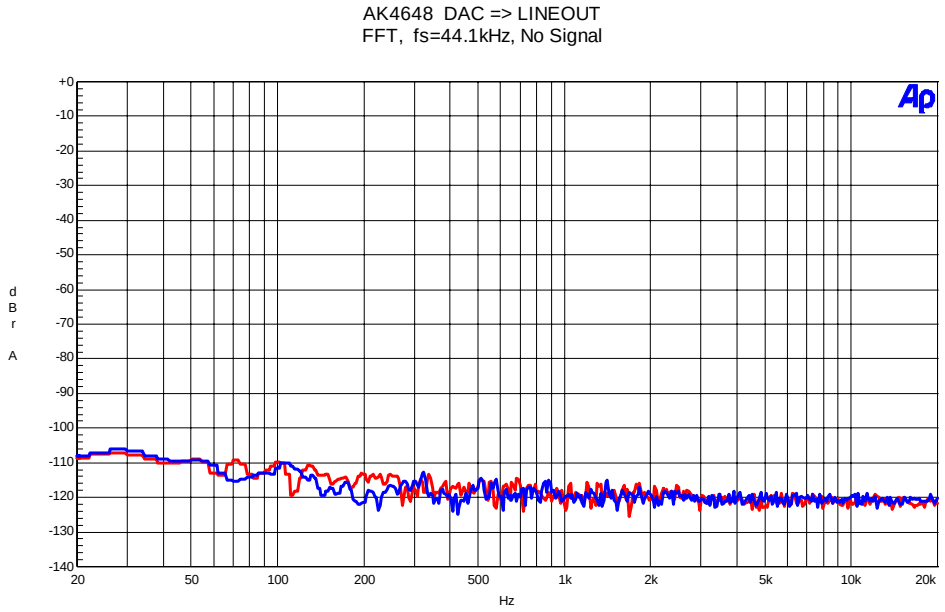


Figure 36. FFT Plot (No signal)

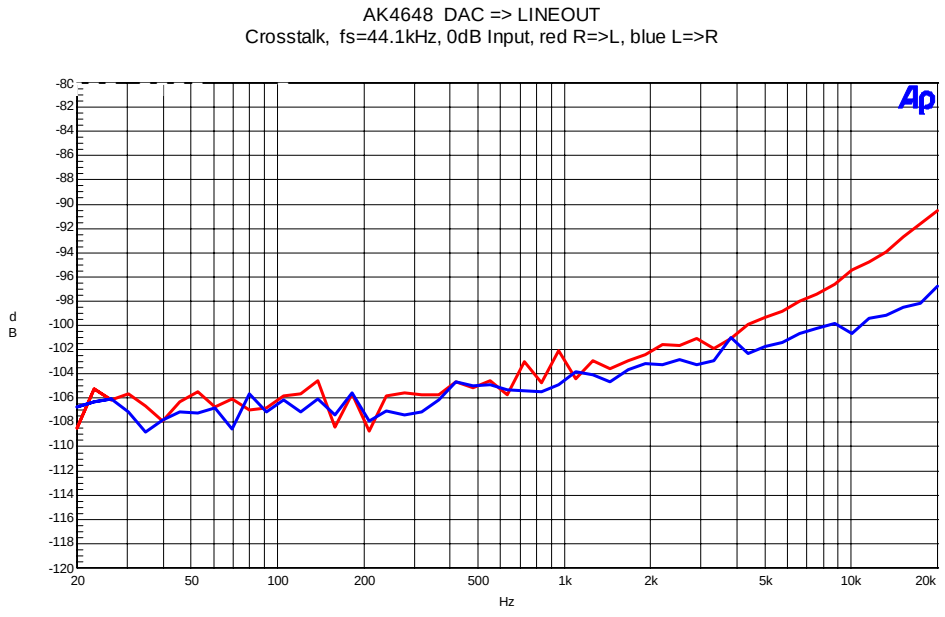


Figure 37. Crosstalk Plot

2-4 DAC (DAC→HP(Single-ended Mode))(HPG=0dB)

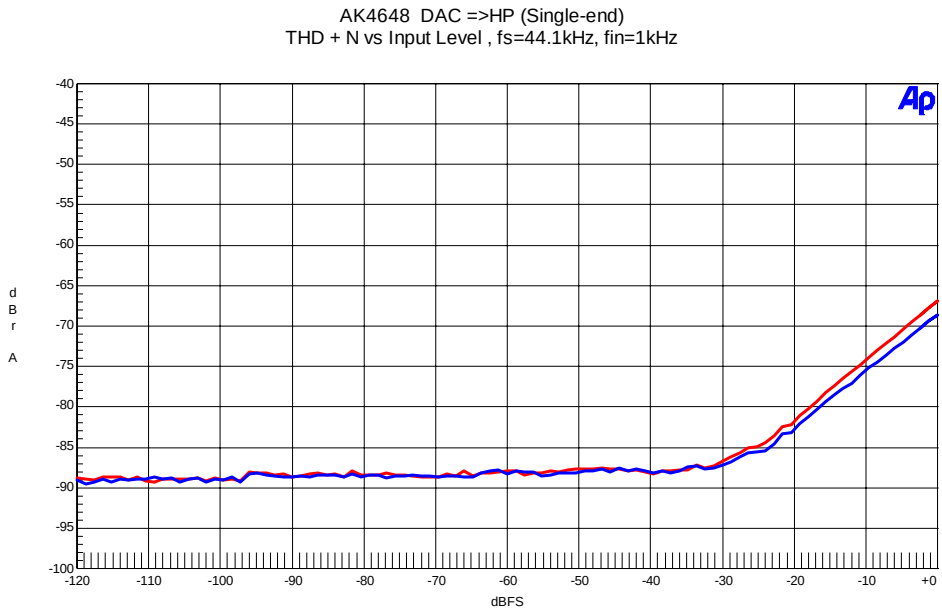


Figure 38. THD+N vs. Input Level

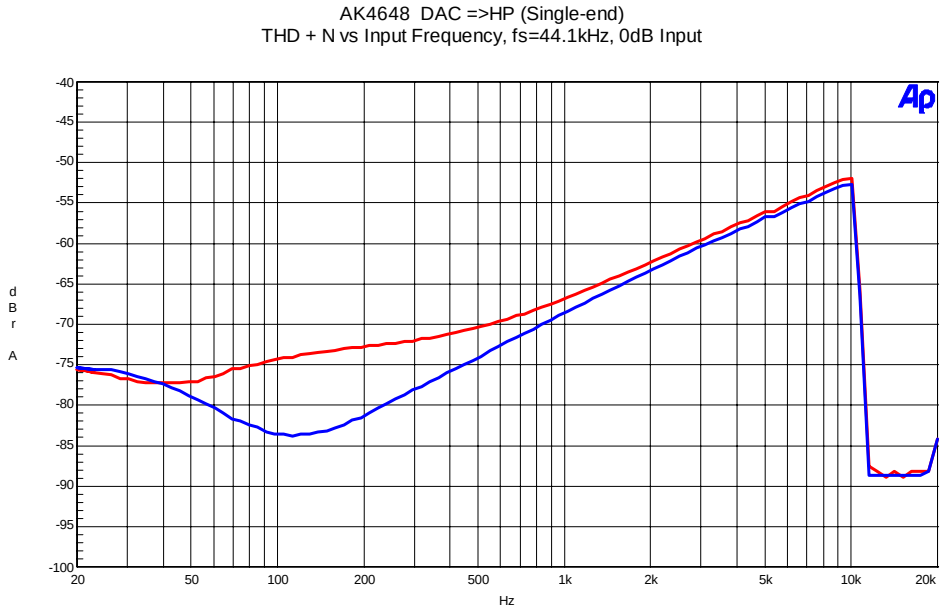


Figure 39. THD+N vs. Input Frequency

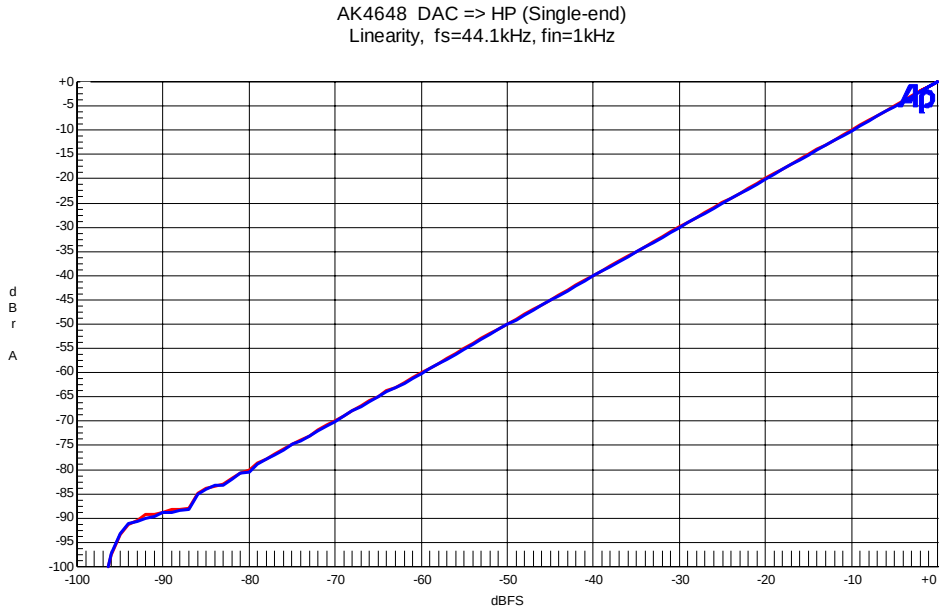


Figure 40. Linearity

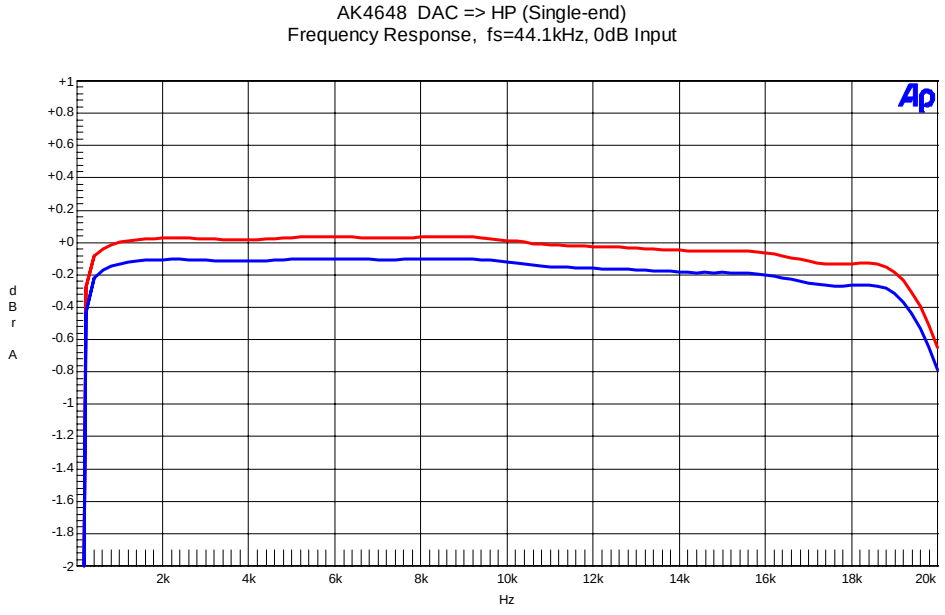


Figure 41. Frequency Response

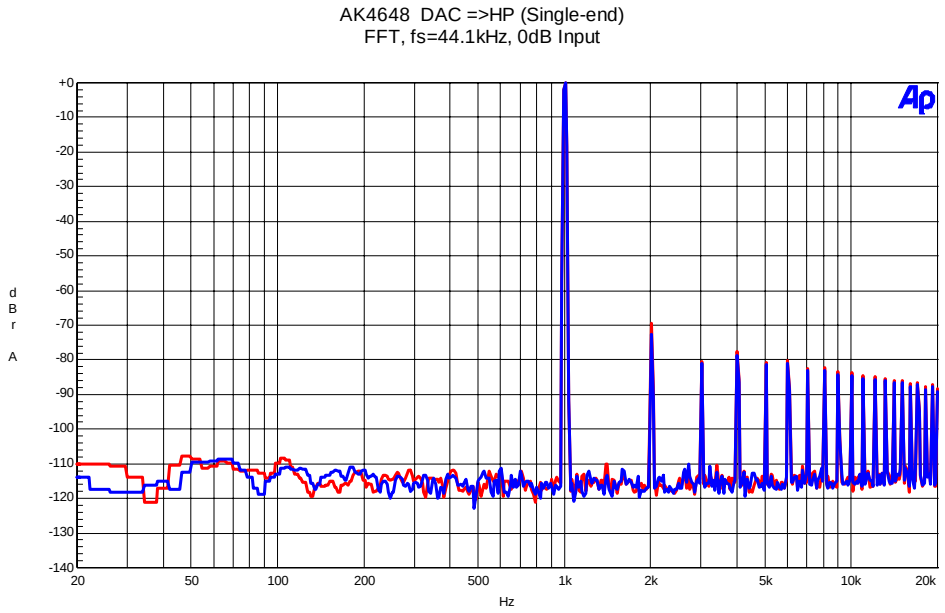


Figure 42. FFT Plot (Input level= 0dBFS)

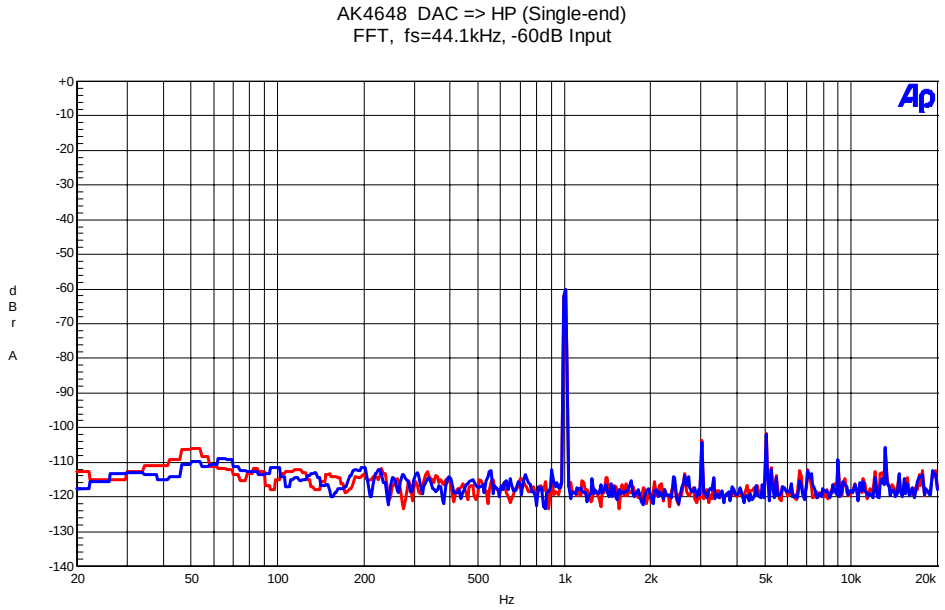


Figure 43. FFT Plot (Input level = -60dBFS)

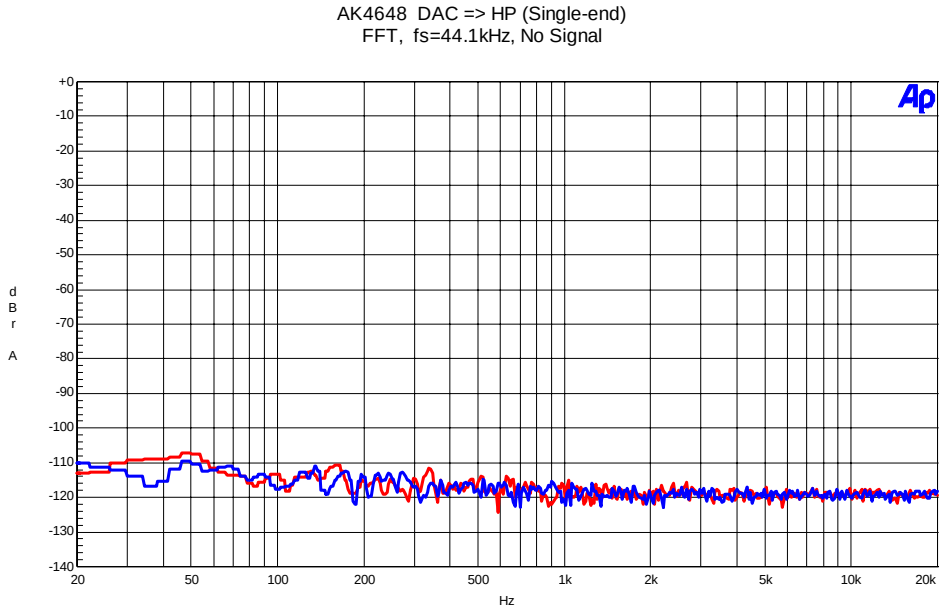


Figure 44. FFT Plot (No signal)

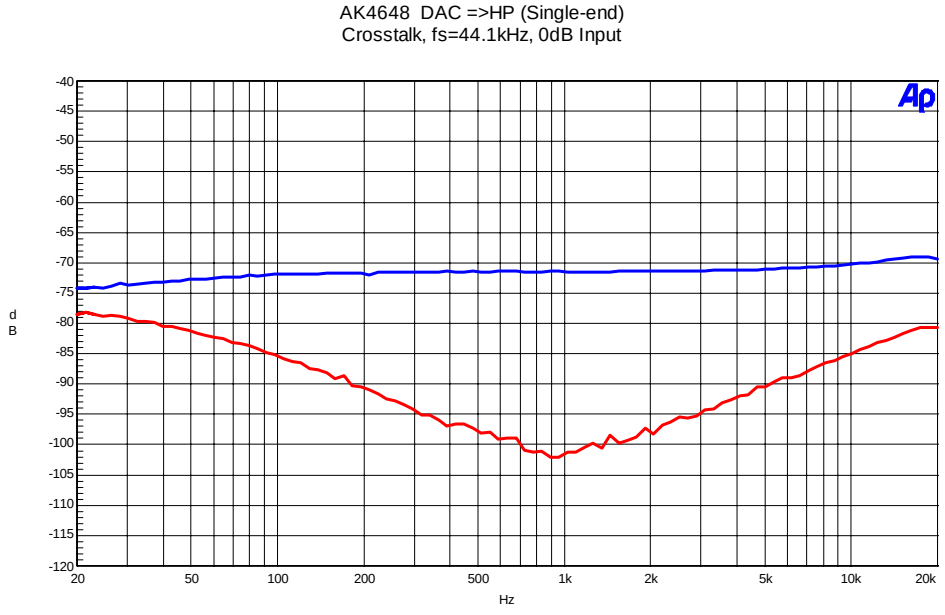


Figure 45. Crosstalk Plot

2-5 DAC (DAC→HP(Pseudo Cap-less Mode))(HPG=0dB)

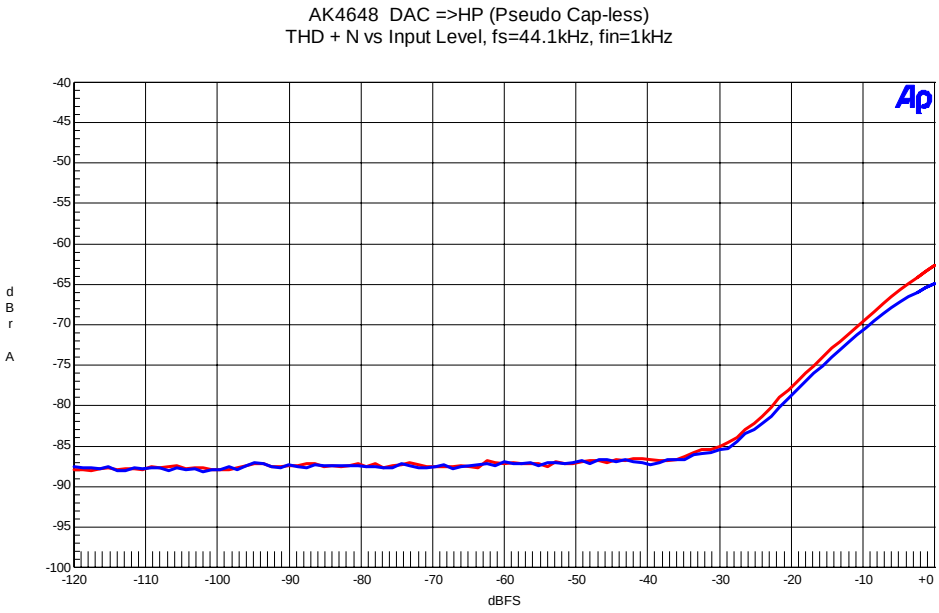


Figure 46. THD+N vs. Input Level

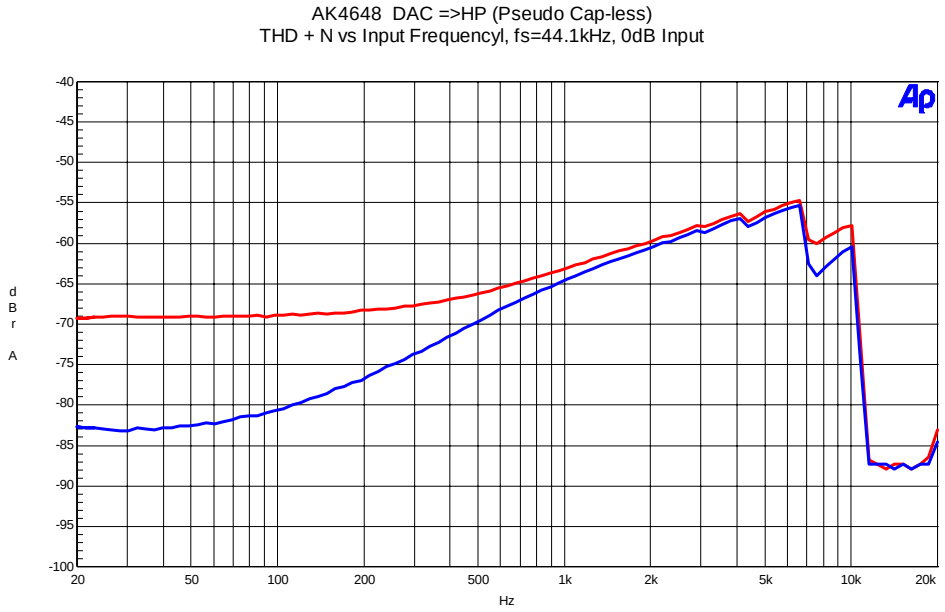


Figure 47. THD+N vs. Input Frequency (Non invert signal input)

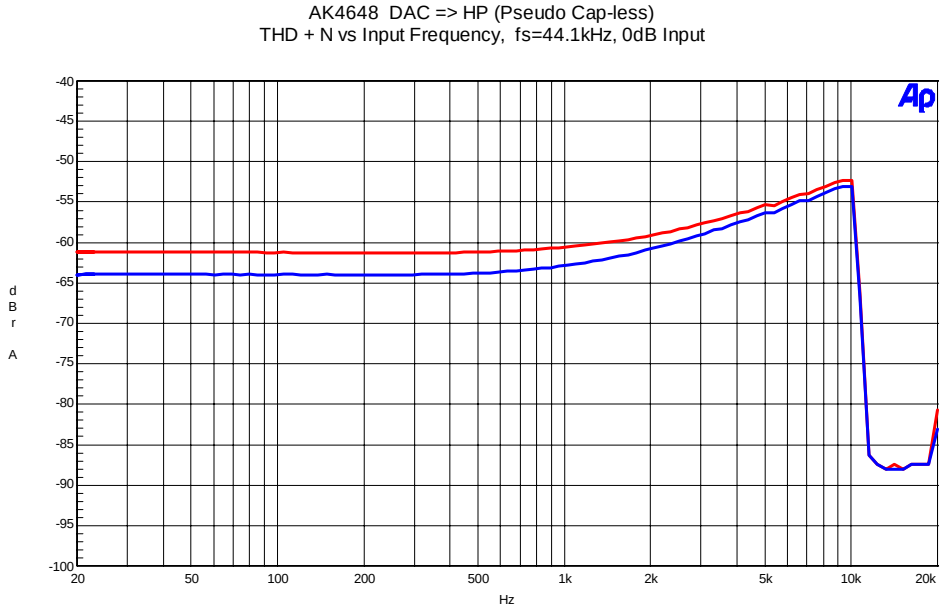


Figure 48. THD+N vs. Input Frequency (Invert signal input)

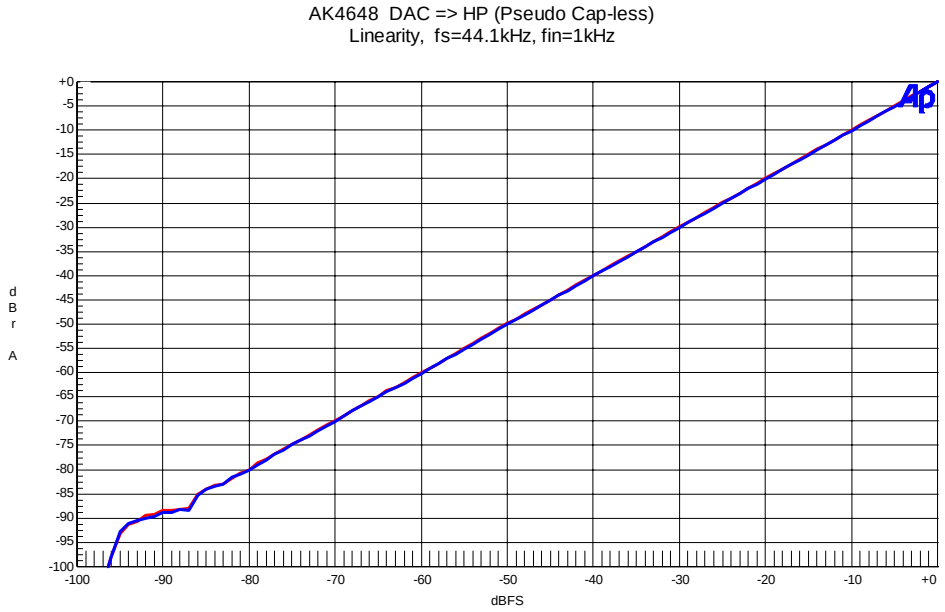


Figure 49. Linearity

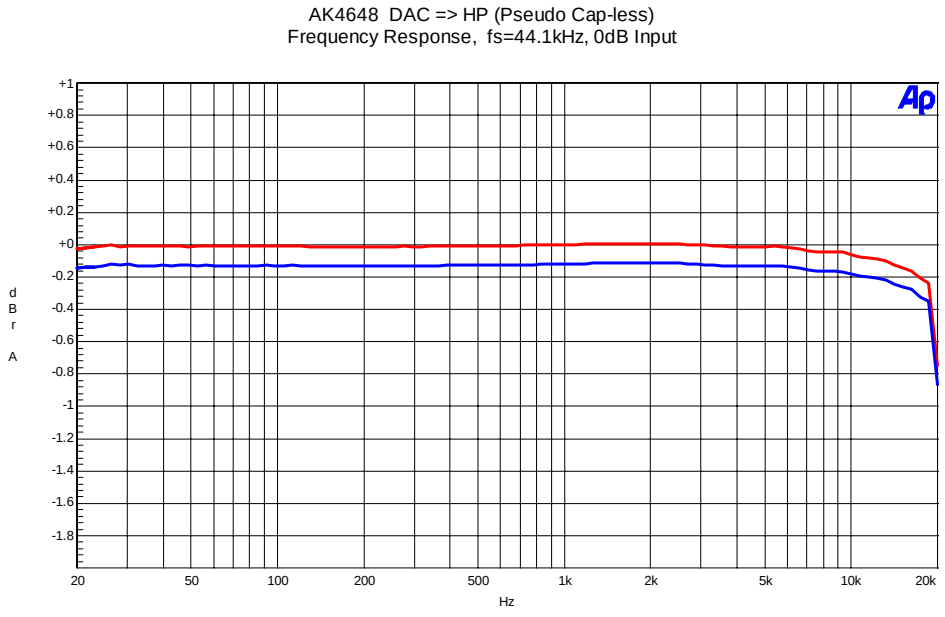


Figure 50. Frequency Response

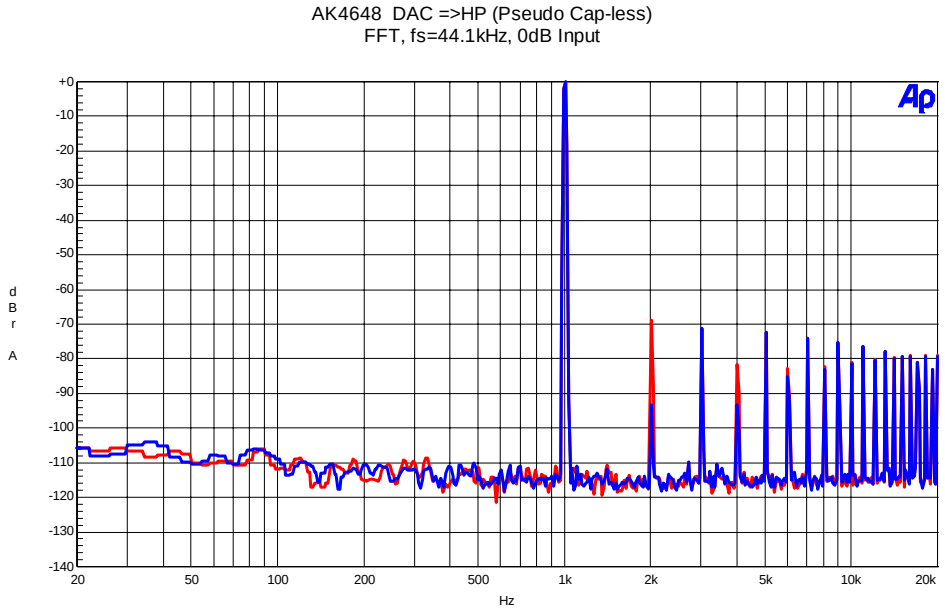


Figure 51. FFT Plot (Input level= 0dBFS)

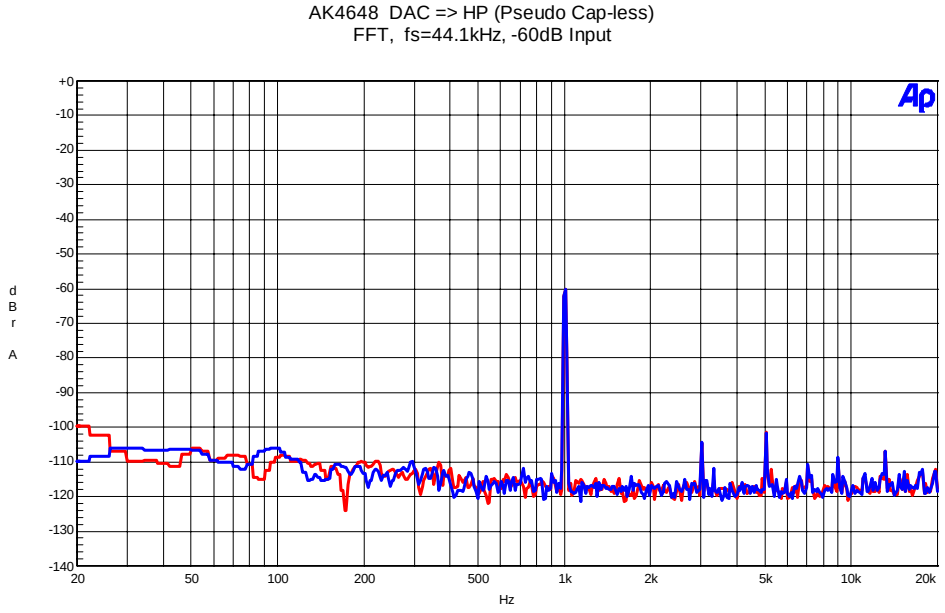


Figure 52. FFT Plot (Input level = -60dBFS)

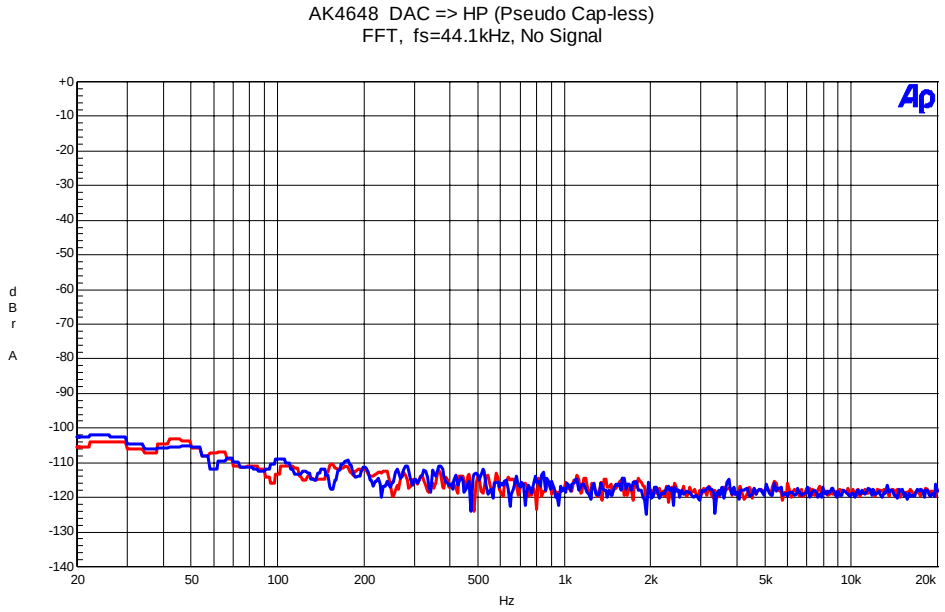


Figure 53. FFT Plot (No signal)

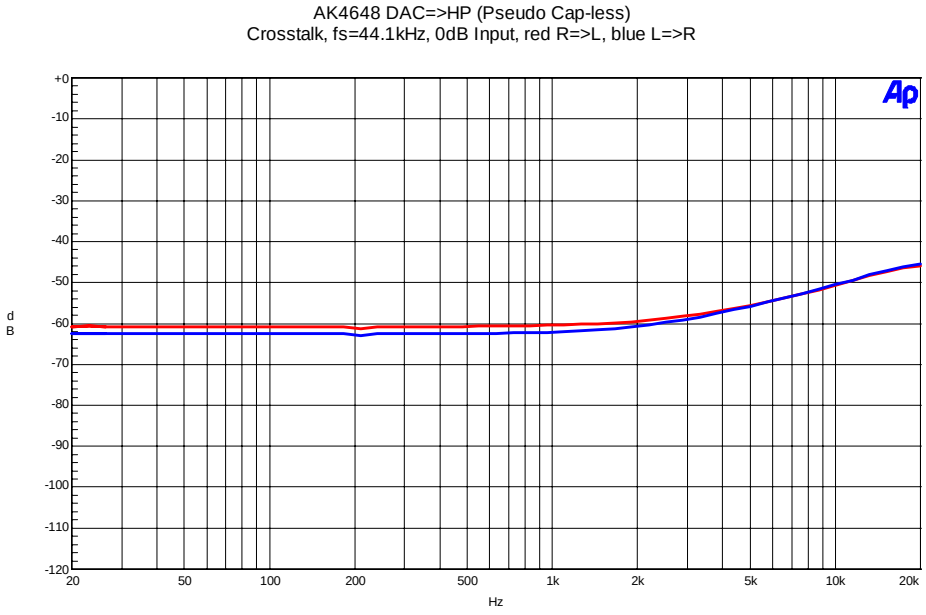


Figure 54. Crosstalk Plot

2-6 DAC (DAC-->SP(Stereo))(SPKG2-0:+4.43dB)

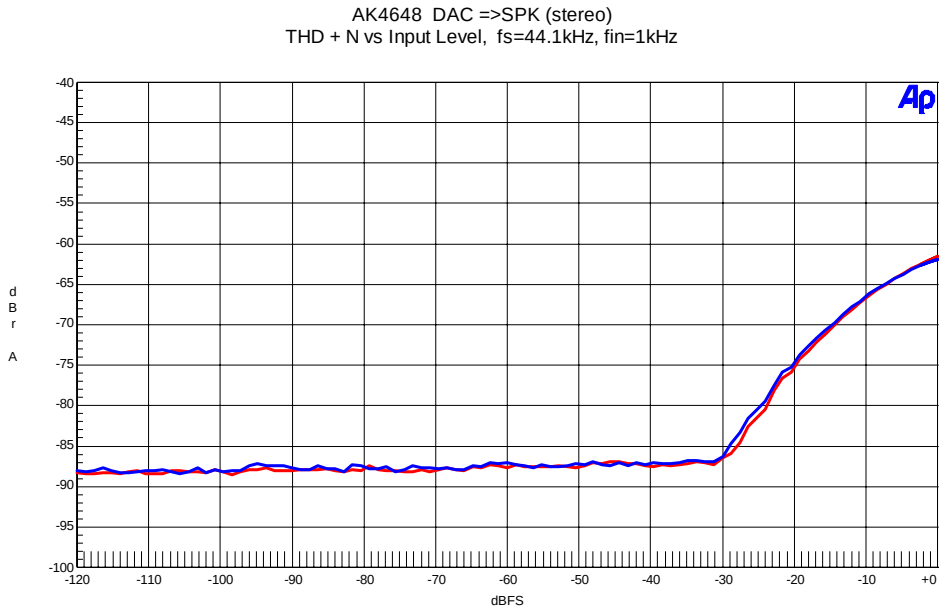


Figure 55. THD+N vs. Input Level

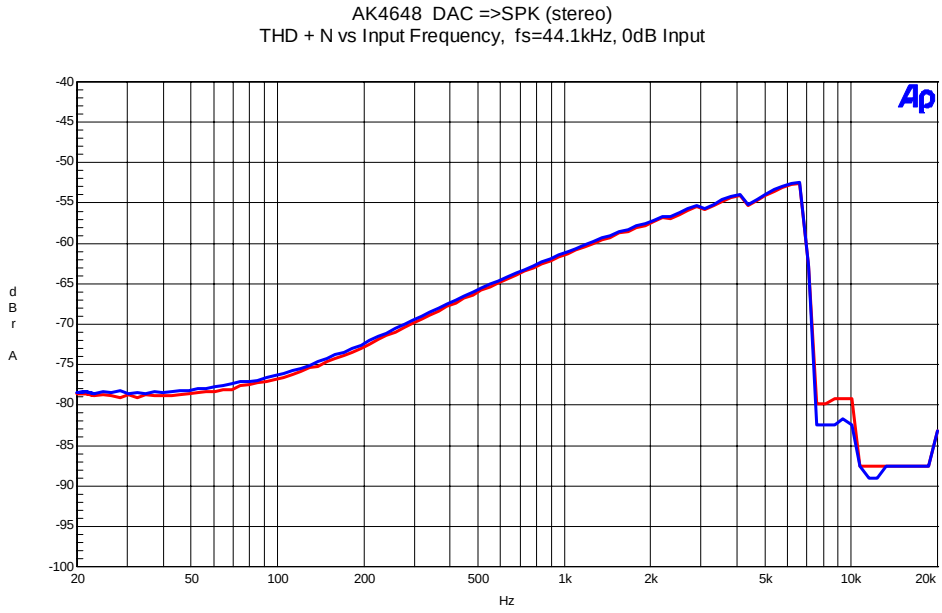


Figure 56. THD+N vs. Input Frequency

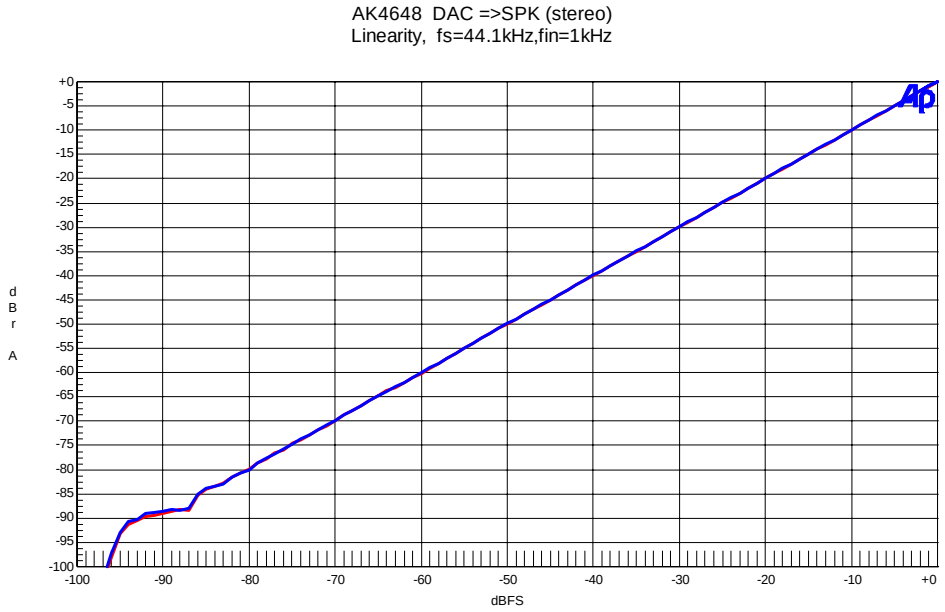


Figure 57. Linearity

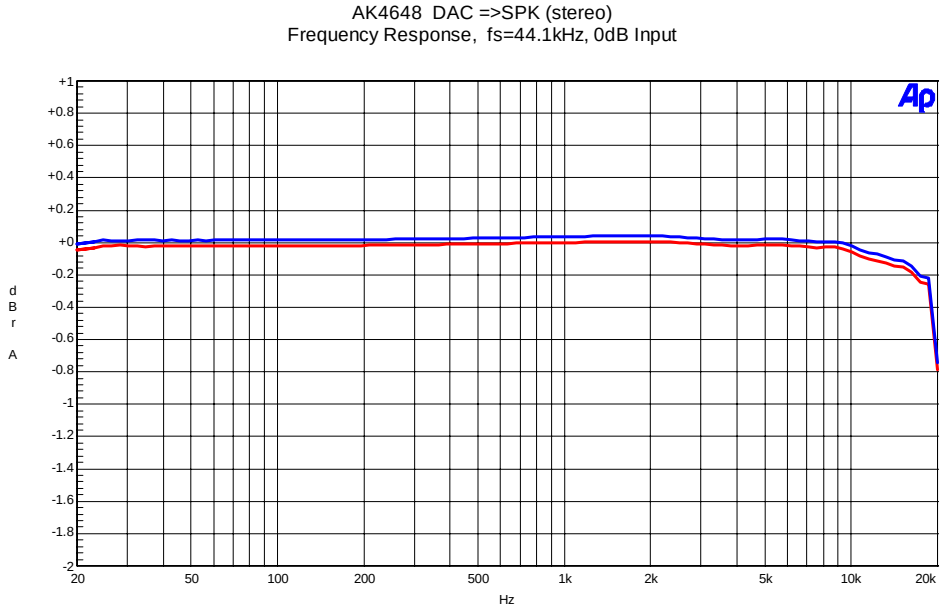


Figure 58. Frequency Response

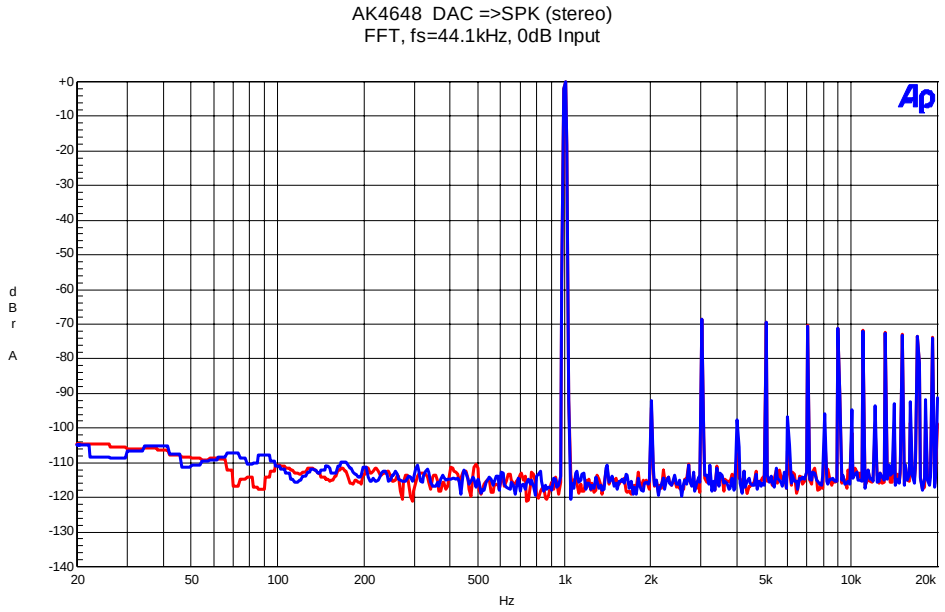


Figure 59. FFT Plot (Input level= 0dBFS)

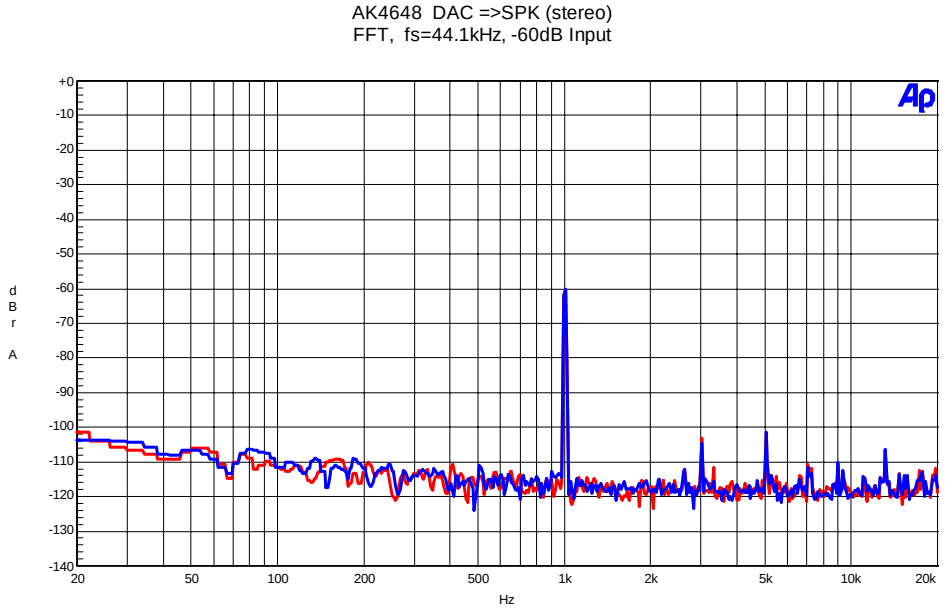


Figure 60. FFT Plot (Input level = -60dBFS)

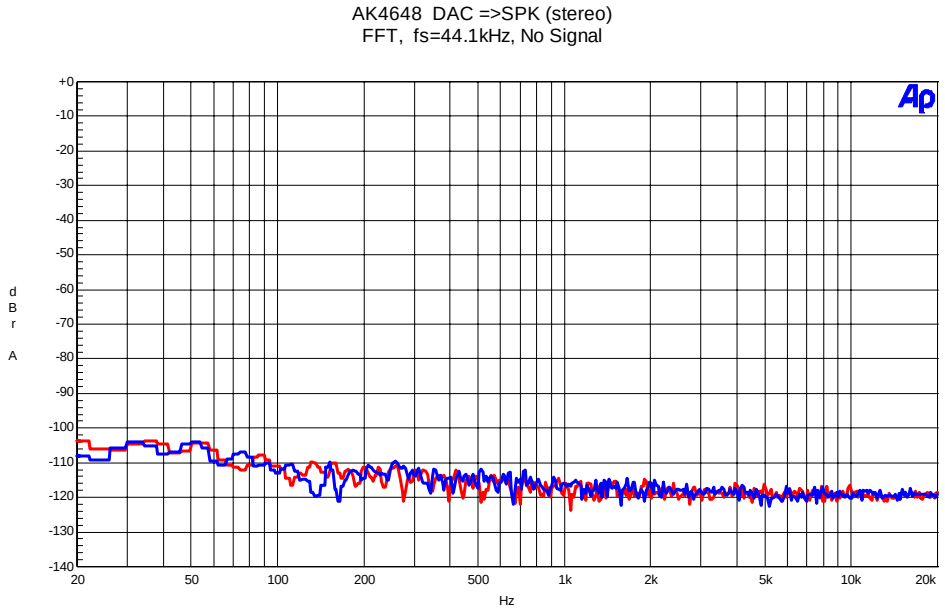


Figure 61. FFT Plot (No signal)

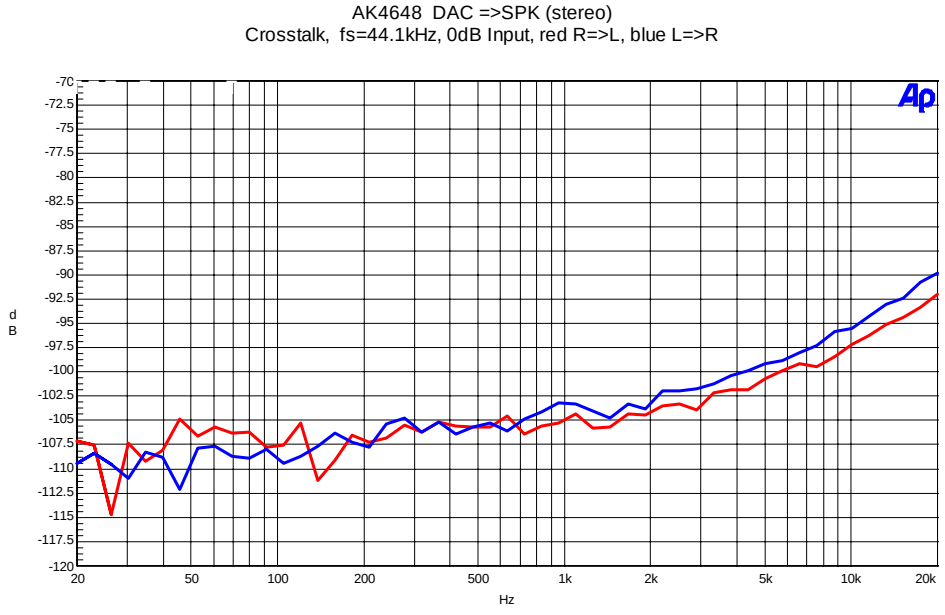


Figure 62. Crosstalk Plot

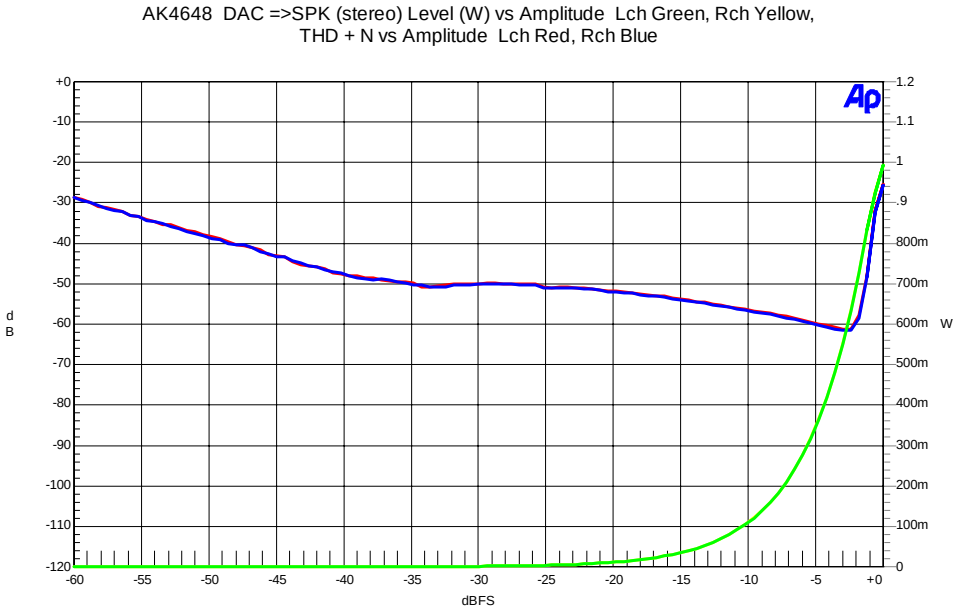


Figure 63. THD+N & Output Power vs. Input Level (SPKG=+12.65dB)

2-7 DAC (DAC-->SP(High Power Mode))(SPKG2-0:+4.43dB)

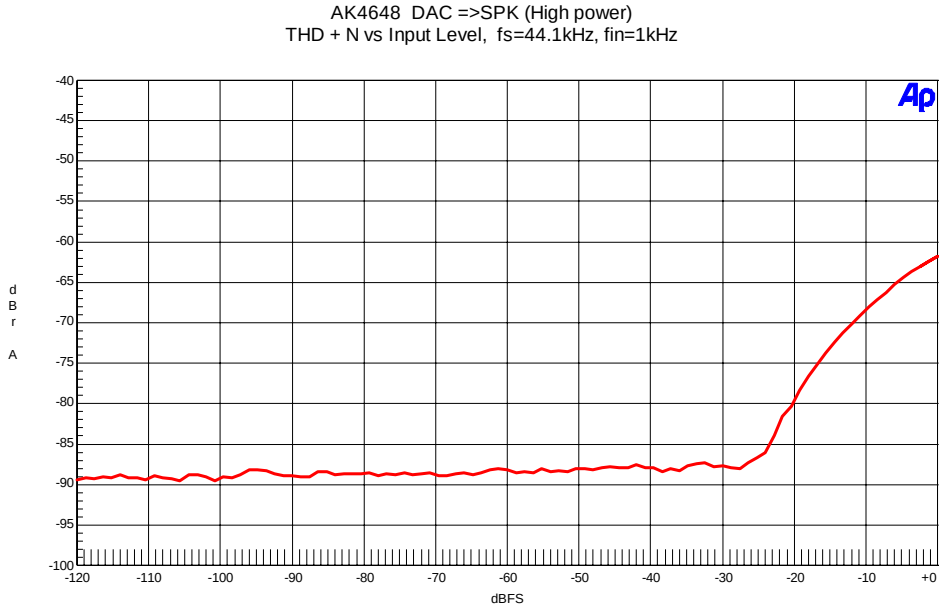


Figure 66. THD+N vs. Input Level

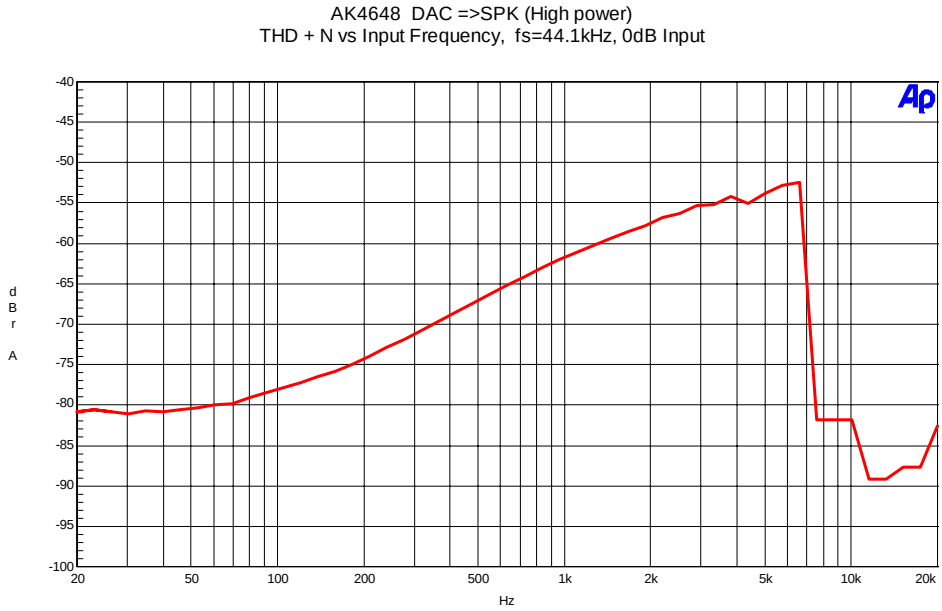


Figure 67. THD+N vs. Input Frequency

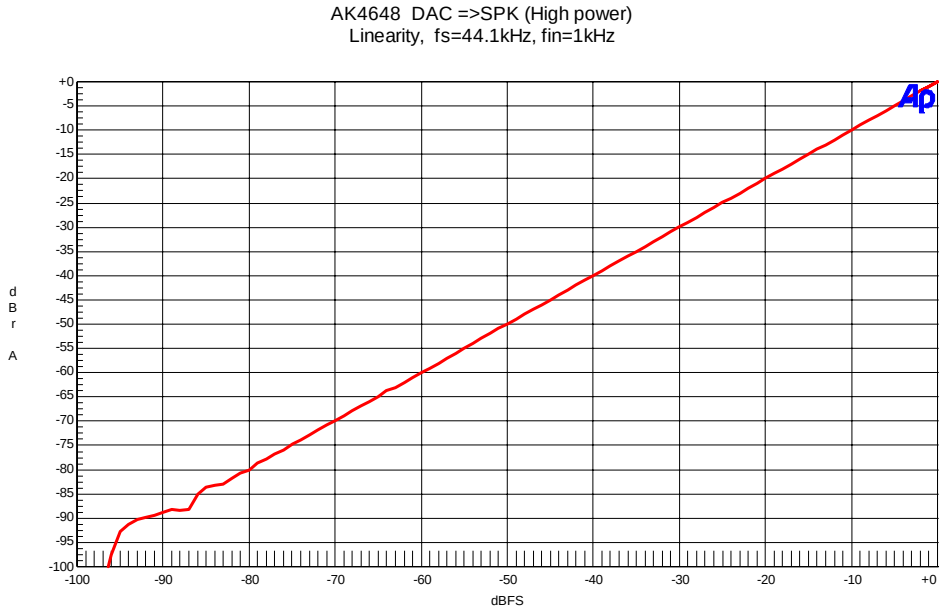


Figure 68. Linearity

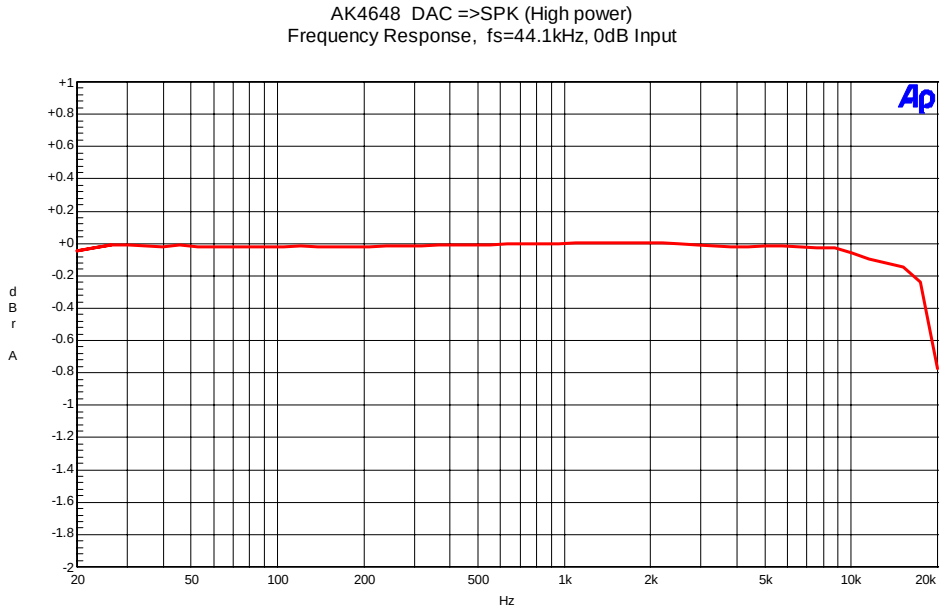


Figure 69. Frequency Response

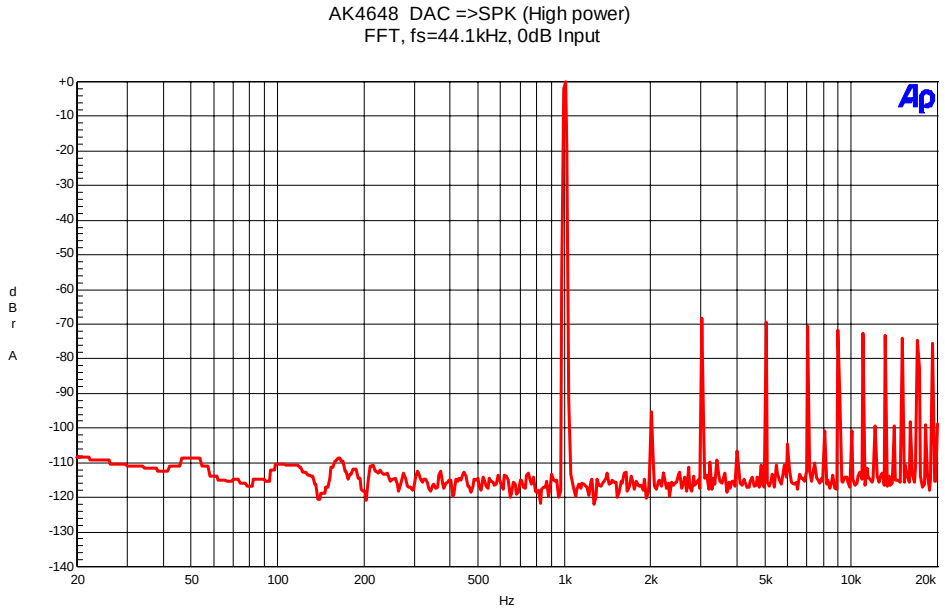


Figure 70. FFT Plot (Input level= 0dBFS)

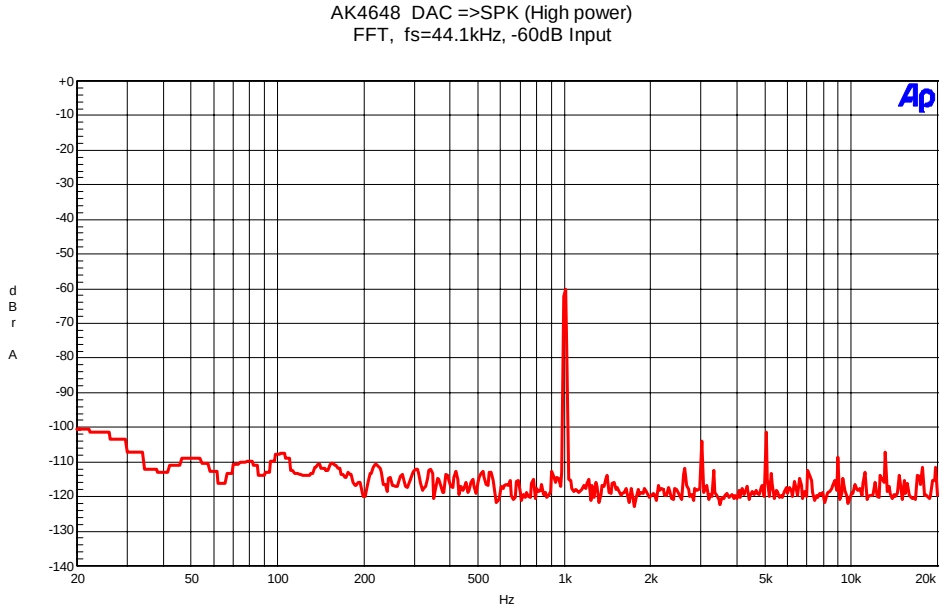


Figure 71. FFT Plot (Input level = -60dBFS)

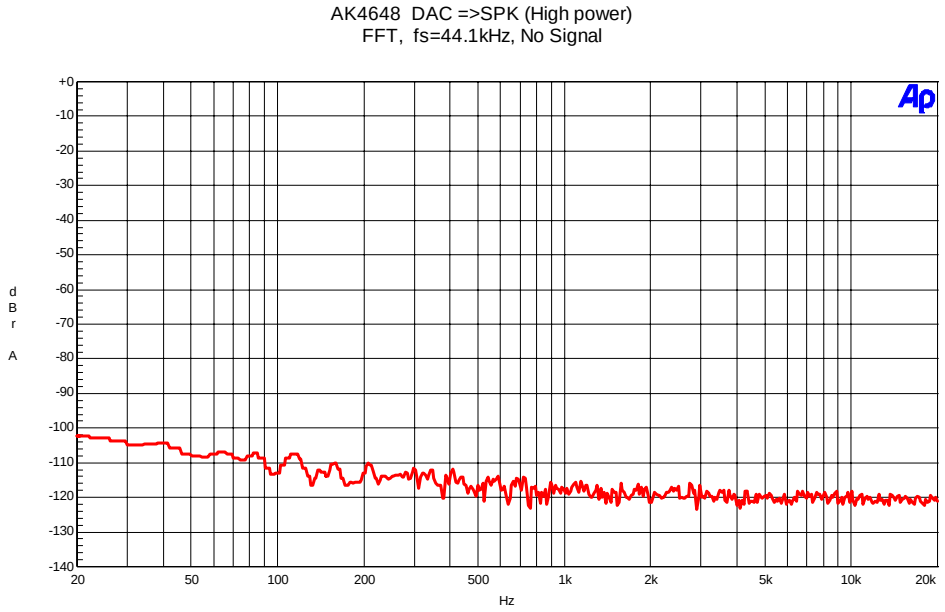


Figure 72. FFT Plot (No signal)

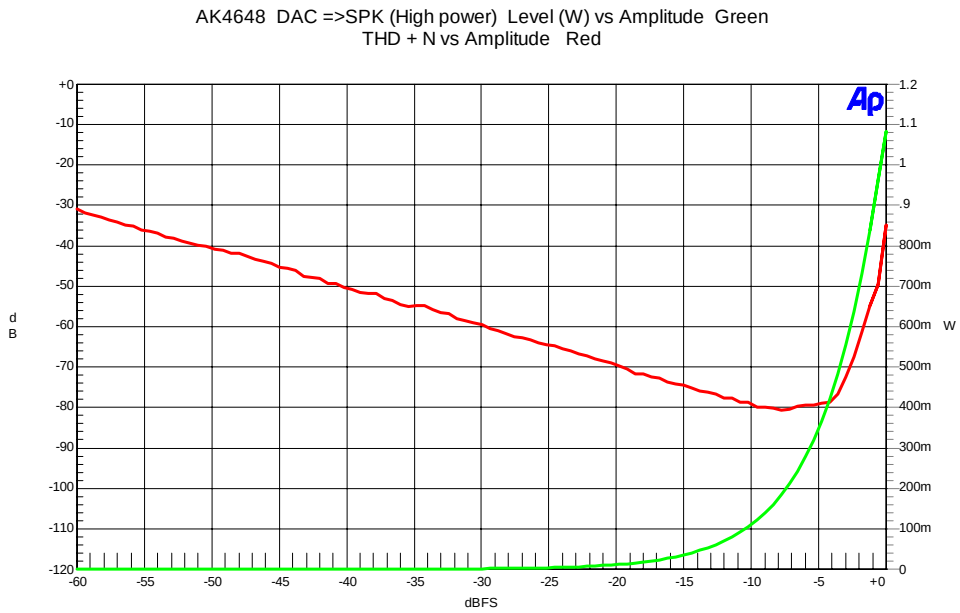
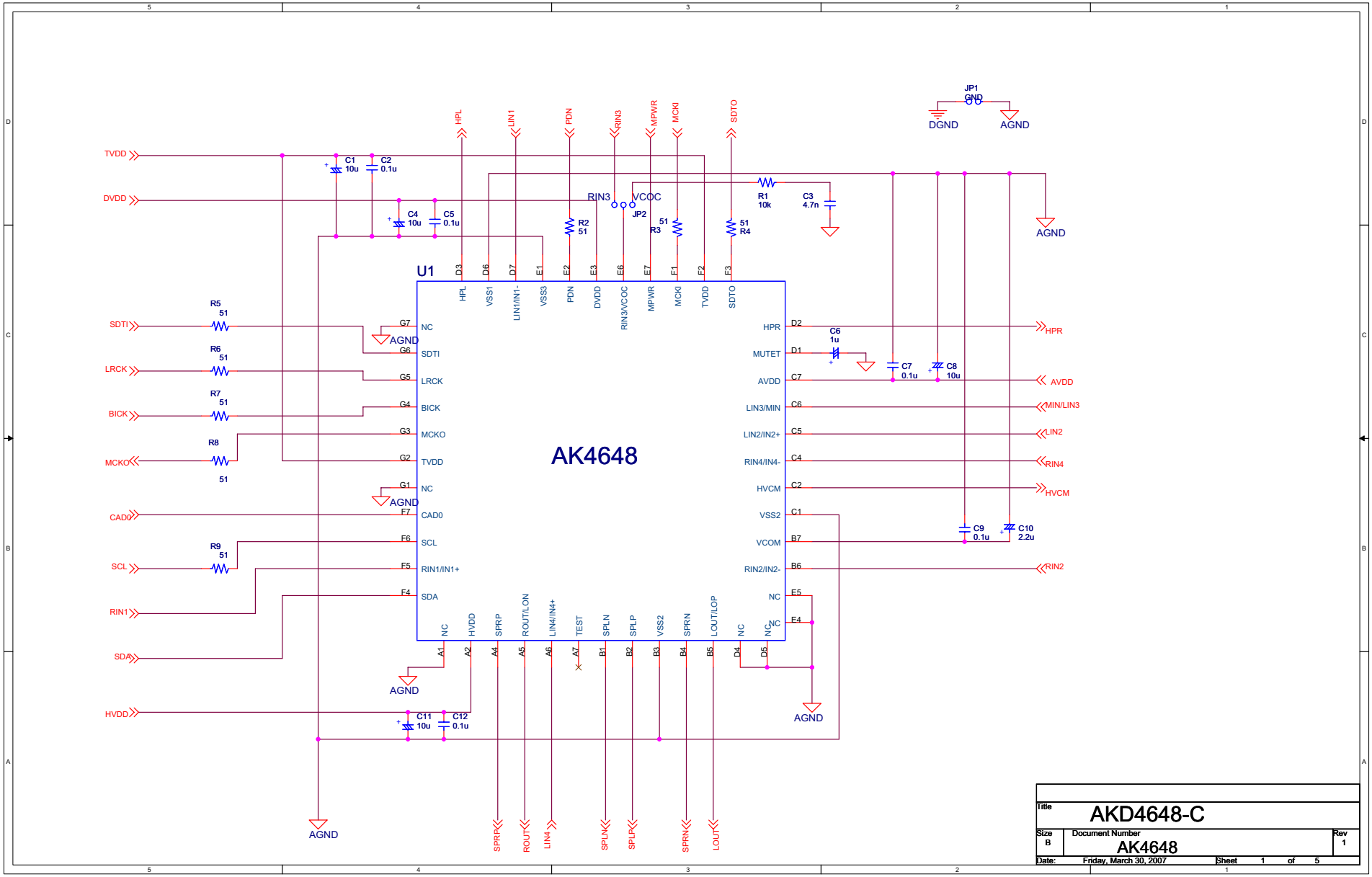


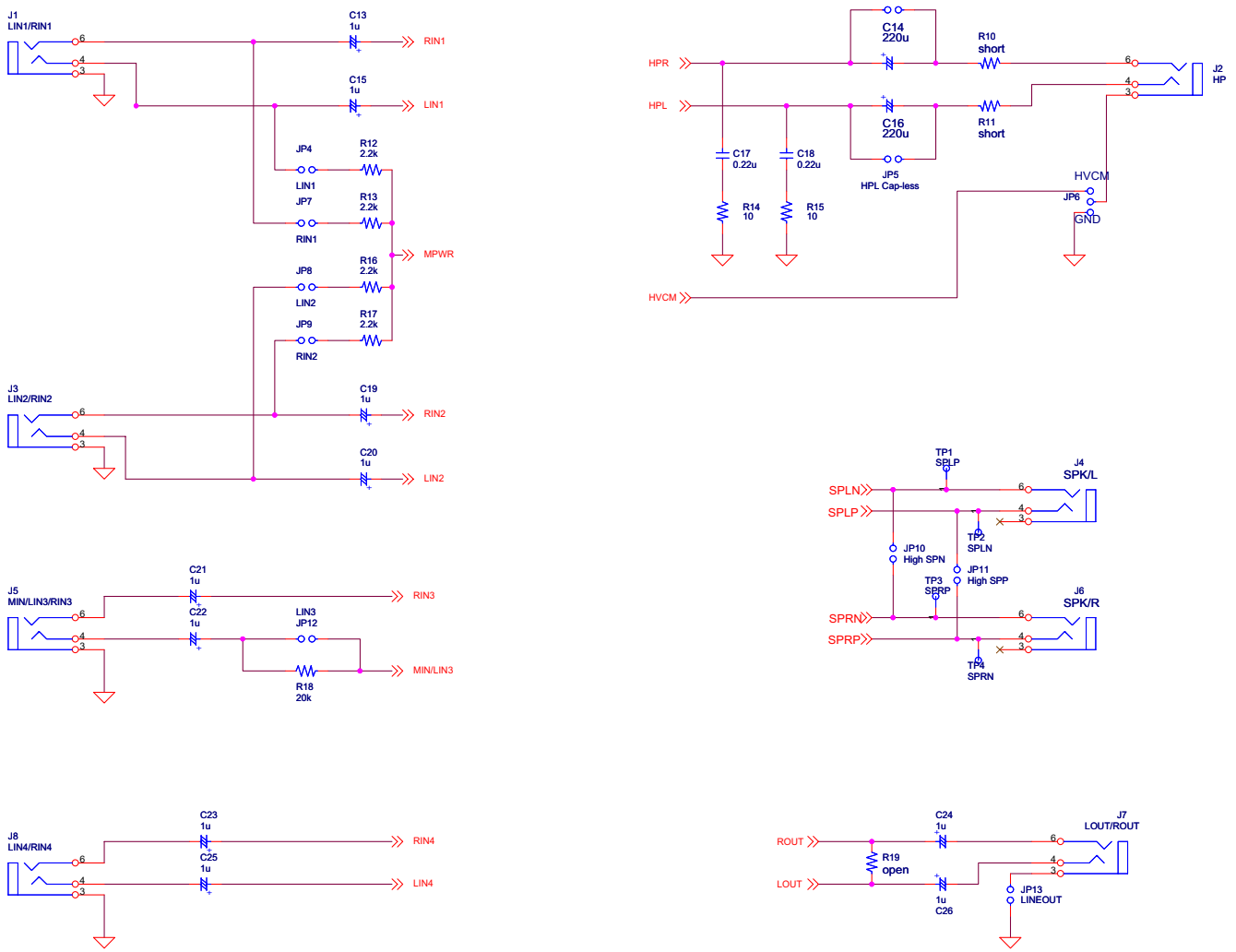
Figure 73. THD+N & Output Power vs. Input Level (SPKG=+12.65dB)

Revision History

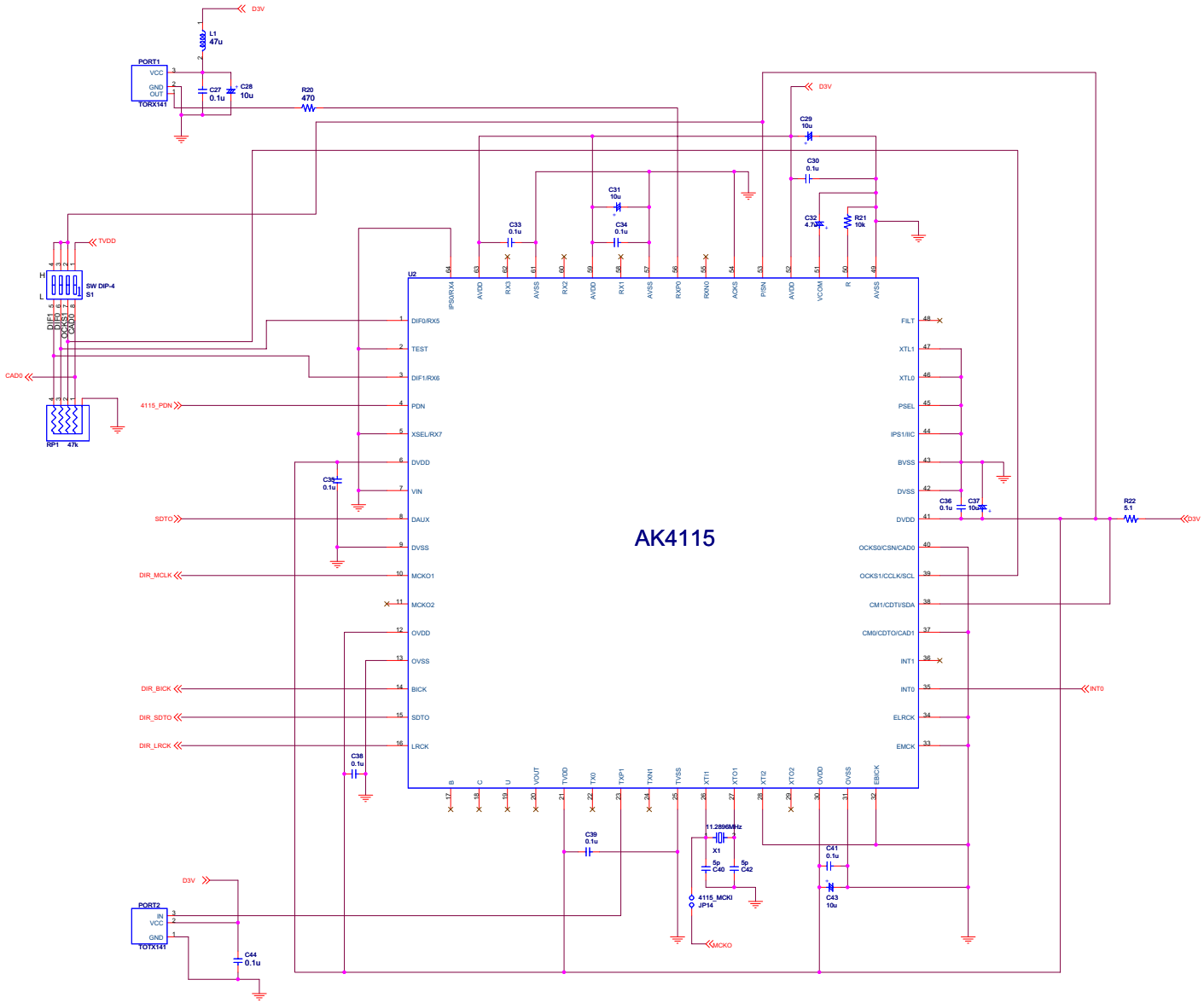
Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
07/03/19	KM088700	0	First Edition	
07/04/13	KM088701	1	Parts Change	AK4648 Rev.A → Rev.B



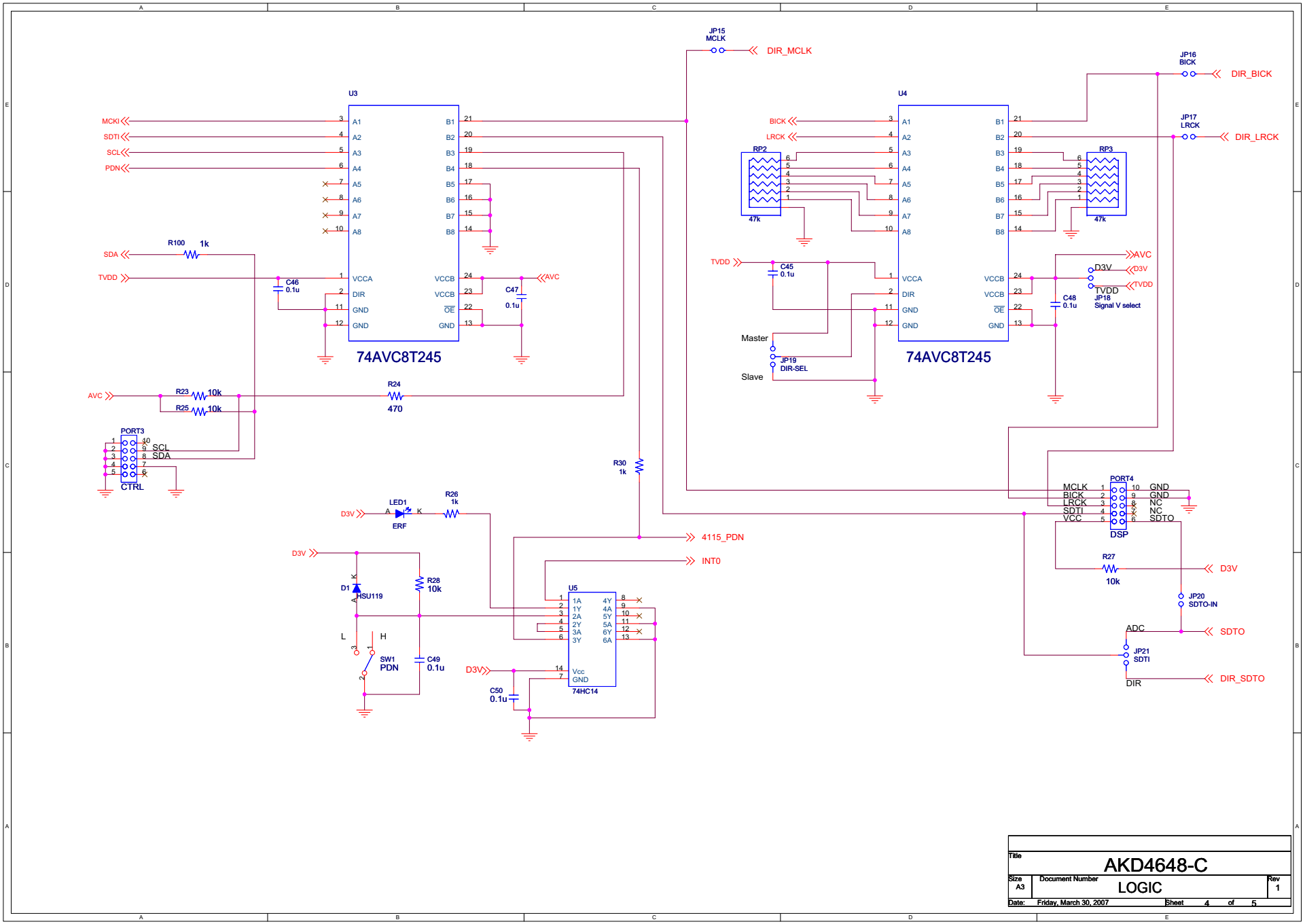
Title	AKD4648-C	
Size B	Document Number AK4648	Rev 1
Date: Friday, March 30, 2007	Sheet 1 of 5	



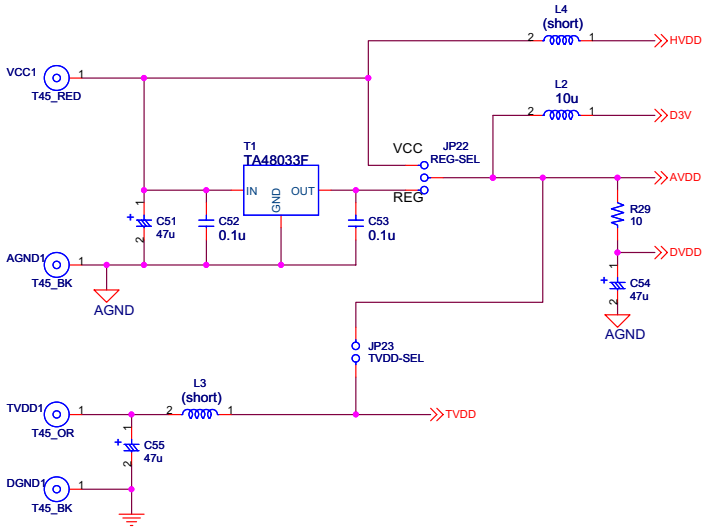
Title	AKD4648-C	
Size A3	Document Number Input/Output	Rev 1
Date: Friday, March 30, 2007	Sheet 2 of 5	



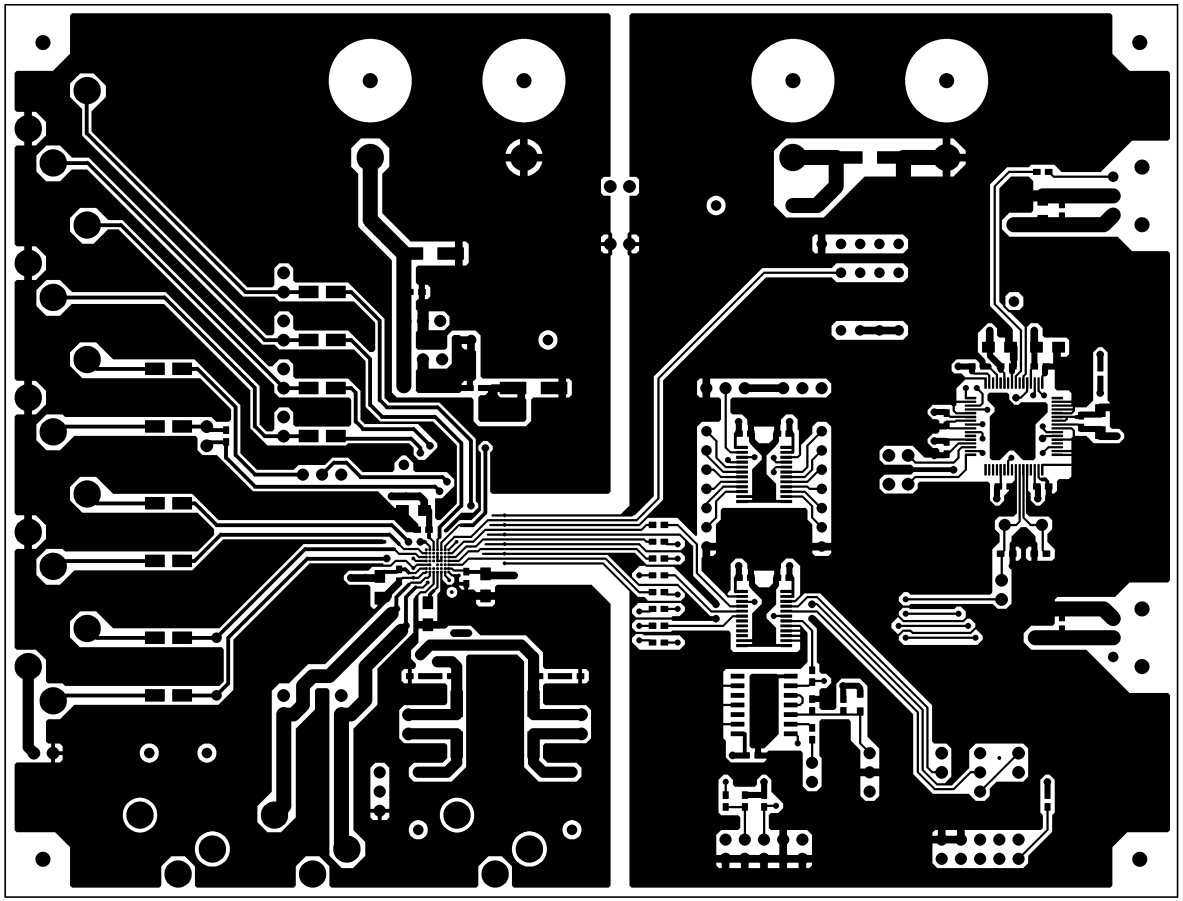
Title	AKD4648-C	
Size A2	Document Number DIR/DIT	Rev 1
Date: Friday, March 30, 2007	Sheet 3 of 5	



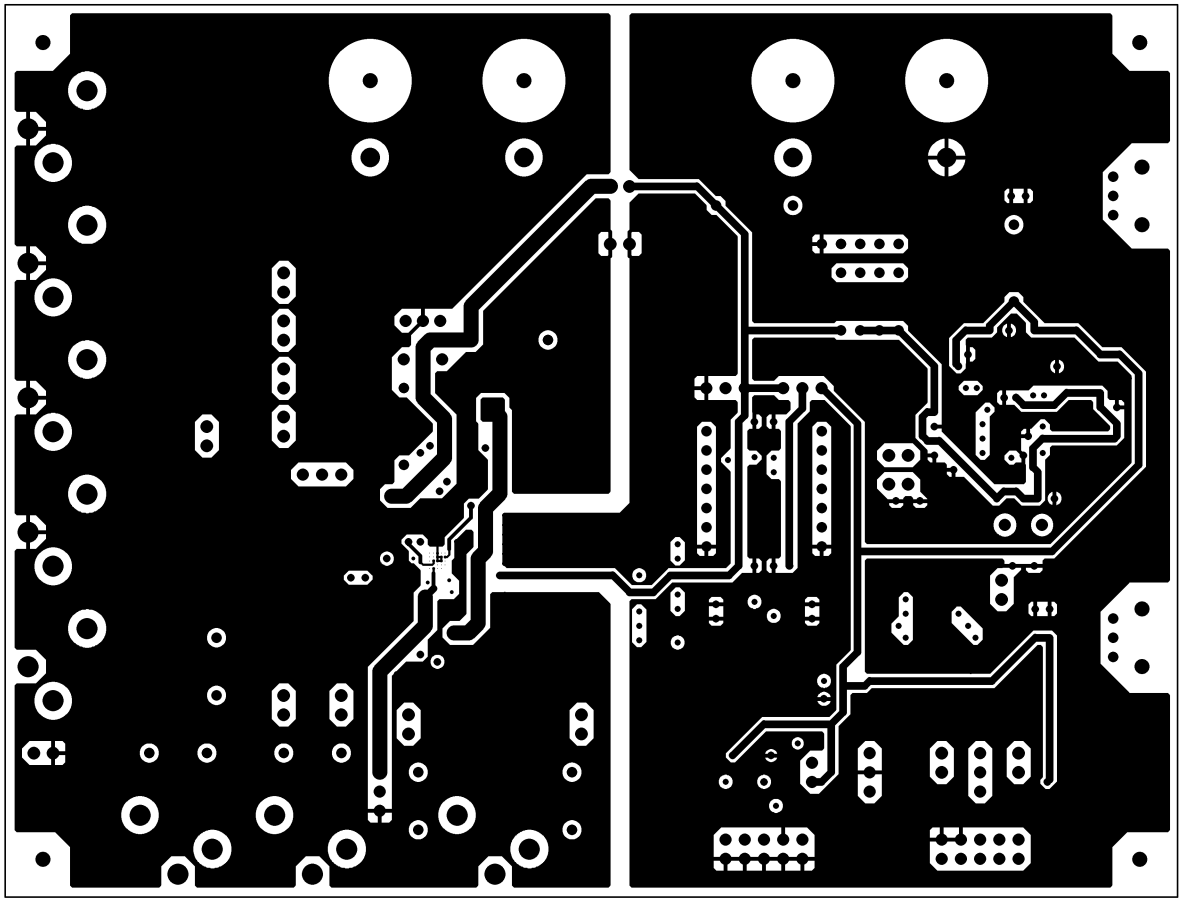
Title	AKD4648-C	
Size A3	Document Number LOGIC	Rev 1
Date: Friday, March 30, 2007	Sheet 4 of 5	



Title	AKD4648-C	
Size B	Document Number POWER	Rev 1
Date: Friday, March 30, 2007	Sheet 5 of 5	



22331 L1



22331 L2

22331 L3

22331 L4

22331 L1 SR SILK

22331 L4 SR SILK