CMOS 8–Bit Microcontrollers

TMP90P800N/TMP90P800F

1. Outline and Characteristics

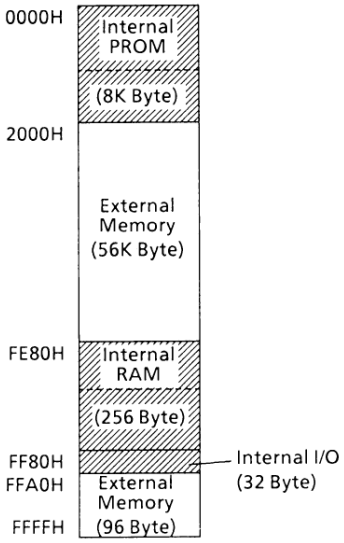
The TMP90P800 is a system evaluation LSI having a built in One-Time PROM for TMP90C400/800.

A programming and verification for internal PROM is achieved by using a general EPROM programmer with an adapter socket.

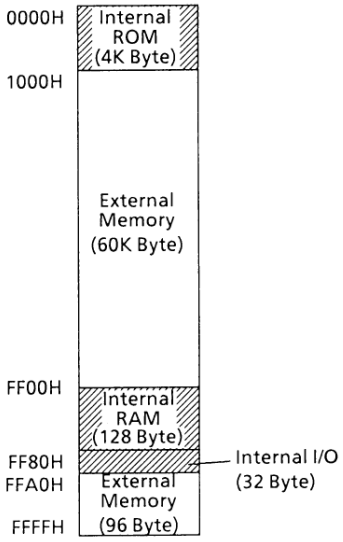
The function of this device is exactly same as the TMP90C400 by programming to the internal PROM.

The differences between TMP90P800 and TMP90C400 are the memory size (ROM/RAM).

The following are the memory map of TMP90P800 and TMP90C400.



TMP90P800 Memory Map



TMP90C400 Memory Map

The TMP90P800N is in a Shrink Dual Inline Package (SDIP64-P-750).

The TMP90P800F is in a Quad Flat Package (QFP64-P-1420A).

Parts No.	ROM	RAM	Package	Adapter Socket No.
TMP90P800N	OTP 8192 x 8bit	256 x 8bit	64-SDIP	BM1142
TMP90P800F			64-FP	BM1147

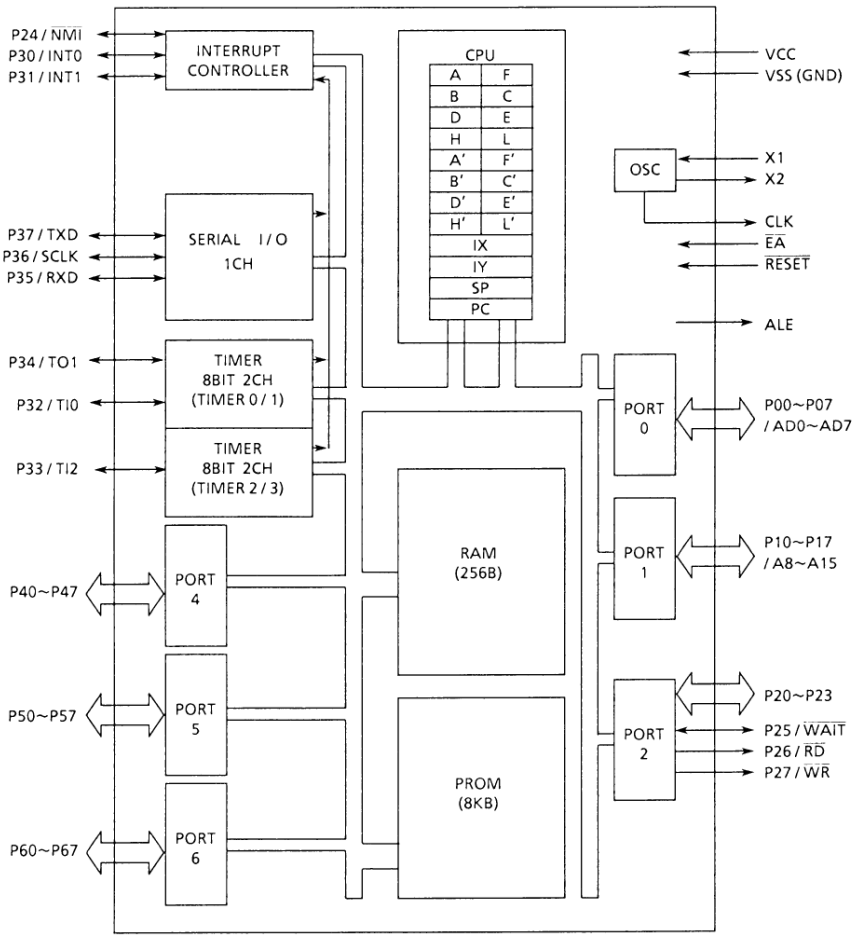


Figure 1. TMP90P800 Block Diagram

2. Pin Assignment and Functions

The assignment of input/output pins, their names and functions are described below.

2.1 Pin Assignment

Figure 2.1 shows pin assignment of the TMP90P800.

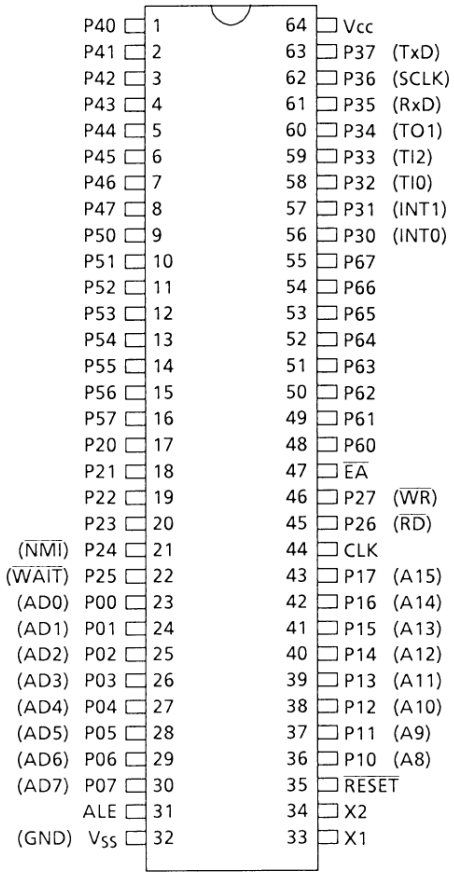


Figure 2.1 (1). Pin Assignment (64-SDIP)

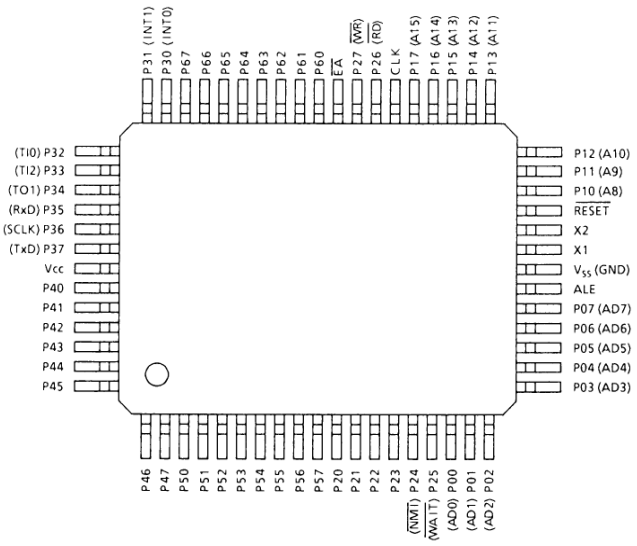


Figure 2.1 (2). Pin Assignment (64-FP)

2.2 Pin Names and Functions

The TMP90P800 has MCU mode and PROM mode.

(1) MCU Mode (The TMP90C400 and the TMP90P800 are pin compatible).

Table 2.2.1 Pin Names and Functions (1/2)

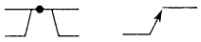
Pin Name	No. of pins	I/O 3 states	Function
P00 ~ P07 /AD0 ~ AD7	8	I/O	Port 0: 8-bit I/O port that allows selection of input/output on bit basi.s
		3 states	Address/Data Bus: Also functions as the lower 8 bits bidirectional data bus for external memory.
P10 ~ P17 /A8 ~ A15	8	I/O	Port 1: 8-bit I/O port that allows selection on bit basis.
		Output	Address Bus: The upper 8 bits address bus for external memory.
P20 ~ P23	4	I/O	Port 20 ~ 23: 4-bit I/O port with a pull-up resistor that allows selection on bit basis
P24 /NMI	1	I/O	Port 24: 1-bit I/O port with a pull-up resistor.
		Input	Non-maskable interrupt request pin: Falling edge interrupt register pin.
P25 /WAIT	1	I/O	Port 25: 1-bit I/O port with a pull-up resistor.
		Input	Wait: Input pin for connecting slow speed memory of peripheral LSI
P26 /RD	1	Output	Port 26: 1-bit output port
		Output	Read: Generates strobe signal for reading external memory.
P27 /WR	1	Output	Port 27: 1-bit output port
		Output	Write: Generates strobe signal for writing into external memory
P30 /INT0	1	I/O	Port 30: 1-bit I/O port with a pull-up resistor.
		Input	Interrupt request pin 0: Interrupt request pin (Level/rising edge is programmable) 
P31 /INT1	1	I/O	Port 31: 1-bit I/O port with a pull-up resistor.
		Input	Interrupt request pin 1: Rising edge interrupt request pin 
P32 /T10	1	I/O	Port 32: 1-bit I/O port with a pull-up resistor.
		Input	Timer input 0: Counter input pin for Timer 0
P33 /TI2	1	I/O	Port 33: 1-bit I/O port with a pull-up resistor.
		Output	Timer input 2: Counter input pin for Timer 2

Table 2.2.1 Pin Names and Functions (2/2)

P35 /RxD	1	I/O	Port 35: 1-bit I/O port with a pull-up resistor.
		I/O	Receive Serial Data
P36 /SCLK	1	I/O	Port 36: 1-bit I/O port with a pull-up resistor.
		Output	Serial clock output
P37 TxD	1	I/O	Port 37: 1-bit I/O port with a pull-up resistor.
		Output	Transmitter Serial Data
P40 ~ P47	8	I/O	Port 4: 8-bit I/O port that allows I/O selection on bit basis.
P50 ~ P57	8	I/O	Port 5: 1-bit I/O port with a pull-up resistor.
P60 ~ P67	8	I/O	Port 6: 8-bit I/O port that allows I/O selection on bit basis.
ALE	1	Output	Address latch enable signal: The negative edge of ALE supplies an address latch timing for external memory access.
$\overline{EA}$	1	Input	External access: Connects with V_{CC} pin in the TMP90P800 built ROM is used.
CLK	1	Output	Clock output: Generates clock pulse at 1/4 frequency of clock oscillation. It is Pulled up internally during resetting.
$\overline{RESET}$	1	Input	Reset: Initializes the TMP90P800.
X1/X2	2	I/O	Pin for quartz crystal or ceramic resonator
V_{CC}	1	–	Power supply (+5V)
V_{SS}	1	–	Ground (0V)

(2) PROM Mode

Table 2.2.2

Pin Function Name	**No. of pins**	**I/O**	**Function**	**Pin Name (MCU mode)**
A7 ~ A0	8	Input	Program Memory Address Input	P67 ~ P60
A12 ~ A8	5	Input		P14 ~ P10
A15 ~ A13	3	Input	Be fixed to “L” level. (Note)	P17 ~ P15
D7 ~ D0	8	I/O	Data Input/Output	P07 ~ P00
$\overline{OE}$	1	Input	Output Enable Input	P26
$\overline{CE}$	1	Input	Chip Enable Input	P27
VPP	1	Power Supply	12.5V/5V (Programming Power Supply)	$\overline{EA}$
VCC	1	Power Supply	5V	
VSS	1	Power Supply	0V	
Pin Name	**No. of pins**	**I/O**	**Pin Setting**	
P20 ~ P23	4	Input	Be fixed to “L” level.	
$\overline{NMI}$	1	Input	Be fixed to “H” level.	
$\overline{WAIT}$	1	Input	Be fixed to “H” level.	
P30 ~ P34	5	Input	Be fixed to “L” level.	
P35, P36	2	Input	Be fixed to “H” level.	
P37	1	Input	Be fixed to “L” level.	
P40 ~ P47 P50 ~ P57	8 8	Input	Be fixed to “L” level.	
RESET	1	Input	Be fixed to “L” level.	
CLK	1	Input	Be fixed to “L” level.	
ALE	1	Output	Open	
X1	1	Input	Resonator connection pin	
X2	1	Output		

(Note) Be fixed to “H” level when The 400-mode Bit or The Security Bit is programmed.

3. Operation

The TMP90P800 is the OTP version of the TMP90C400 that is replaced an internal ROM from Mask ROM to EPROM.

The function of TMP90P800 is exactly as that of TMP90C400 except the internal ROM/RAM size.

Refer to the TMP90C400 except the functions which are not described this section.

The following is an explanation of the hardware configuration and operation in the relation to the TMP90P800.

The TMP90P800 has an MCU mode and a PROM mode.

3.1 MCU Mode

(1) Mode Setting and Function

The MCU mode is set by opening the CLK pin (Output status).

In the MCU mode, the operation is the same as that of TMP90C400.

(2) Memory Map

Figure 3.1 shows the memory map of TMP90P800, and the accessing area by the respective addressing mode.

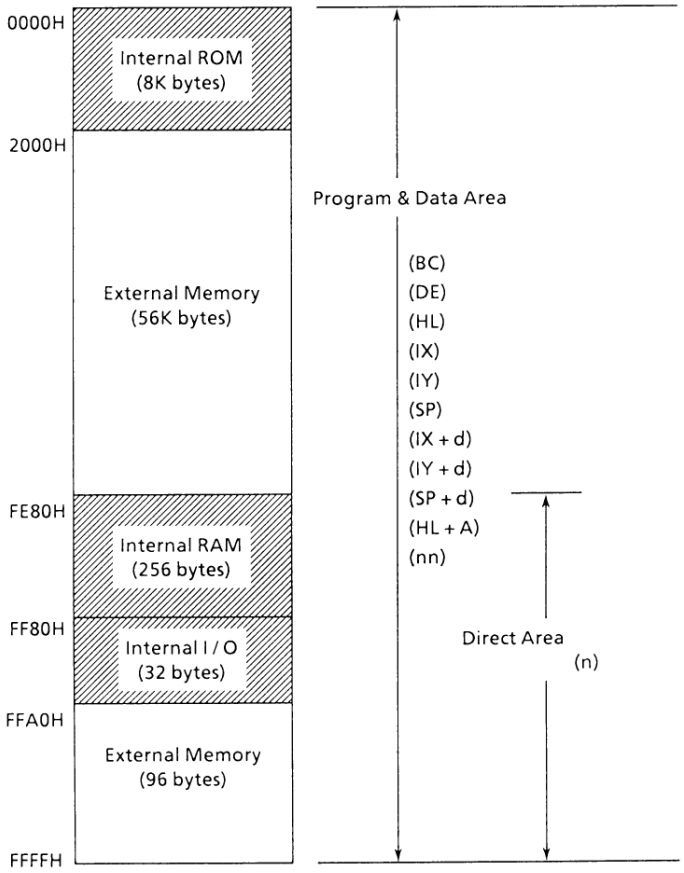


Figure 3.1. TMP90P800 Memory Map

3.2 PROM Mode

(1) Mode Setting and Function

PROM mode is set by setting the $\overline{\text{RESET}}$ and CLK pins to the “L” level.

The programming and verification for the internal PROM is achieved by using a general EPROM programmer with the adaptor socket. The device selection (ROM Type) should be “27256” with following conditions.

size: 256Kbit (32K x 8bit) VPP: 12.5V TPW: 1ms

Figure 3.2 shows the setting of pins in PROM mode.

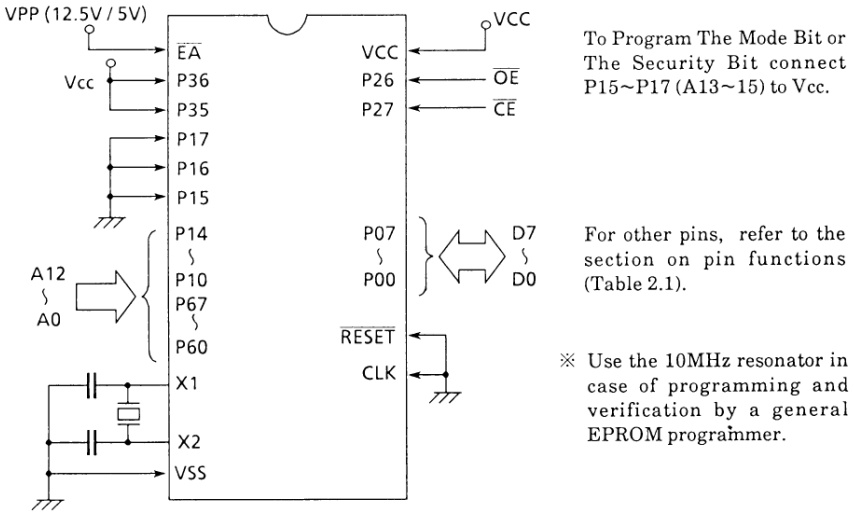


Figure 3.2. PROM Mode Pin Setting

(2) Programming Flow Chart

The programming mode is set by applying 12.5V (programming voltage) to the VPP pin when the following pins are set as follows,

(Vcc : 6.0V) *These conditions can be
($\overline{\text{RESET}}$: “L” level) obtained by using adaptor
(CLK : “L” level) socket.

After the address and data have been fixed, a data on the Data Bus is programmed when the $\overline{\text{CE}}$ pin is set to “Low” (1ms plus is required).

General Programming procedure of an EPROM programmer is as follows,

- Write a data to a specified address for 1ms.
- Verify the data. If the read-out data does not match the expected data, another writing is performed until the correct data is written (Max. 25 times).

After the correct data is written, an additional writing is performed by using three times longer programming pulse width (1ms x programming times), or using three times more programming pulse number. Then, verify the data and increment the address.

The verification for all data is done under the condition of Vpp = Vcc = 5V after all data were written.

Figure 3.3 shows the programming flow chart.

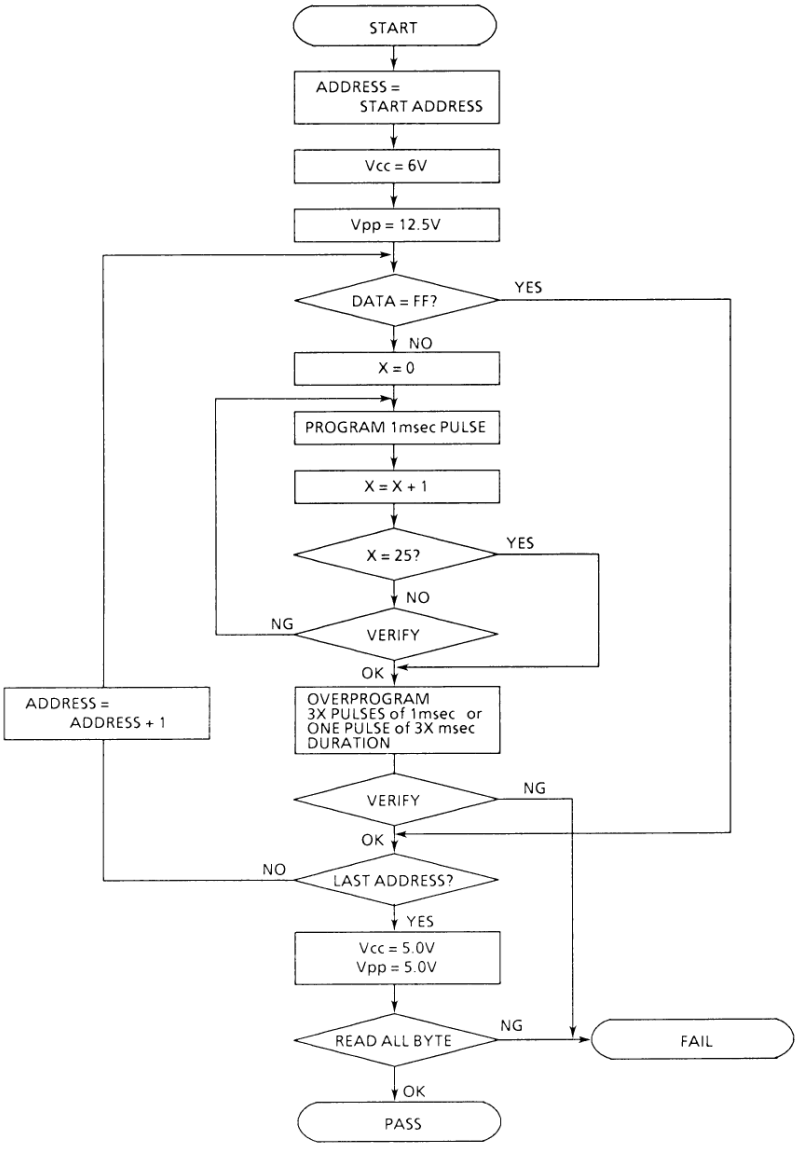


Figure 3.3. Flow Chart

(3) The 400-mode Bit and The Security Bit

The TMP90P800 has The 400-mode Bit and The Security Bit in PROM cell. If The 400-mode Bit is programmed to "0", The TMP90P800 functions as its memory size is same as TMP90C400 (ROM: 0000H ~ 0FFFH, RAM: FF00H ~ FF7FH). If The Security Bit is programmed to "0", the content of the PROM is disable to read in PROM mode. If both The 400-mode Bit and The Security Bit is programmed to "0", the memory size is as same as TMP90C400 and its content of the PROM is disable to read.

How to Program The 400-Mode Bit or The Security Bit.

1) Connect A13, A14 and A15 pins to Vcc. [Otherwise connect them to GND to program PROM. (address 0000H ~ 1FFFH)]

2) Set programming address to 0000H.

3) To program the 400-mode Bit, set D1 to "0".

4) To program the Security Bit, set D0 to "0".

5) Set D2 ~ D7 to "1" respectively.

The following table shows the 8-bit data to program The 400-mode Bit or The Security Bit.

Table 3.1 Data to Program

Bit To PROGRAM	D0 ~ D7	A0 ~ A12	A13, A14, A15
The 400-mode Bite The Security BIt The 400-mode Bit and The Security Bit	FDH FEH FCH	all "0"	all "1"
PROM (0000H ~ 1FFFH)	–	–	all "0"

4. Electrical Characteristics

TMP90P800N/TMP90P800F

4.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Supply voltage	-0.5 ~ + 7	V
V_{IN}	Input voltage	-0.5 ~ V_{CC} + 0.5	V
P_D	Power dissipation (Ta = 85°C)	F 500	mW
		N 600	
T_{SOLDER}	Soldering temperature (10s)	260	°C
T_{STG}	Storage temperature	-65 ~ 150	°C
T_{OPR}	Operating temperature	-40 ~ 85	°C

4.2 DC Characteristics

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
TA = -20 ~ 70°C (1 ~ 12.5MHz)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (P0)	-0.3	0.8	V	–
V_{IL1}	P1, P2, P3, P4, P5, P6	-0.3	$0.3V_{CC}$	V	–
V_{IL2}	$\overline{RESET}$, $\overline{NMI}$	-0.3	$0.25V_{CC}$	V	–
V_{IL3}	$\overline{EA}$	-0.3	0.3	V	–
V_{IL4}	X1	-0.3	$0.2V_{CC}$	V	–
V_{IH}	Input High Voltage (P0)	2.2	V_{CC} + 0.3	V	–
V_{IH1}	P1, P2, P3, P4, P5, P6	$0.7V_{CC}$	V_{CC} + 0.3	V	–
V_{IH2}	$\overline{RESET}$, $\overline{NMI}$	$0.75V_{CC}$	V_{CC} + 0.3	V	–
V_{IH3}	$\overline{EA}$	V_{CC} - 0.3	V_{CC} + 0.3	V	–
V_{IH4}	X1	$0.8V_{CC}$	V_{CC} + 0.3	V	–
V_{OL}	Output Low Voltage	–	0.45	V	I_{OL} = 1.6mA
V_{OH} V_{OH1} V_{OH2}	Output High Voltage	2.4 $0.75V_{CC}$ $0.9V_{CC}$	–	V V V	I_{OH} = -400μA I_{OH} = -100μA I_{OH} = -20μA
I_{DAR}	Darlington Drive Current (8 I/O pins) (Note)	-0.1	-3.5	mA	V_{EXT} = 1.5V R_{EXT} = 1.1kΩ
I_{LI}	Input Leakage Current	0.02 (Typ)	±5	μA	0.0 ≤ Vin ≤ V_{CC}
I_{LO}	Output Leakage Current	0.05 (Typ)	±10	μA	0. 2≤ Vin ≤ V_{CC} - 0.2
I_{CC}	Operating Current (RUN) Idle 1 Idle 2	20 (Typ) 1.5 (Typ) 6 (Typ)	40 5 15	mA mA mA	tosc = 10MHz (25%Up @12.5MHz)
	STOP (TA = -40 ~ 85°C) STOP (TA = 0 ~ 50°C)	0.05(Typ)	50 10	μA μA	0.2 ≤ Vin ≤ V_{CC} - 0.2
V_{STOP}	Power Down Voltage (@STOP)	2 RAM BACK UP	6	V	V_{IL2} = $0.2V_{CC}$, V_{IH2} = $0.8V_{CC}$
R_{RST}	$\overline{RESET}$ Pull Up Register	50	150	KΩ	–
CIO	Pin Capacitance	–	10	pF	testfreq = 1MHz
V_{TH}	Schmitt width $\overline{RESET}$, $\overline{NMI}$	0.4	1.0 (Typ)	V	–

Note: I_{DAR} is guaranteed for a total of up to 8 optional ports.

4.3 AC Characteristics

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
TA = -20 ~ 70°C (1 ~ 12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		12.5MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{OSC}	Oscillation cycle (= x)	80	1000	100	–	80	–	ns
t_{CYC}	CLK Period	4x	4x	400	–	320	–	ns
t_{WH}	CLK High width	2x - 40	–	160	–	120	–	ns
t_{WL}	CLK Low width	2x - 40	–	160	–	120	–	ns
t_{AL}	A0 ~ 7 effective address→ALE fall	0.5x - 15	–	35	–	25	–	ns
t_{LA}	ALE fall →A0 ~ 7 hold	0.5x - 15	–	35	–	25	–	ns
t_{LL}	ALE Pulse width	x - 40	–	60	–	40	–	ns
t_{LC}	ALE fall $\overline{RD}/\overline{WR}$ fall	0.5x - 30	–	20	–	10	–	ns
t_{CL}	$\overline{RD}/\overline{WR}$ →ALE rise	0.5x - 20	–	30	–	20	–	ns
t_{ACL}	A0 ~ 7 effective address →$\overline{RD}/\overline{WR}$ fall	x - 25	–	75	–	55	–	ns
t_{ACH}	Upper effective address →$\overline{RD}/\overline{WR}$ fall	1.5x - 50	–	100	–	70	–	ns
t_{CA}	$\overline{RD}/\overline{WR}$ fall →Upper address hold	0.5x - 20	–	30	–	20	–	ns
t_{ADL}	A0 ~ 7 effective address →Effective data input	–	3.0x - 35	–	265	–	205	ns
t_{ADH}	Upper effective address →Effective data input	–	3.5x - 55	–	295	–	225	ns
t_{RD}	$\overline{RD}$ fall →Effective data input	–	2.0x - 50	–	150	–	110	ns
t_{RR}	$\overline{RD}$ Pulse width	2.0x - 40	–	160	–	120	–	ns
t_{HR}	$\overline{RD}$ rise →Data hold	0	–	0	–	0	–	ns
t_{RAE}	$\overline{RD}$ rise→ Address enable	x - 15	–	85	–	65	–	ns
t_{WW}	WR pulse width	2.0x - 40	–	160	–	120	–	ns
t_{DW}	Effective data→$\overline{WR}$ rise	2.0x - 50	–	150	–	110	–	ns
t_{WD}	WR rise→Effective data hold	0.5x - 10	–	40	–	30	–	ns
t_{ACKH}	Upper address→CLK fall	2.5x - 50	–	200	–	150	–	ns
t_{ACKL}	Lower address →CLK fall	2.0x - 50	–	150	–	110	–	ns
t_{CKHA}	CLK fall→Upper address hold	1.5x - 80	–	70	–	40	–	ns
t_{CCK}	$\overline{RD}/\overline{WR}$→CLK fall	x - 25	–	75	–	55	–	ns
t_{CKHC}	CLK fall→$\overline{RD}/\overline{WR}$ rise	x - 60	–	40	–	20	–	ns
t_{DCK}	Valid data CLK fall	x - 50	–	50	–	30	–	ns
t_{CWA}	$\overline{RD}/\overline{WR}$ fall→Valid $\overline{WAIT}$	–	x - 40	–	60	–	40	ns
t_{AWAL}	Lower address →Valid $\overline{WAIT}$	–	2.0x - 70	–	130	–	90	ns
t_{WAH}	CLK fall →Valid $\overline{WAIT}$ hold	0	–	0	–	0	–	ns
t_{AWAH}	Upper address →Valid $\overline{WAIT}$	–	2.5x - 70	–	180	–	130	ns
t_{CPW}	CLK fall →Port Data Output	–	X + 200	–	300	–	280	ns
t_{PRC}	Port Data Input →CLK fall	200	–	200	–	200	–	ns
t_{CPR}	CLK fall →Port Data hold	100	–	100	–	100	–	ns

AC Measuring Conditions

- Output level: High 2.2V/Low 0.8V, C_L = 50pF
  (However, CL = 100pF for AD0 ~ 7, A8 ~ 15, ALE, $\overline{RD}$, $\overline{WR}$)
- Input level: High 2.4V/Low 0.45V (AD0 ~ AD7)
  High 0.8V_{CC}/Low 0.2V_{CC} (excluding AD0 ~ AD7)

4.4 Zero-Cross Characteristics

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
TA = -20 ~ 70°C (1 ~ 12.5MHz)

Symbol	Parameter	Condition	Min	Max	Unit
V_{ZX}	Zero-cross detection input	AC coupling C = 0.1μF	1	1.8	VAC p-p
A_{ZX}	Zero-cross accuracy	50/60Hz sine wave	–	135	mV
F_{ZX}	Zero-cross detection input frequency	–	0.04	1	KHz

4.5 Serial Channel Timing-I/O Interface Mode

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
CL = 50pF TA = -20 ~ 70°C (1 ~ 12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		12.5MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	Serial Port Clock Cycle Time	8x	–	800	–	640	–	ns
t_{OSS}	Output Data Setup SCLK Rising Edge	6x - 150	–	450	–	330	–	ns
t_{OHS}	Output Data Hold After SCLK Rising Edge	2x - 120	–	80	–	40	–	ns
t_{HSR}	Input Data Hold After SCLK Rising Edge	0	–	0	–	0	–	ns
t_{SRD}	SCLK Rising Edge to Input DATA Valid	–	6x - 150	–	450	–	330	ns

4.6 8-bit Event Counter

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
TA = -20 ~ 70°C (1 ~ 12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		12.5MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{VCK}	TI2 clock cycle	8x + 100	–	900	–	740	–	ns
t_{VCKL}	TI2 Low clock pulse width	4x + 40	–	440	–	360	–	ns
t_{VCKH}	TI2 High clock pulse width	4x + 40	–	440	–	360	–	ns

4.7 Interrupt Operation

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
TA = -20 ~ 70°C (1 ~ 12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		12MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	$\overline{NMI}$, INT0 Low level pulse width 	4x	–	400	–	320	–	ns
t_{INTAH}	$\overline{NMI}$, INT0 High level pulse width 	4x	–	400	–	320	–	ns
t_{INTBL}	INT1 Low level pulse width 	8x + 100	–	900	–	740	–	ns
t_{INTBH}	INT1 High level pulse width 	8x + 100	–	900	–	740	–	ns

4.8 Read Operation (PROM Mode)

DC Characteristic, AC Characterisc

TA = -40 ~ 85°C Vcc = 5V ± 10%

Symbol	Parameter	Condition	Min	Max	Unit
V_{PP}	V_{PP} Read Voltage	–	4.5	5.5	V
V_{IH1}	Input High Voltage (A0 ~ A15, $\overline{CE}$, $\overline{OE}$)	–	0.7 x V_{CC}	Vcc + 0.3	V
V_{IL1}	Input Low Voltage (A0 ~ A15, $\overline{CE}$, $\overline{OE}$)	–	-0.3	0.3 x V_{CC}	V
t_{ACC}	Address to Output Delay	C_L = 50pF	–	2.25TCYC + α	ns

TCYC = 400ns (10MHz Clock)
α = 200ns

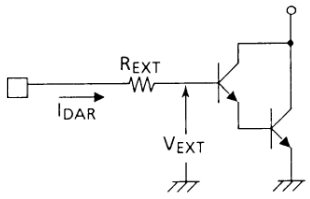
4.9 Programming Operation (PROM Mode)

DC Characteristic, AC Characteristic

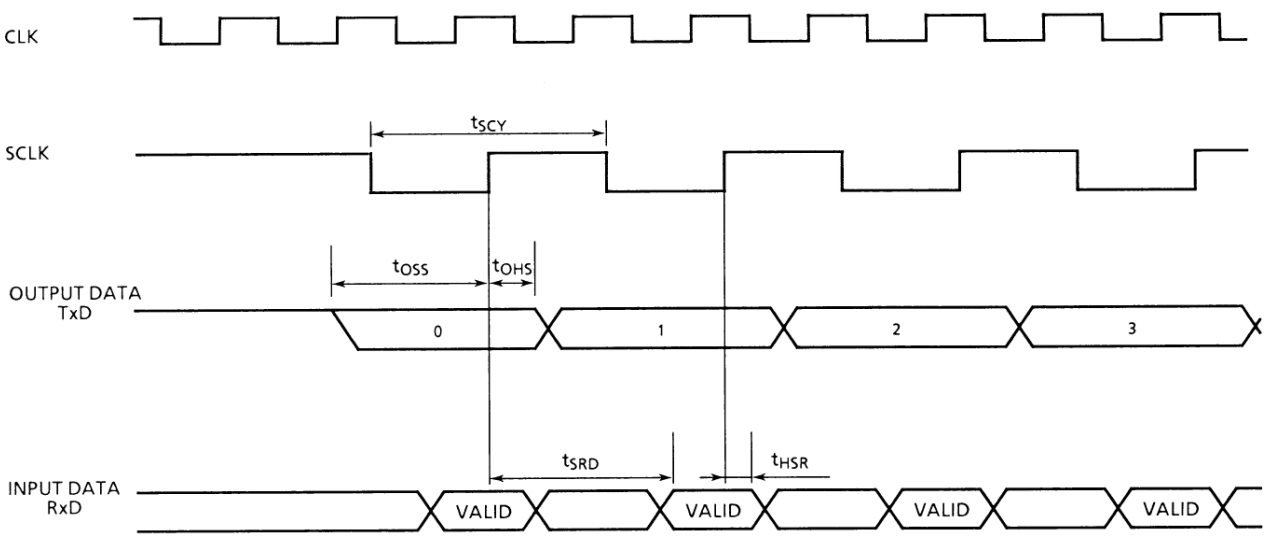
TA = 25 ± 5°C Vcc = 6V ± 0.25V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PP}	Programming Voltage	–	12.25	12.50	12.75	V
V_{IH}	Input High Voltage (D0 ~ D7)	–	0.2V_{CC} + 1.1		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage (D0 ~ D7)	–	-0.3		0.2V_{CC} - 0.1	V
V_{IH1}	Input High Voltage (A0 ~ A15, $\overline{CE}$, $\overline{OE}$)	–	0.7V_{CC}		V_{CC} + 0.3	V
V_{IL1}	Input Low Voltage (A0 ~ A15, $\overline{CE}$, $\overline{OE}$)	–	-0.3		0.3V_{CC}	V
I_{CC}	V_{CC} Supply Current	t_{OSC} = 10MHz	–		50	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = 13.00V	–		50	mA
t_{PW}	$\overline{CE}$ Programming Pulse Width	C_L = 50pF	0.95	1.00	1.05	ms

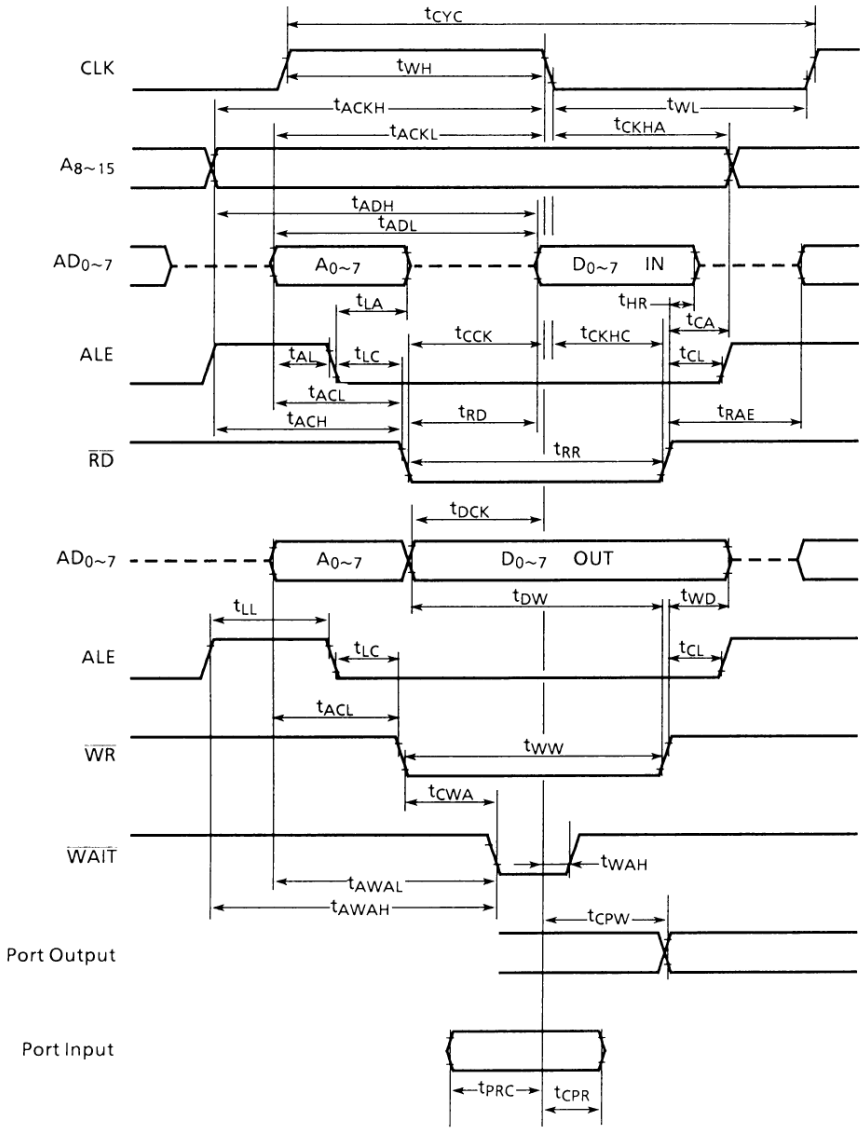
(Reference) Definition of I_{DAR}



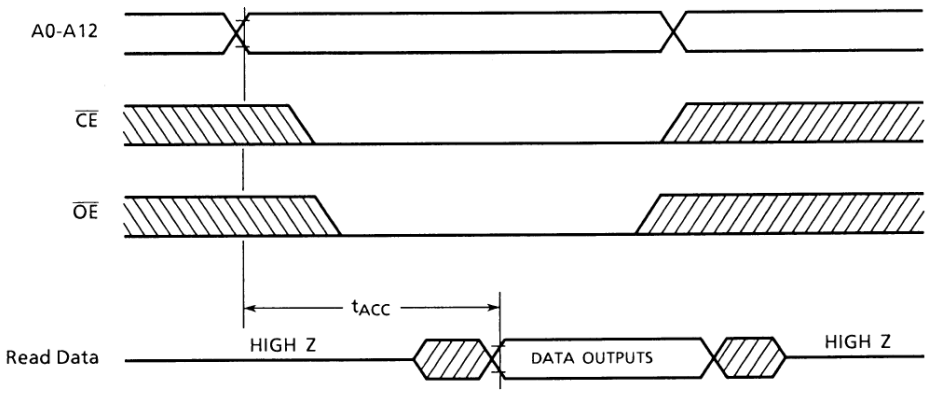
4.10 I/O Interface Mode Timing



4.11 Timing Chart



4.12 Read Operation Timing Chart (PROM Mode)



4.13 Programming Operation Timing Chart (PROM Mode)