Ordering number : EN*A0459A

Preliminary

SANYO Semiconductors
DATA SHEET

LC72F3781 — CMOS IC Electronic tuning radio for car audio ETR Controller

Overview

The LC72F3781 is a ETR controller with an on-chip one-time PROM for use with the LC723781N, 2N, 3N, 4 and 5 mask versions. Since it has the equivalent electrical performance, pin layout and package as these mask versions, it is ideally suited for checking program operations, starting the initial shipment of finished products and reducing the switchover time frame when specifications are changed.
The PROM size is 128 Kbytes (64K × 16 bits).

Functions

- ROM : Up to 64K steps (65,535×16-bits)
  The subroutine area holds 4K steps (4,096×16-bits)
- RAM : Up to 16K×4-bits (In banks 00 through FF)
- Stack : 32levels
- Serial I/O : Three channels. These circuits can support both 2-wire and 3-wire 8-bit communication techniques, and can be switched between MSB first and LSB first operation.
  One of six internally generated serial transfer clock rates can be selected: 12.5kHz, 37.5kHz, 187.5kHz, 281.25kHz, 375kHz, and 450kHz
- External interrupts : Seven interrupt inputs (pins INT0 through INT5, and the HOLD pin)
  These interrupts can be set to switch between rising and falling edges, although the HOLD pin only supports falling edge detection.
- Internal interrupts : Seven interrupts ; four internal timer interrupts, and three serial I/O interrupts.

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- Interrupt nesting levels : 14 levels
  Interrupts are prioritized in hardware as follows :
  HOLD pin>INT0 pin>INT1 pin>INT2 pin>INT3 pin>INT4 pin>INT5 pin>
  S-I/O0>S-I/O1>S-I/O2>Internal TMR0>Internal TMR1>Internal TMR2>
  Internal TMR3
- A/D Converter : 8-bit resolution and 8 inputs
- General-purpose ports : Input ports : 13
  Output ports : 4
  I/O ports : 62 (These pins can be switched between input and output in 1-bit units.)
- PLL block : Includes a sub-charge pump for high-speed locking.
  Supports dead zone control.
  Built-in unlock detection circuit
  Twelve reference frequencies : 1kHz, 3kHz, 3.125kHz, 5kHz, 6.25kHz, 9kHz, 10kHz, 12.5kHz, 25kHz, 30kHz, 50kHz, and 100kHz
- Universal counter : This 20-bit counter can be used for either frequency or period measurement and supports four measurement (calculation) periods : 1ms, 4ms, 8ms, and 32ms
- Timers : Two fixed timers and two programmable timers (8-bit counters)
  TMR0 : Supports four periods : 10µs, 100µs, 1ms, and 5ms
  TMR1 : Supports four periods : 10µs, 100µs, 1ms, and 10ms
  TMR2 and TMR3 : Programmable 8-bit counters.
  Input clocks with 10µs, 100µs, and 1ms
  One 125-ms timer flip-flop provided
- Beep circuit : Provides 12 fixed beep tones :
  500Hz, 1kHz, 2kHz, 2.08kHz, 2.2kHz, 2.5kHz, 3kHz, 3.125kHz, 3.33kHz, 3.75kHz, 4.17kHz, and 7.03kHz
  Programmable 8-bit beep tone generator.
  Reference clocks with frequencies of 50kHz, 15kHz, and 5kHz.
- Reset : Built-in voltage detection reset circuit
  External reset pin
- Cycle time : 1.33µs/833ns (All instructions are one word), X'tal : 4.5MHz/7.2MHz
  Supports software switching (Initial cycle time is 1.33µs)
- Halt mode : The microcontroller operating clock is stopped in Halt mode.
  There are four conditions that can clear Halt mode : Interrupt requests, timer flip-flop overflows, port PA inputs, and HOLD pin inputs.
- Operating supply voltage : 4.5 to 5.5V (Microcontroller block only : 3.5 to 5.5V)
- Package : QIP100E
- Development tools : Emulator : RE128V
  Evaluation chip : LC72EV3780
  Evaluation board : EB-72EV3780

Specifications

Absolute Maximum Ratings at Ta = 25°C V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		-0.3 to +6.5	V
Input voltage	$V_{IN}1$	PC-PORT	-0.3 to +8	V
	$V_{IN}2$	All input pins other than $V_{IN}1$	-0.3 to V_{DD}+0.3	V
Output voltage	$V_{OUT}1$	PJ-PORT	-0.3 to +14	V
	$V_{OUT}2$	PC-PORT	-0.3 to +8	V
	$V_{OUT}3$	All input pins other than $V_{OUT}1$ and $V_{OUT}2$	-0.3 to V_{DD}+0.3	V
Output current	$I_{OUT}1$	PC, PJ-PORT	0 to +5	mA
	$I_{OUT}2$	PB, PD, PE, PF, PG, PK, PL, PM, PN, PO, PP PQ, PR, PS, PT-PORT, EO1, EO2, SUBPD	0 to +3	mA
Allowable power dissipation	Pd max	Ta = -40 to +85 °C	400	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-40 to +125	°C

Allowable Operating Range at Ta = -40 to +85°C, V_{DD} = 3.5 to 5.5V

Parameter	Symbol	Pins	Ratings			uit
			min	typ	mx	
Supply voltage	$V_{DD}1$	CPU and PLL operation	4.5	5.0	5.5	V
	$V_{DD}2$	CPU operation	3.5		5.5	
	$V_{DD}3$	Memory retention	1.1		5.5	
Input high-level voltage	$V_{IH}1$	PB, PC, PH, PI, PL, PM, PN, PP, PO, PQ, PR, PS, PT-PORT, HCTR, LCTR, INEO, SUBPD (with the I/O ports set to input mode)	0.7V_{DD}		V_{DD}	V
	$V_{IH}2$	PD, PE, PF, PG, PK-PORT, LCTR (in period measurement mode), $\overline{HOLD}$, $\overline{RESET}$	0.8V_{DD}		V_{DD}	V
	$V_{IH}3$	$\overline{SNS}$	2.5		V_{DD}	V
	$V_{IH}4$	PA-PORT	0.6V_{DD}		V_{DD}	V
Input low-level voltage	$V_{IL}1$	PB, PC, PH, PI, PL, PM, PN, PP, PO, PQ, PR, PS, PT-PORT, HCTR, LCTR, INEO, SUBPD (with the I/O ports set to input mode)	0		0.3V_{DD}	V
	$V_{IL}2$	PA, PD, PE, PF, PG, PK-PORT, LCTR (in period measurement mode), $\overline{RESET}$	0		0.2V_{DD}	V
	$V_{IL}3$	$\overline{SNS}$	0		1.1	V
	$V_{IL}4$	$\overline{HOLD}$	0		0.4V_{DD}	V
Input frequency	$F_{IN}1$	XIN	4.0	4.5	8.0	MHz
	$F_{IN}2$	FMIN : $V_{IN}2$, $V_{DD}1$	10		150	MHz
	$F_{IN}3$	FMIN : $V_{IN}3$, $V_{DD}1$	10		130	MHz
	$F_{IN}4$	AMIN(H) : $V_{IN}3$, $V_{DD}1$	2.0		40	MHz
	$F_{IN}5$	AMIN(L) : $V_{IN}3$, $V_{DD}1$	0.5		10	MHz
	$F_{IN}6$	HCTR : $V_{IN}3$, $V_{DD}1$	0.4		12	MHz
	$F_{IN}7$	LCTR : $V_{IN}3$, $V_{DD}1$	100		500	kHz
	$F_{IN}8$	LCTR (in period measurement) : $V_{IH}2$, $V_{IL}2$, $V_{DD}1$	1		20×10^3	Hz
Input amplitude	$V_{IN}1$	XIN	0.5		1.5	Vrms
	$V_{IN}2$	FMIN	0.07		1.5	Vrms
	$V_{IN}3$	FMIN, AMIN, HCTR, LCTR	0.04		1.5	Vrms
Input voltage range	$V_{IN}6$	ADI0 to ADI7	0		V_{DD}	V

Electrical Characteristics in the allowable operating ranges

Parameter	Symbol	Pins	Ratings			unit
			min	typ	max	
Input high-level current	$I_{IH}1$	XIN : $V_I = V_{DD} = 5.0V$	2.0	5.0	15	µA
	$I_{IH}2$	FMIN, AMIN, HCTR, LCTR : $V_I = V_{DD} = 5.0V$	4.0	10	30	µA
	$I_{IH}3$	PA, PB, PC, PD, PE, PF, PG, PH, PI, PK, PL, PM, PN, PO, PP, PQ, PR, PS, PT-PORT, $\overline{SNS}$, $\overline{HOLD}$, $\overline{RESET}$, HCTR, LCTR, INEO, SUBPD : $V_I = V_{DD} = 5.0V$ (with the ports PB, PC, PD, PE, PF, PG, PK, PL, PM, PN, PP, PO, PQ, PR, PS, and PT-PORT set to input mode)			3	µA
Input low-level current	$I_{IL}1$	XIN : $V_I = V_{DD} = V_{SS}$	2.0	5.0	15	µA
	$I_{IL}2$	FMIN, AMIN, HCTR, LCTR : $V_I = V_{DD} = V_{SS}$	4.0	10	30	µA
	$I_{IL}3$	PA, PB, PC, PD, PE, PF, PG, PH, PI, PK, PL, PM, PN, PO, PP, PQ, PR, PS, PT-PORT, $\overline{SNS}$, $\overline{HOLD}$, $\overline{RESET}$, HCTR, LCTR, INEO, SUBPD : $V_I = V_{SS}$ (with the ports PB, PC, PD, PE, PF, PG, PK, PL, PM, PN, PP, PO, PQ, PR, PS, and PT-PORT set to input mode)			3	µA
Hysteresis	VH	PD, PE, PF, PG, PK-PORT, $\overline{RESET}$, LCTR (in period measurement)	$0.1V_{DD}$	$0.2V_{DD}$		V
Output high-level voltage	$V_{OH}1$	PB, PD, PE, PF, PG, PK, PL, PM, PN, PO, PP, PQ, PR, PS, PT-PORT : $I_O = -1mA$	$V_{DD}-1.0$			V
	$V_{OH}2$	EO1, EO2, SUBPD : $I_O = -500µA$	$V_{DD}-1.0$			V
	$V_{OH}3$	XOUT : $I_O = -200µA$	$V_{DD}-1.0$			V
Output low-level voltage	$V_{OL}1$	PB, PD, PE, PF, PG, PK, PL, PM, PN, PO, PP PQ, PR, PS, PT-PORT : $I_O = -1mA$			1.0	V
	$V_{OL}2$	EO1, EO2, SUBPD : $I_O = -500µA$			1.0	V
	$V_{OL}3$	XOUT : $I_O = -200µA$			1.5	V
	$V_{OL}4$	PC, PJ-PORT : $I_O = -5mA$			2.0	V
Output off leakage current	$I_{OFF}1$	PB, PD, PE, PF, PG, PK, PL, PM, PN, PO, PP, PQ, PR, PS, PT-PORT	-3		+3	µA
	$I_{OFF}2$	EO1, EO2, SUBPD	-100		+100	nA
	$I_{OFF}3$	PC, PJ-PORT	-5		+5	µA
A/D conversion error		ADI0 to ADI7	-1.5		+1.5	LSB
Rejected pulse width	PREJ1	$\overline{SNS}$			50	µs
Power down detection voltage	VDET		2.7	3.0	3.3	V
Power supply current	$I_{DD}1$	$V_{DD}1$: $F_{IN}2$ = 130MHz Ta = 25°C		5	10	mA
	$I_{DD}2$	$V_{DD}1$: $F_{IN}2$ = 130MHz Ta = 25°C		5.5	11	mA
	$I_{DD}3$	$V_{DD}2$: Halt mode Ta = 25°C, X'tal : 4.5 MHz *1 (Fig. 1)		0.45		mA
	$I_{DD}4$	$V_{DD}2$: Halt mode Ta = 25°C, X'tal : 7.2MHz		0.55		mA
	$I_{DD}5$	Backup mode (OSC stopped) V_{DD} = 5.5V, Ta = 25°C *2 (Fig. 2)			5	µA
	$I_{DD}6$	Backup mode (OSC stopped) V_{DD} = 2.5V, Ta = 25°C *2 (Fig. 2)			1	µA

*1 : Twenty instruction steps are executed every millisecond. The PLL, universal counter, and other functions are stopped.

Test Circuits

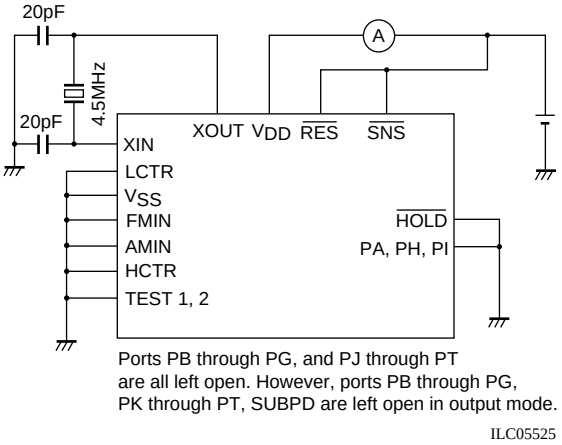


Figure 1. $I_{DD}2$ in Halt Mode

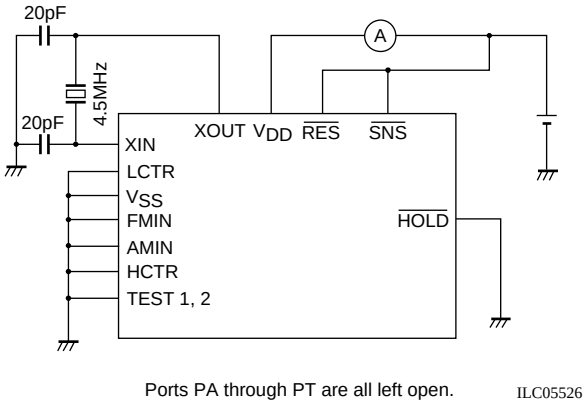
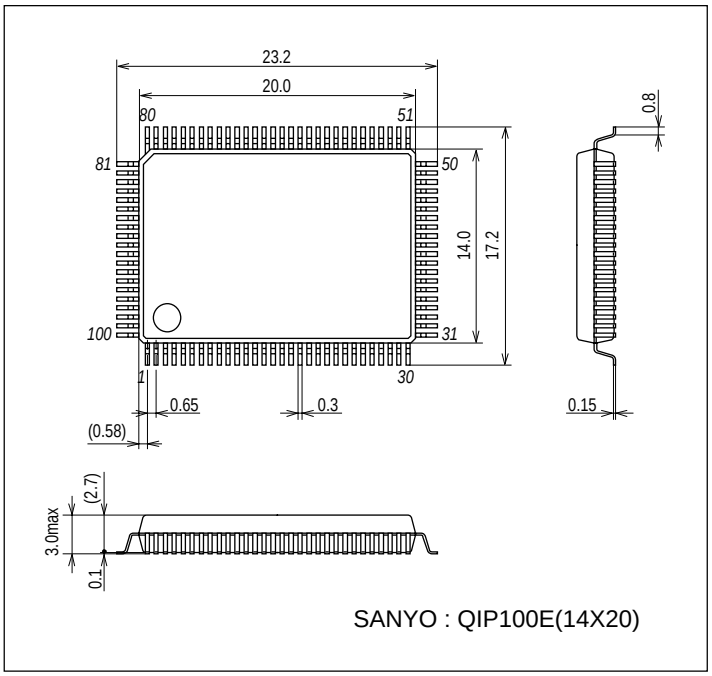


Figure 2. $I_{DD}3$ and $I_{DD}4$ in Backup Mode

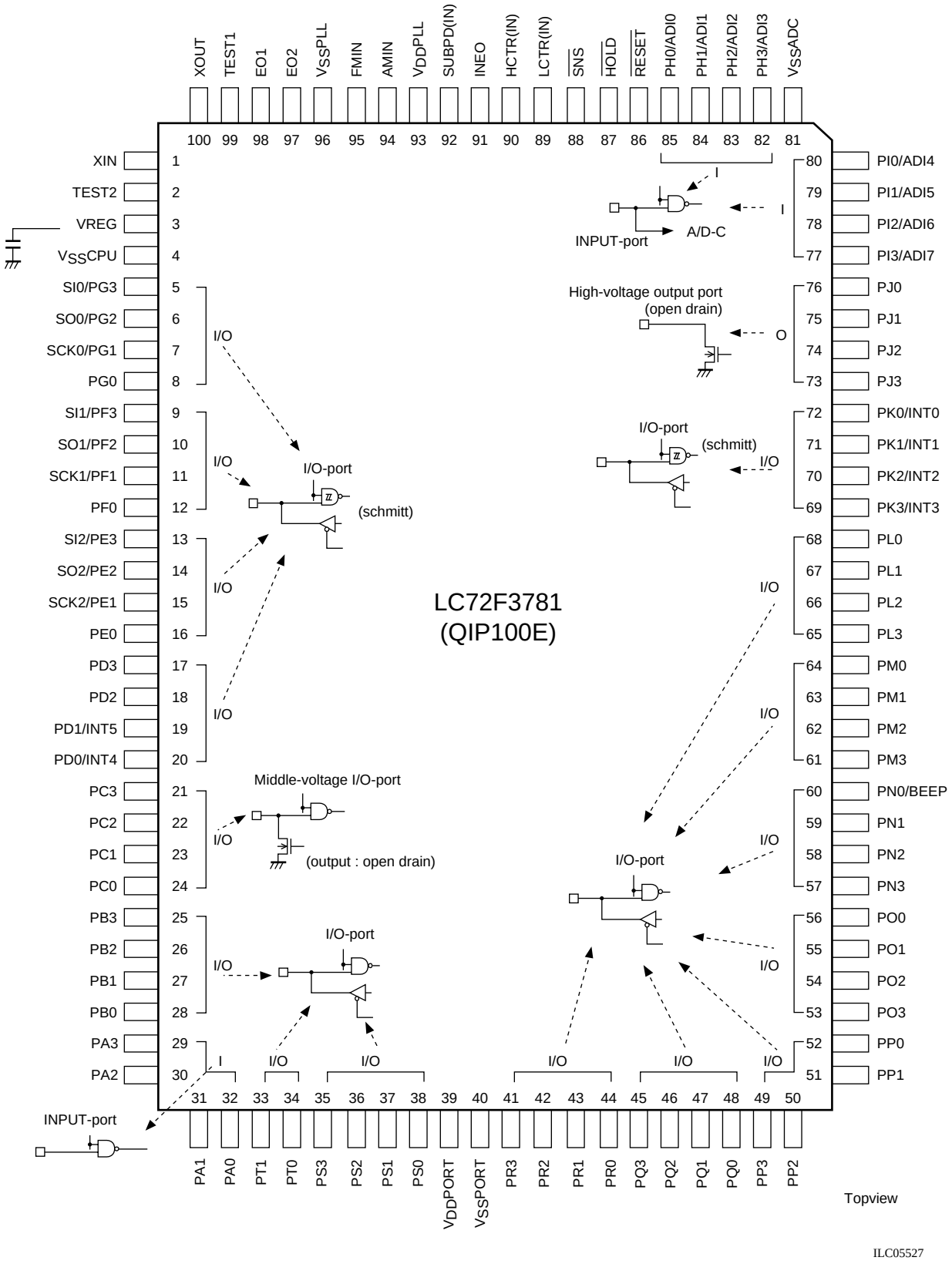
Package Dimensions

unit:mm (typ)

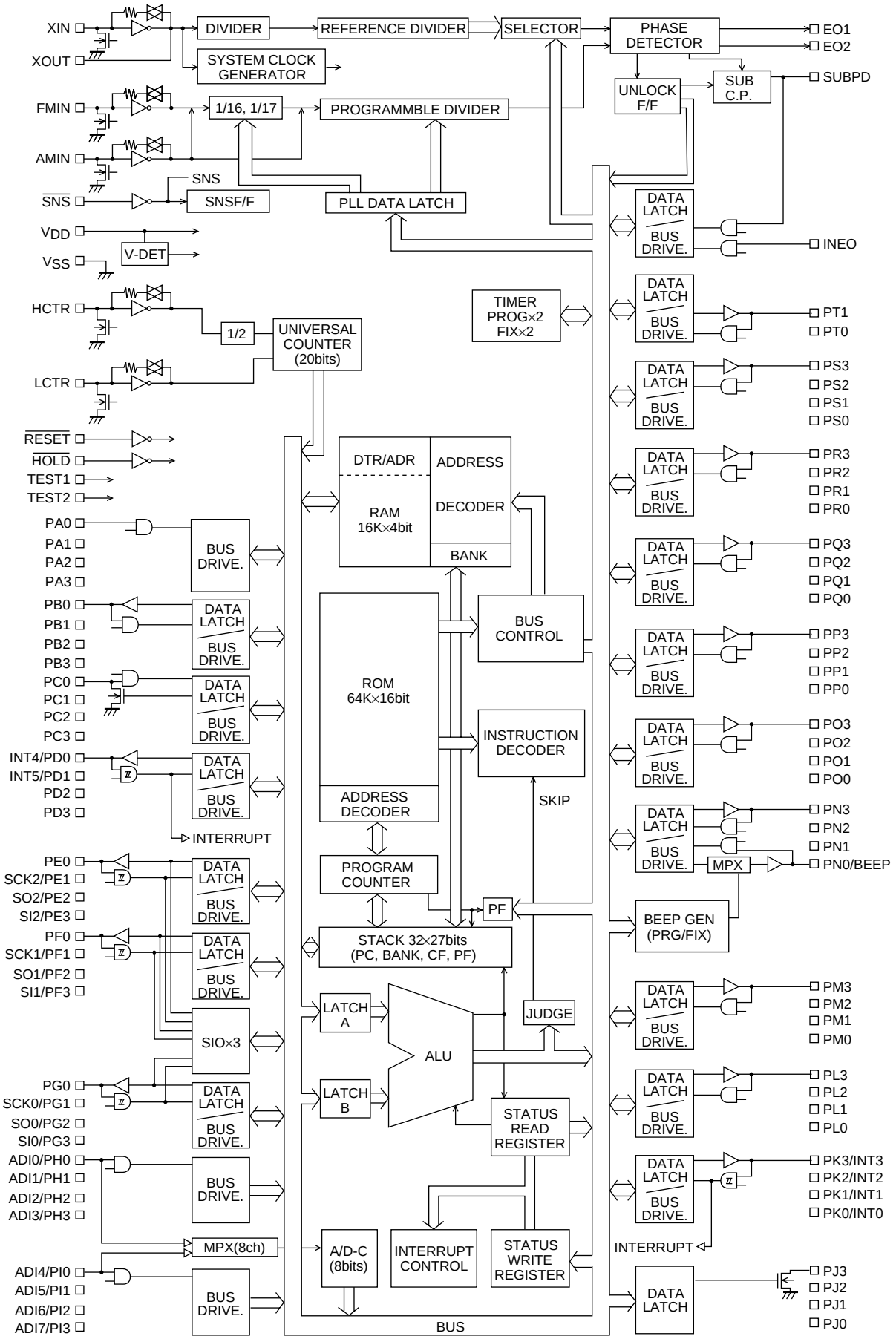
3151A



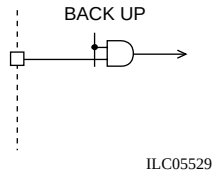
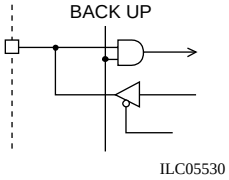
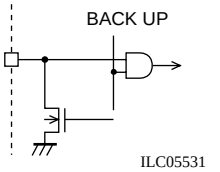
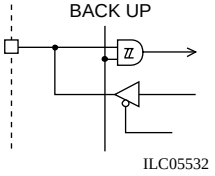
Pin Assignment



Block Diagram



Pin Description

Pin name	Pin No.	I/O	Pin explanation	Equivalent circuit
PA0 PA1 PA2 PA3	32 31 30 29	I	Dedicated input ports. These ports are designed with a low threshold voltage. Input is disabled in Backup mode.	
PB0 PB1 PB2 PB3	28 27 26 25	I/O	General-purpose I/O ports. The mode (input or output) is set using the IOS2 instruction. Input is disabled and the pins go to the high-impedance state in Backup mode. These ports are set up as general-purpose input ports after a power on reset.	
PC0 PC1 PC2 PC3	24 23 22 21	I/O	General-purpose I/O ports (middle-voltage input and output). The mode (input or output) is set using the IOS2 instruction. External pull-up resistors are required since the output circuits are open drain. Input is disabled and the pins go to the high-impedance state in Backup mode. These ports are set up as general-purpose input ports after a power on reset.	
PD0/INT4 PD1/INT5 PD2 PD3	20 19 18 17	I/O	General-purpose I/O and external interrupt shared function ports. The input formats are Schmitt inputs. The external interrupt function is enabled when the external interrupt enable flag is set. • When used as general-purpose I/O ports : The mode (input or output) is set in 1-bit units using the IOS2 instruction. • When used as external interrupt pins : The external interrupt functions are enabled by setting the corresponding external interrupt enable flag (INT4EN or INT5EN). In this case, the pins must be set to input mode in advance. Input is disabled and the pins go to the high-impedance state in Backup mode. These ports are set up as general-purpose input ports after a power on reset.	

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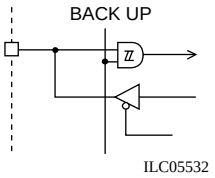
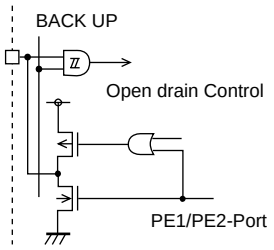
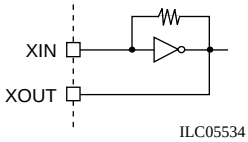
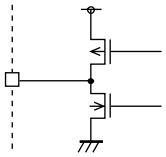
Pin name	Pin No.	I/O	Pin explanation	Equivalent circuit
PE0 PE1/SCK2 PE2/SO2 PE3/SI2 PF0 PF1/SCK1 PF2/SO1 PF3/SI1 PG0 PG1/SCK0 PG2/SO0 PG3/SI0	16 15 14 13 12 11 10 9 8 7 6 5	I/O	General-purpose I/O ports with shared functions as serial I/O ports. The input formats are Schmitt inputs. The PE1/SCK2 and PE2/SO2 pins can be switched to function as open drain outputs. The IOS1 instruction is used to switch between the general-purpose I/O port and serial I/O port functions. • When used as general-purpose I/O ports : The pins are set to the general-purpose I/O port function using the IOS1 instruction. The mode (input or output) is set in 1-bit units using the IOS1 instruction • When used serial I/O ports : The pins are set to the serial I/O port function using the IOS1 instruction. [Pin states when set to the serial I/O port function] PE0, PF0, PG0 … General-purpose I/O PE1, PF1, PG1 … SCK input or output PE2, PF2, PG2 … SO output PE3, PF3, PG3 … SI input The PE1/SCK2 and PE2/SO2 pins can be switched to function as open drain outputs with the IOS2 instruction. When using this circuit type, the external pull-up resistors must be connected to the same power supply as that used by the IC. Input is disabled and the pins go to the high-impedance state in Backup mode. These ports are set up as general-purpose input ports after a power on reset.	 ILC05532  ILC05533
XIN XOUT	1 100	I O	Connections for 4.5MHz/7.2MHz crystal oscillator element	 ILC05534
EO1 EO2	98 97	O	Main charge pump outputs. These pins output a high level when the frequency of the local oscillator divided by n is higher than that of the reference frequency, and they output a low level when that frequency is lower. They go to the high-impedance state when the frequencies match. These pins go to the high-impedance state in Backup mode, after a power on reset, and in the PLL stopped state.	 ILC05535
V_{DD}PORT V_{DD}PLL V_{SS}CPU V_{SS}PORT V_{SS}ADC V_{SS}PLL	39 93 4 40 81 96	-	Power supply connections. The V_{DD}PORT and V_{SS}PORT pins are mainly supply power for the peripheral I/O blocks. The V_{DD}PLL and V_{SS}PLL pins are mainly for the PLL circuits and the regulator. The V_{SS}CPU pin is mainly used by the CPU block. The V_{SS}ADC pin is mainly used by the ADC block. Since all the V_{DD} and V_{SS} pins are independent, all must be connected to the same power supply.	
VREG	3	O	Internal low voltage output. Connect a bypass capacitor to this pin.	

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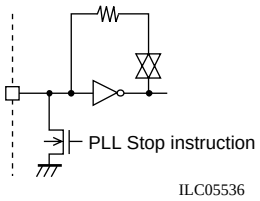
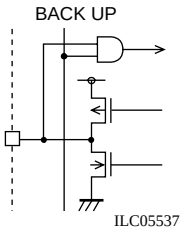
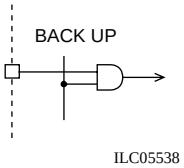
<table>
<tr><th>Pin name</th><th>Pin No.</th><th>I/O</th><th>Pin explanation</th><th>Equivalent circuit</th></tr>
<tr><td>FMIN</td><td>95</td><td>I</td><td>FM VCO (local oscillator) input.
This pin is selected with CW1 in the PLL instruction.
The signal input to this pin must be capacitor coupled.
Input is disabled in Backup mode, after a power on reset, and in the PLL stopped state.</td><td rowspan="2"> 
</td></tr>
<tr><td>AMIN</td><td>94</td><td>I</td><td>AM VCO (local oscillator) input.
This pin is selected and the band set with CW1 (b1, b0) in the PLL instruction.
<table>
<tr><th>b1</th><th>b0</th><th>Band</th></tr>
<tr><td>1</td><td>0</td><td>2 to 40MHz (SW, AM upconversion)</td></tr>
<tr><td>1</td><td>1</td><td>0.5 to 10MHz (MW, LW)</td></tr>
</table>
The signal input to this pin must be capacitor coupled.
Input is disabled in Backup mode, after a power on reset, and in the PLL stopped state.</td></tr>
<tr><td>SUBPD</td><td>92</td><td>I/O</td><td>Sub-charge pump output and general-purpose input shared function port.
The IOS2 instruction is used for switching between the sub-charge pump output and general-purpose input functions.
• When used as the sub-charge pump output :
The sub-charge pump output function is set up with the IOS2 instruction.
A high-speed locking circuit can be formed by using this pin in conjunction with the main charge pump.
The sub-charge pump is controlled using the DZC instruction.
<table>
<tr><th>b3</th><th>b2</th><th>Operation</th></tr>
<tr><td>0</td><td>0</td><td>High impedance</td></tr>
<tr><td>0</td><td>1</td><td>Only operates when the PLL is unlocked (450kHz)</td></tr>
<tr><td>1</td><td>0</td><td>Only operates when the PLL is unlocked (900kHz)</td></tr>
<tr><td>1</td><td>1</td><td>Normal operation</td></tr>
</table>
• When used as a general-purpose input :
The general-purpose input function is set up with the IOS2 instruction.
Data is read from the port using the INR instruction.
This pin goes to the high-impedance state in Backup mode, after a power on reset, and in the PLL stopped state.</td><td> 
</td></tr>
<tr><td>INEO</td><td>91</td><td>I</td><td>Dedicated input port.
Data is read from the port using the INR instruction
Input is disabled in Backup mode.</td><td> 
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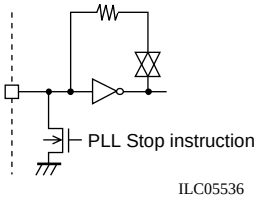
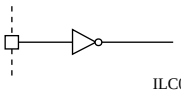
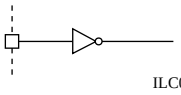
Pin name	Pin No.	I/O	Pin explanation	Equivalent circuit
HCTR	90	I	Universal counter and general-purpose input shared function input port. The IOS1 instruction is used for switching between the universal counter and general- purpose input functions. • When used for frequency measurement : The universal counter function is set up with the IOS1 instruction. The counter is controlled using UCS and UCC instructions. Since this pin functions as an AC amplifier in this mode, the input signal must be input with capacitor coupling. • When used as a general-purpose input pin : The general-purpose input function is set up with the IOS1 instruction. Data is read from the port using the INR (b0) instruction. Input is disabled in Backup mode. (The input pin will be pulled down.) The universal counter function is selected after a power on reset.	
LCTR	89	I	Universal counter (frequency or period measurement) and general-purpose input shared function input port. The IOS1 instruction is used for switching between the universal counter and general-purpose input functions. • When used for frequency measurement : The universal counter function is set up with the IOS1 instruction. Set up LCTR frequency measurement mode with the UCS instruction, and control operation with the UCC instruction. Since this pin functions as an AC amplifier in this mode, the input signal must be input with capacitor coupling. • When used for period measurement : The universal counter function is set up with the IOS1 instruction. Set up LCTR frequency measurement mode with the UCS instruction, and control operation with the UCC instruction. Since the bias feedback resistor is disconnected in this mode, the input signal must be input with DC coupling. • When used as a general-purpose input pin : The general-purpose input port function is set up with the IOS1 instruction. Data is read from the port using the INR (b1) instruction. Input is disabled in Backup mode. (The input pin will be pulled down.) The universal counter function (HCTR frequency measurement mode) is selected after a power on reset.	
$\overline{\text{SNS}}$	88	I	Voltage sense and general-purpose input shared function port. This input circuit is designed with a low input threshold voltage. • When used as a voltage sense input : The pin is used to test for power failures on the return from Backup mode. Application can test this condition using the internal SNS flip-flop. The SNS flip-flop can be tested with the TST instruction. (This usage requires external components, capacitors and resistors. For the sample application circuit, see the user's manual.) • When used as a general-purpose input port : When used as a general-purpose input port the pin state can be tested with the TST instruction. Unlike the other input ports, input to this pin is not disabled in Backup mode and after a power on reset. As a result, through currents must be taken into account when designing applications that use this pin as a general-purpose input.	
$\overline{\text{HOLD}}$	87	I	Power supply monitor (with interrupt function) This is designed with a high input threshold voltage. This pin is normally connected to the ACC line and used for power off detection. When a power off state is detected, the HOLDON flag and the hold interrupt request flag will be set. To enter Backup mode, execute a CKSTP instruction when the HOLD pin is low. Set this pin high to clear Backup mode.	

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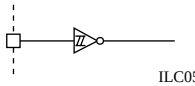
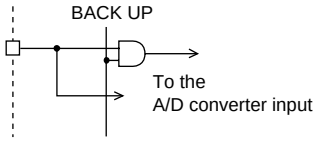
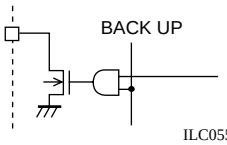
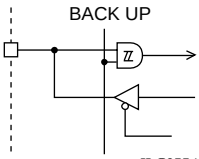
Pin name	Pin No.	I/O	Pin explanation	Equivalent circuit
$\overline{\text{RESET}}$	86	I	System reset pin. When the CPU is operating or in Halt mode, the system is reset when this pin is held low for at least one machine cycle. Execution starts with the PC pointing to location 0. At this time the SNS flip-flop is set. A low level must be applied for at least 50ms when power is first applied.	 ILC05540
PH0/ADI0 PH1/ADI1 PH2/ADI2 PH3/ADI3 PI0/ADI4 PI1/ADI5 PI2/ADI6 PI3/ADI7	85 84 83 82 81 80 79 78	I	General-purpose input and A/D converter input shared function ports. The IOS1 instruction is used to switch between the general-purpose input and the A/D converter input functions. • When used as general-purpose input ports : The general-purpose input port function is set up with the IOS1 instruction. (In bit units) • When used as A/D converter input pins : The A/D converter input port function is set up with the IOS1 instruction. (In bit units) The pin whose voltage is to be converted is specified with the IOS1 instruction, and the conversion is started with UCC instruction. Note : Since input is disabled for ports specified for the ADI function, executing an input instruction for such a port will always return a low level. Input is disabled in Backup mode. These ports are set up as general-purpose input ports after a power on reset.	 ILC05541
PJ0 PJ1 PJ2 PJ3	76 75 74 73	O	General-purpose output ports (high-voltage output) Since these are open-drain output circuits, external pull-up resistors are required. The internal transistors are turned off (resulting in a high-level output) in Backup mode and after a power on reset.	 ILC05542
PK0/INT0 PK1/INT1 PK2/INT2 PK3/INT3	72 71 70 69	I/O	General-purpose I/O and external interrupt shared function ports. The input formats are Schmitt inputs. The external interrupt function is enabled when the external interrupt enable flag is set. • When used as general-purpose I/O ports : The mode (input or output) is set in 1-bit units using the IOS1 instruction. • When used as external interrupt pins : The external interrupt functions are enabled by setting the corresponding external interrupt enable flag (INT0EN through INT3EN). Here, the pins must be set to input mode in advance. Input is disabled and the pins go to the high-impedance state in Backup mode. These ports are set up as general-purpose input ports after a power on reset.	 ILC05543

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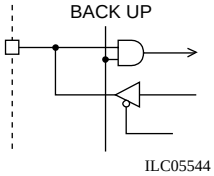
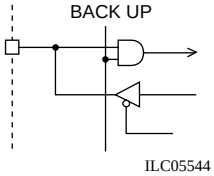
Pin name	Pin No.	I/O	Pin explanation	Equivalent circuit
PL0 to 3 PM0 to 3	68 to 61	I/O	General-purpose I/O ports The mode is switched between input and output with the IOS instruction. Input is disabled and the pins go to the high-impedance state in Backup mode. These ports are set up as general-purpose input ports after a power on reset.	
PN0/BEEP PN1 PN2 PN3	60 59 58 57	I/O	General-purpose I/O port and beep tone output shared function ports. The IOS2 instruction is used to switch between the general-purpose I/O port and the beep tone output functions. • When used as general-purpose I/O ports : The general-purpose I/O port function is set up with the IOS2 instruction. (Pins PN1 through PN3 are dedicated general-purpose output pins.) • When used as the beep tone output pin : The beep tone output function is set up with the IOS2 instruction. The frequency is set up with the BEEP instruction. When this pin is used as the beep tone output pin, executing an output instruction for this pin only sets the internal latch and has no influence on the output. Input is disabled and the pins go to the high-impedance state in Backup mode. These ports are set up as general-purpose input ports after a power on reset.	
PO0 to 3 PP0 to 3	56 to 49	I/O	General-purpose I/O ports The mode is switched between input and output with the IOS instruction. Input is disabled and the pins go to the high-impedance state in Backup mode. These ports are set up as general-purpose input ports after a power on reset.	
PQ0 to 3 PR0 to 3 PS0 to 3 PT0 to 3	48 to 41 38 to 33	I/O	General-purpose I/O ports. The mode is switched between input and output with the IOS instruction, and data is input with the INR instruction and output with the OUTR instruction. The SPB, RPB, TPT, and TPF instruction cannot be used with these ports. Input is disabled and the pins go to the high-impedance state in Backup mode. These ports are set up as general-purpose input ports after a power on reset.	
TEST1 TEST2	99 2		LSI test pins. These pins must be connected to GND.	

Concerning Differences from the LC723781N, 2N, 3N, 4 and 5 Mask Versions

Item	Mask version (LC723781N, 2N, 3N, 4 and 5)	OTP version (LC72F3781)
Design rule	0.35µ process	0.45µ process
ROM	Masked ROM structure	Flash ROM structure
Write mode	Not available	Available

Design Considerations

1) Although the electrical specifications are the same for the mask and OTP versions, differences may arise in the actual values for the threshold level of the input ports, output current of the output ports, input sensitivity, etc. Variations may also be found from lot to lot. It must therefore be kept in mind that if finished products are designed using the actual values of the samples, these variations may prevent the finished products from operating.
2) The undesirable radiation level is not listed among the specifications. Since differences may arise between the mask and OTP versions, this must be kept in mind when designing the finished products.

Concerning ROM Writing

1) The job of writing data onto the ROM in-house at SANYO Semiconductor is not currently supported.
2) The LC72F3781 circuit board must be requested as the data writing board.
3) The AF-9706 or AF-9708 made by Ando or the 1890A or 1881XP made by Minato is recommended as the ROM writer.

Example of Writing Data onto the on-chip Flash ROM of the LC72F3781

(using the AF-9706 or AF-9708)

I. Writing the data using the AF-9706 or AF-9708 (made by Ando) PROM programmer

1. ROMTYPE settings

ROMTYPE	→	Select [MAKER]	→	SET
	→	Select [SST]	→	SET
	→	Select [29EE010]	→	SET

2. Start/stop address settings

FUNCTION → 1 : Address setting mode

* The address that corresponds to the ROM capacity provided in the table below must be set as the stop address.

Type No.	ROM capacity	Stop address
LC723781N	40KB	9FFF
LC723782N	48KB	BFFF
LC723783N	64KB	FFFF
LC723784	96KB	17FFF
LC723785	128KB	1FFFF

3. Executing data erasure

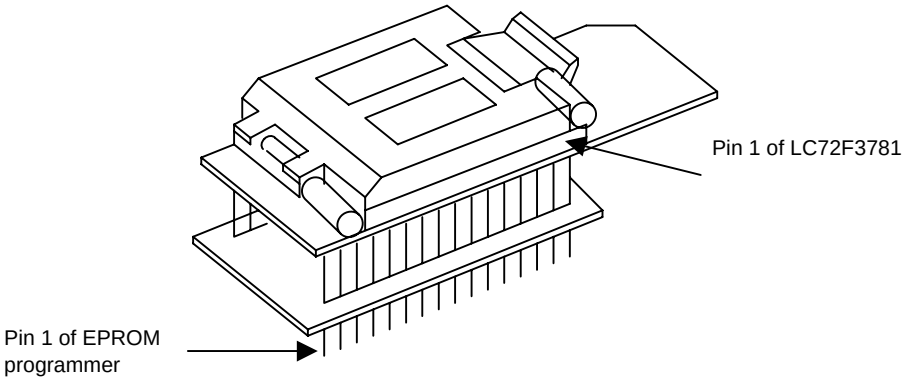
DEVICE → B → SET : For data erasure execution.

4. Executing data writing

DEVICE → F → SET : For program and verify execution.

II. Writing board

The writing board is shown in the figure below. The position of pin 1 must be checked before connecting to the EPROM programmer.



Note: The writing adapter has been changed.

To be used for the general-purpose EPROM programmer: Model LC72F3781-ADP-N EPROM programmer

Example of writing data onto the on-chip Flash ROM of the LC72F3781

(using the 1890A)

I. Data writing method

1. ROMTYPE settings

DEVICE → D734 → ENTRY → ENTRY : Device code [29EE010]

2. Start/stop address settings

EDIT → PAE : Address setting mode

<1> Since BEGIN ADD is displayed, 00000 → ENTRY
<2> Since END ADD is displayed, 1FFFF → ENTRY (128kbytes = 1FFFF)
<3> Since BUF ADD is displayed, 00000 → ENTRY

* The address that corresponds to the ROM capacity provided in the table below must be set as the stop address.

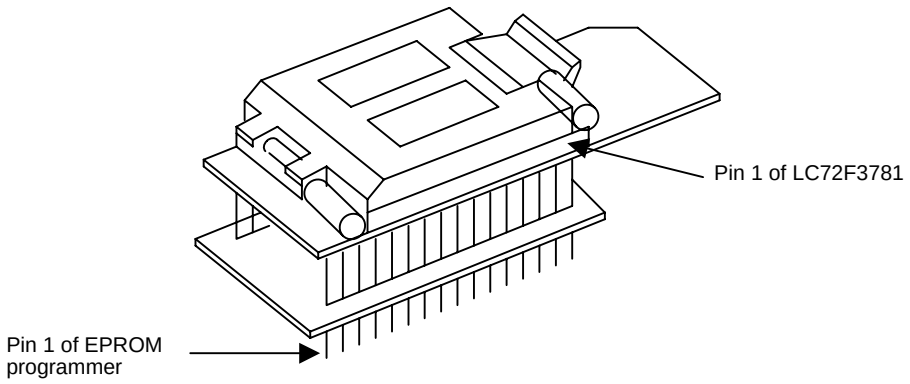
Type No.	ROM capacity	Stop address
LC723781N	40KB	9FFF
LC723782N	48KB	BFFF
LC723783N	64KB	FFFF
LC723784	96KB	17FFF
LC723785	128KB	1FFFF

3. Executing data writing

PROG → PAE : For program and verify execution.

II. Writing board

The writing board is shown in the figure below. The position of pin 1 must be checked before connecting to the EPROM programmer.



Note: The writing adapter has been changed.

To be used for the general-purpose EPROM programmer: Model LC72F3781-ADP-N EPROM programmer

This catalog provides information as of September, 2006. Specifications and information herein are subject to change without notice.