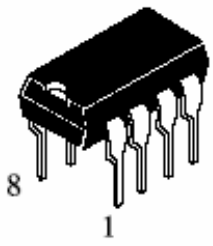
PWM Power Control IC with Interference Suppression

IL6083

Description

The designed IC is based on bipolar technology for the control of an N-channel power MOSFET used as a high-side switch. The IC is ideal for use in brightness control systems (dimming) of lamps, for example, in dashboard applications.



IL6083N DIP-8
T_A = –40 ~ +110°C

Features

- Protection Against Short-circuit, Load Dump Overvoltage and Reverse VS
- Duty Cycle 18 to 100% Continuously
- Internally Reduced Pulse Slope of Lamp's Voltage
- Interference and Damage Protection
- Charge-pump Noise Suppression
- Ground-wire Breakage Protection

Pin Configuration

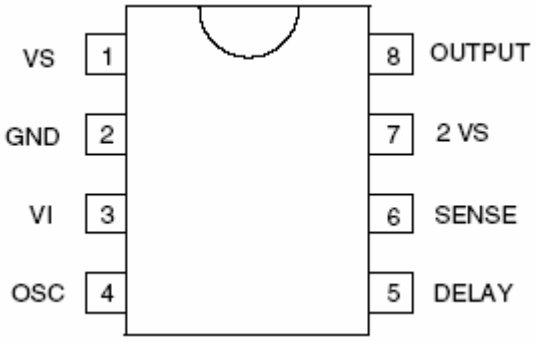


Figure 1.

Pin	Symbol	Pin Description
01	**Vs**	Supply voltage
02	**GND**	IC ground
03	**Vi**	Control input (duty cycle)
04	**Osc**	Oscillator
05	**Delay**	Short-circuit protection delay
06	**Sense**	Current sensing
07	**2Vs**	Voltage doubler
08	**Output**	Output

Block diagram with External Circuit

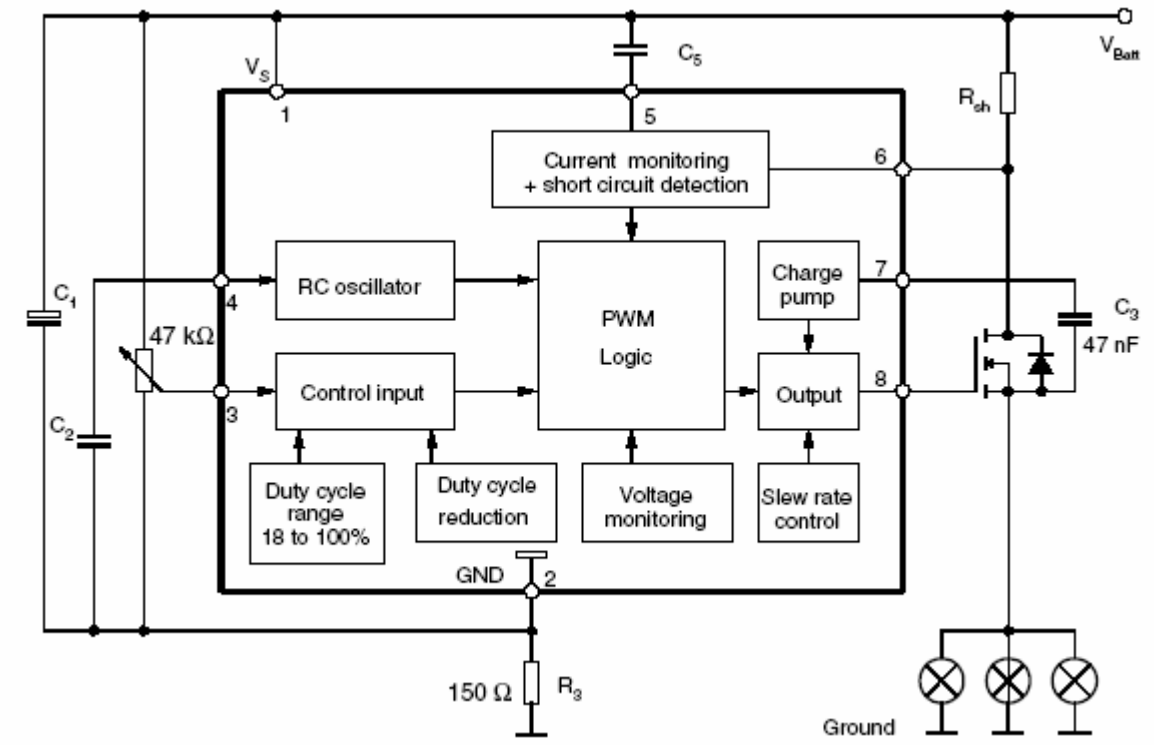


Figure 2.

Maximum and Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter, Symbol, Unit	Maximum Ratings		Absolute Maximum Ratings	
	min	max	min	Max
Supply voltage Vbatt, V	9.0	25		32.5
Storage temperature Tstg, °C			-55	+125
Ambient operation temperature range T_A, °C	-40	+110	-55	+125
Junction maximum temperature TJ(max), °C				+150
Temperature resistance junction – ambient Rth j-a, =120°C/W				

Functional Description

Pin 1, Supply Voltage, V_S or V_{Batt}

Overvoltage Detection

Stage 1

If overvoltages of V_{Batt} > 20 V (typically) occur, the external transistor is switched off, and switched on again at V_{Batt} < 18.5 V (hysteresis).

Stage 2

If V_{Batt} > 28.5 V (typically), the voltage limitation of the IC is reduced from V_S = 26 V to 20 V. The gate of the external transistor remains at the potential of the IC ground, thus producing voltage sharing between FET and lamps in the event of overvoltage pulses (e.g. , load dump). The short - circuit protection is not in operation.
At V_{Batt} approximately < 23 V, the overvoltage detection stage 2 is switched off. Thus, during overvoltage detection stage 2, the lamp voltage V_{lamp} is calculated as follows:

$V_{Lamp} = V_{Batt} - V_S - V_{GS}$
V_S = supply voltage of the IC at overvoltage detection stage 2
V_{GS} = gate - source voltage of the FET

Undervoltage Detection

In the event of voltages of approximately V_{Batt} < 5.0 V, the external FET is switched off and the latch for short-circuit detection is reset.
A hysteresis ensures that the FET is switched on again at approximately $V_{Batt} \geq 5.4$ V.

Pin 2, GND

Ground-wire Breakage
To protect the FET in the case of ground-wire breakage, a 1 MΩ resistor between gate and source is recommended to provide proper switch-off conditions.

Pin 3, Control Input

The pulse width is controlled by means of an external potentiometer (47 kΩ). The characteristic (angle of rotation/duty cycle) is linear. The duty cycle can be varied from 18 to 100%. It is possible to further restrict the duty cycle with the resistors R_1 and R_2 (see Figure 4).

In order to reduce the power dissipation of the FET and to increase the lifetime of the lamps, the IC automatically reduces the maximum duty cycle at pin 8 if the supply voltage exceeds V_2 = 13 V. Pin 3 is protected against short-circuit to V_{Batt} and ground ($V_{Batt} \leq 16.5$ V).

Pin 4, Oscillator

The oscillator determines the frequency of the output voltage. This is defined by an external capacitor, C_2. It is charged with a constant current, I, until the upper switching threshold is reached. A second current source is then activated which taps a double current, 2 x I, from the charging current. The capacitor, C_2, is thus discharged at the current, I, until the lower switching threshold is reached. The second source is then switched off again and the procedure starts once more.

Example for Oscillator

Frequency Calculation

Switching thresholds

V_{T100} = High switching threshold (100% duty cycle)

$V_{T100} = V_S \times \alpha_1 = (V_{Batt} - I_S \times R_3) \times \alpha_1$

$V_{T<100}$ = High switching threshold (< 100% duty cycle)

$V_{T<100} = V_S \times \alpha_2 = (V_{Batt} - I_S \times R_3) \times \alpha_2$

V_{TL} = Low switching threshold

$V_{TL} = V_S \times \alpha_3 = (V_{Batt} - I_S \times R_3) \times \alpha_3$

where

α_1, α_2 and α_3 are fixed values

Calculation Example

The above mentioned threshold voltages are calculated for the following values given in the data sheet.

V_{Batt} = 12 V, I_S = 4 mA, R_3 = 150 Ω, α_1 = 0.7, α_2 = 0.67 and α_3 = 0.28

V_{T100} = (12 V - 4 mA x 150 Ω) x 0.7 ≈ 8 V

$V_{T<100}$ = 11.4 V x 0.67 = 7.6 V

V_{TL} = 11.4 V x 0.28 = 3.2 V

Oscillator Frequency

3 cases have to be distinguished

1. f_1 for duty cycle = 100%, no slope reduction with capacitor C_4 (see Figure 4)

$$f_1 = \frac{I_{OSC}}{2 \times (V_{T100} - V_{TL}) \times C_2}, \text{ where } C_2 = 68\ nF,\ I_{OSC} = 45\ \mu A$$

f_1 = ... = 75 Hz

2. f_2 for duty cycle < 100%, no slope reduction with capacitor C_4 . For a duty cycle of less than 100%, the oscillator frequency, f, is as follows:

$$f_2 = \frac{I_{OSC}}{2 \times (V_{T<100} - V_{TL}) \times C_2}, \text{ where } C_2 = 68\ nF,\ I_{OSC} = 45\ \mu A$$

f_2 = ... = 69 Hz

3. f_3 with duty cycle < 100% with slope reduction capacitor C_4 (see “Output Slope Control”)

Electrical parameters are given for temperature range from minus 40 to + 110° C and V_{batt}. From 9 to 16,5V. Operation is guaranteed for Vbatt from 6 to 9V. All electrical parameters are specified relatively to “common” output (02).

$$f_3 = \frac{I_{osc}}{2 \times (V_{T<100} - V_{TL}) \times C_2 + 2V_{Batt} \times C_4}$$

where C_2 = 68 nF, I_{OSC} = 45 µA, C_4 = 1.8 nF

f_3 = ... = 70 Hz

By selecting different values of C_2 and C_4, it is possible to have a range of oscillator frequencies from 10 to 2000 Hz as shown in the data sheet.

Output Slope Control

The slope of the lamp voltage is internally limited to reduce radio interference by limitation of the voltage gain of the PWM comparator.
Thus, the voltage rise on the lamp is proportional to the oscillator voltage increase at the switchover time according to the equation.

$$dV_\vartheta/d_t = \alpha_4 \times dV_4/d_t = 2 \times \alpha_4 \times f \times (\alpha_2 - \alpha_3) \times (V_{Batt} - I_S \times R_3)$$

when

$f = 75\ Hz$, $V_{TX} = V_T < 100$ and $\alpha_4 = 63$

then

$$dV_\vartheta/d_t = 2 \times 63 \times 75\ Hz \times (0.67 - 0.28) \times (12\ V - 4\ mA \times 15\ \Omega) = 42\ V/ms$$

Via an external capacitor, C_4, the slope can be further reduced as follows:

$$dV_\vartheta/d_t = I_{OSC}/(C_4 + C_2/\alpha_4)$$

when

$I_{OSC} = 45\ \mu A$, $C_4 = 1.8\ nF$, $C_2 = 68\ nF$ and $\alpha_4 = 63$

then $dV_\vartheta/d_t = 45\ \mu A/(1.8\ nF + 68\ nF/63) = 15.6\ V/ms$

To damp oscillation tendencies, a resistance of 100Ω in series with capacitance C_4 is recommended.

Interference Suppression

- "On-board" radio reception according to VDE 0879 part 3/4.81
- Test conditions refering to Figure 3
- Application circuit according to Figure 1 or Figure 4
- Load: nine 4 W lamps in parallel
- Duty cycle = 18%
- V_{Batt} = 12 V
- f_{Osc} = 100 Hz

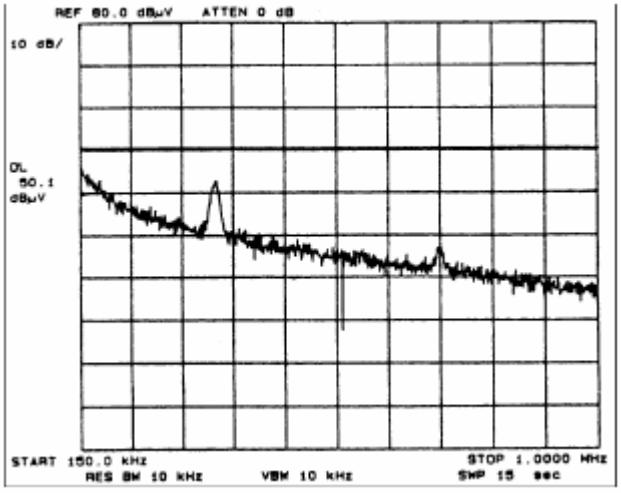


Figure 3. Voltage Spectrum of On-board Radio Reception

Pins 5 and Pin 6, Short-circuit Protection and Current Sensing

Short-circuit Detection and Time Delay, t_d

The lamp current is monitored by means of an external shunt resistor. If the lamp current exceeds the threshold for the short-circuit detection circuit ($V_{T2} \approx 90$ mV), the duty cycle is switched over to 100% and the capacitor C5 is charged by a current source of $I_{ch} - I_{dis}$. The external FET again is switched off after the cut-off threshold (V_{T5}) is reached. Switching on the FET again is possible after a power-on reset only. The current source, I_{dis}, ensures that the capacitor C_5 is not charged by parasitic currents.

The time delay, td, is calculated as follows:

$t_d = C_5 \times V_{T5}/(I_{ch} - I_{dis})$

With $C_5 = 100$ nF and $V_{T5} = 10.4$ V, $I_{ch} = 13$ µA, $I_{dis} = 3$ µA, the time delay is as follows:

$t_d = 100\ nF \times 10.4\ V/(13\ \mu A - 3\ \mu A)$

$t_d = 104$ ms

Current Limitation

The lamp current is limited by a control amplifier to protect the external power transistor. The voltage drop across the external shunt resistor acts as the measured variable. Current limitation takes place for a voltage drop of $V_{T1} \approx 100$ mV. Owing to the difference $V_{T1} - V_{T2} \approx 10$ mV, it ensures that current limitation occurs only when the short-circuit detection circuit has responded.
After a power-on reset, the output is inactive for half an oscillator cycle. During this time, the supply voltage capacitor can be charged so that current limitation is guaranteed in the event of a short-circuit when the IC is switched on for the first time.

Pins 7 and 8, Charge Pump and Output

Pin 8 (output) is suitable for controlling a power MOSFET. During the active integration phase, the supply current of the operational amplifier is mainly supplied by the capacitor C_3 (bootstrapping). In addition, a trickle charge is generated by an integrated oscillator ($f_7 \approx 400$ kHz) and a voltage doubler circuit. This permits a gate voltage supply at a duty cycle of 100%.

Table of Electrical Parameters

T_{amb} = -40°C to +110°C, V_{Batt} = 9 to 16.5 V, (basic function is guaranteed between 6.0 V to 9.0 V) reference point ground, unless otherwise specified (see Figure 2). All other values refer to pin GND (pin 2).

Parameter	Symbol	Test Conditions	Rate			Unit
			min	Typ.	max	
Pin 1						
Current Consumption	Is				7.9	mA
Supply voltage	V_{batt}	Overvoltage Detection, stage 1			25	V
Stabilized voltage	V_S	Is=10mA	24.5		27.0	V
Level of the lowered battery voltage	V_{batt}	Switching on Switching off	4.4 4.8	5.0 5.4	5.6 6.0	V
Battery Overvoltage Detection						
Stage 1	V_{batt}	Switching on Switching off	18.3 16.7	20.0 18.5	21.7 20.3	V
Stage 2 Detection stage 2	V_{batt}	Switching on Switching off	25.5 19.5	28.5 23.0	32.5 26.5	V
Stabilized voltage	V_S	Is=30mA	18.5	20.0	21.5	V
Short- Circuit Protection, Pin 6						
short-circuit current limitation	V_{T1}	$V_{T1} = V_S - V_6$	85	100	120	mV
Short circuit voltage	V_{T2}	$V_{T2} = V_S - V_6$	75	90	105	mV
	$V_{T1} - V_{T2}$	$V_{T2} = V_S - V_6$	3	10	30	
Delay Timer Short-circuit Detection, Vbatt = 12.0V, Pin 5						
Switch off threshold	V_{T5}	$V_{T5} = V_S - V_5$	10.2	10.4	10.6	V
Charge current	I_{ch}			13		uA
Dicharge current	I_{dis}			3		uA
Capacitance current	I_5	$I_5 = I_{ch} - I_{dis}$	5	10	15	mA
Voltage doubler, Pin 7						
Voltage	V_7	Duty cycle 100%	$2V_S$			V
Oscillator frequency	f_7		280	400	520	kHz
Internal voltage limitation	V_7	I_7=5mA (whichever is lower)	26.0 V_{S+14}	27.5 V_{S+15}	30.0 V_{S+16}	V
Edge rate	α_4	$dV_8/dt = \alpha_4\ dV_4/dt$ dV_8/dt_{max}	53	63	72 130	V/ms

Parameter	Symbol	Test Conditions	Rate			Unit
			min	Type	max	
Gate Output , Pin 8						
Voltage	V_8	Low level	0.35	0.70	0.95	V
		Vbatt = 16.5V Tamb = 110° C, R_3=150Ω			1.5*	
		High level, duty cycle 100%		V_7		
Current,	I_8	V_8 = low level	1.0			mA
		V_8 = high level, $I_7 > \|I_8\|$	-1.0			
Duty cycle	$t_{рмин}$ /T	Min: C_2=68nF	15	18	21	%
		Max: V_{batt} ≤12.4V,	100			
		V_{batt} = 16.5V, C_2=68nF	65	73	81	
Oscillator, Pin 4						
Frequency	f		10		2000	Hz
Threshold cycle	α_1	V_8 = High, $\alpha_1 = \frac{V_{T100}}{V_S}$	0.68	0.7	0.72	
Upper	α_2	V_8 = Low, $\alpha_2 = \frac{V_{T<100}}{V_S}$	0.65	0.67	0.69	
Lower	α_3	$\alpha_3 = \frac{V_{TL}}{V_S}$	0.26	0.28	0.3	
Oscillator current	± I_{OSC}	V_{batt}=12.0 V	34	45	54	uA
Frequency	f	C_4 is open, C_2=68nF, duty cycle=50%	56	75	90	Hz

***** Reference point is battery ground

Application Circuit

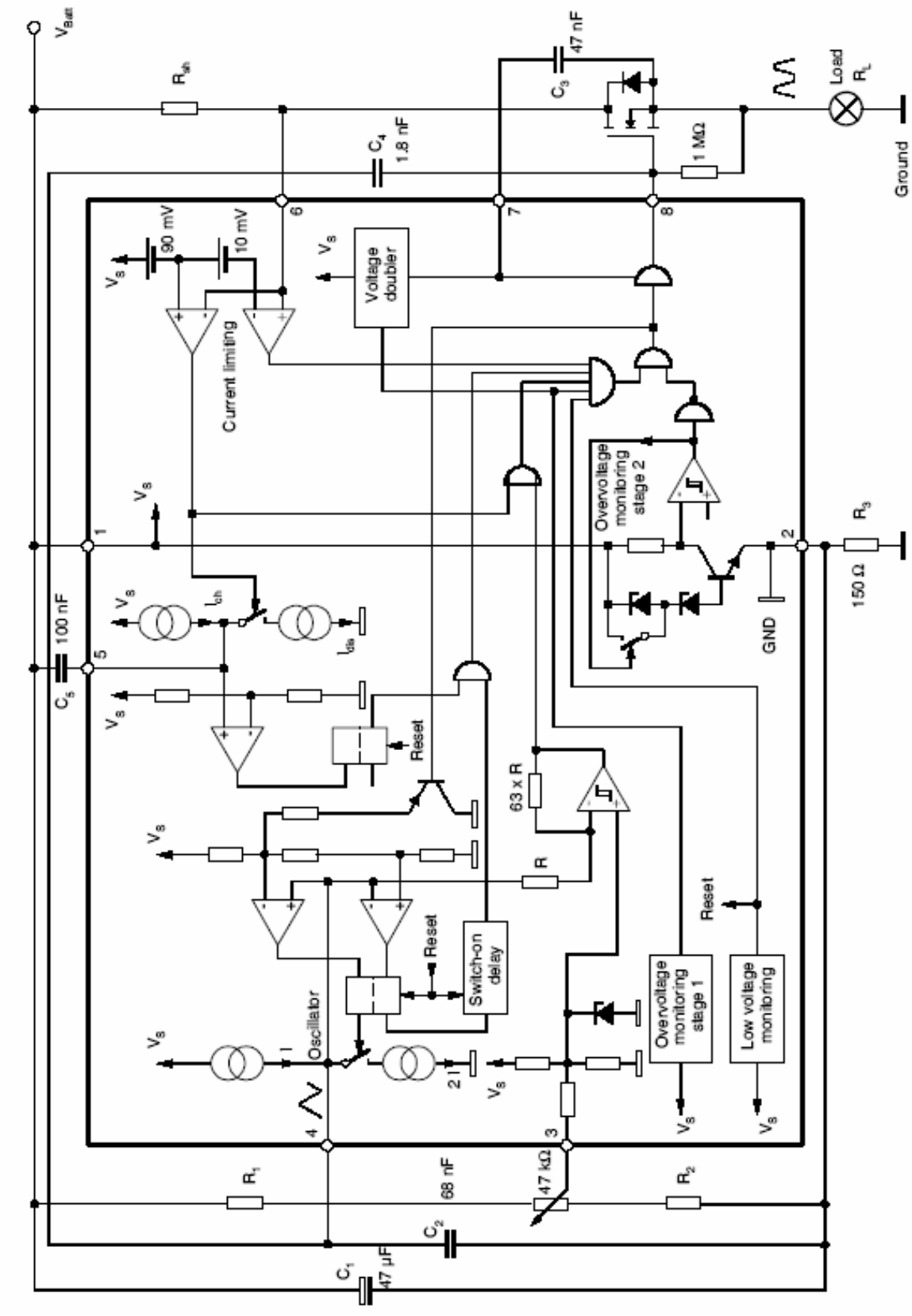
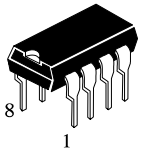
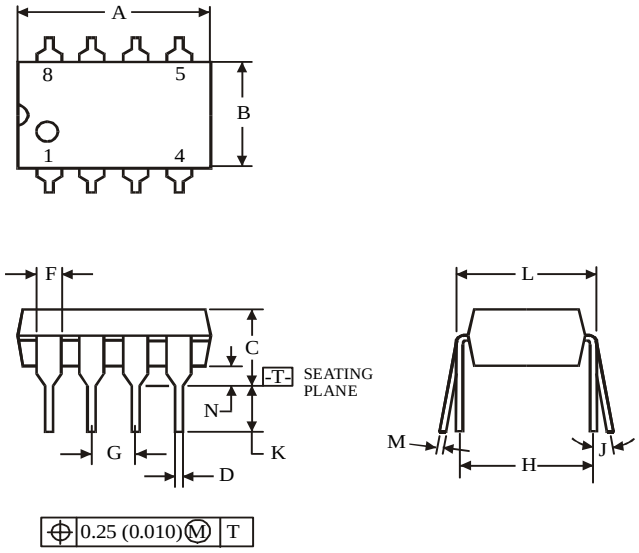


Figure 4. Application Circuit

Package Outline Dimension
DIP-8

N SUFFIX PLASTIC DIP
(MS – 001BA)





	Dimension, mm	
Symbol	**MIN**	**MAX**
A	8.51	10.16
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

NOTES:

1. Dimensions “A”, “B” do not include mold flash or protrusions.
   Maximum mold flash or protrusions 0.25 mm (0.010) per side.