e88C312 DATA CONTROLLER

An Overview

The e88C312 data controller controls the interface between the CPU data bus (D<31:0>), the local or main memory data bus (MD<31:0>), and the local system data bus (LSD<15:0>). The local system data bus can be connected to the AT data bus (SD<15:0>) through external buffers or directly bypassing the external buffers. In the latter case, the local system data bus LSD<15:0> is the same as the AT data bus SD<15:0>. The lower byte of the local system data bus (LSD<7:0>) is also called the peripheral data bus and is connected to all on-board peripherals. The BIOS EPROM (16-bit) resides on the LSD<15:0> bus. In the case where a single 8-bit EPROM is used in the system, the BIOS EPROM resides on the LSD<7:0> bus.

The e88C312 data buffer also implements byte alignment and byte swapping for data transfers where the source and target are of different bus widths. In order to maintain data integrity, the e88C312 generates a parity bit for each byte of data written into local memory. When data is read from the local memory, the e88C312 regenerates the parity bits for each data byte and compares then against the parity bits read from the memory array. If there is a mismatch indicating a parity error condition, the e88C312 will activate an error signal (PARERR) to prompt the e88C311 to take proper actions.

In order to simplify on-board I/O port designs, two serial port selects (SERCS1, SERCS2-, one parallel port select (PARCS-) and two software programmable chip selects (PGCS0-, PGCS1-) are implemented in the e88C312. In addition, the e88C312 also provides the math-coprocessor detection and interface logic for the Intel 80387 and the Weitek WTL3167.

7. FUNCTIONAL DESCRIPTION

The e88C312 can be divided into the following functional modules as shown in the block diagram.

Action Decode and Control
Data Transfer Logic
Parity Handler
Timer Clock
Math Coprocessor Interface Logic

7.1 .e88C312 Action Decode and Control

The activities within the e88C312 are initiated by the 5-bit action codes (DBAM<4:0>) which are generated by the e88C311. The action codes determine what the current bus cycle is and prompts the e88C312 to control the direction of data flow by decoding DBAM<4:0> together with HLDA1, AEN1, XBHE-, XA1, XA0 and REF-. Table 1.1 below summarizes the bus cycle definition. The detailed definition of the action codes are given in Tables 1.2 through 1.4.

The SDIR1 and SDIR0 outputs are decoded to support the on-board optional bidirectional buffers which interface the local I/O bus (LSD<15:0>) to the AT SD<15:0> bus. When high, these outputs direct the local bus to the AT bus and vice versa when they are low. In the absence of these bidirectional buffers, SD<15:0> outputs may be directly connected to the AT bus. The BDIR output is active (high) during CPU cycles, DMA cycles or Refresh cycles and drives the XA<16:1> address bus onto the system address bus SA<16:1>. During Master cycles, the BDIR output is low and the XA<16:1> address bus is driven by the system address bus SA<16:1>.

7.1.1 Port Select Logic

Embedded in the Action Decode and Control module is the port select logic. The outputs associated with this sub-module are the peripheral chip selects: CS8042-, SERCS1-, SERCS2-, PARCS-, PGCS1-, PGCS0- and the Real Time Clock Address Strobe signal RTCAS. The on-chip implementation of these outputs eliminates the necessity of on-board glue logic generally required for external decoding of these functions. In addition, two programmable chip selects, PGCS1- and PGCS0- are implemented to provide greater flexibility for the system/board design. These chip selects can be defined through the e88C311 configuration registers.

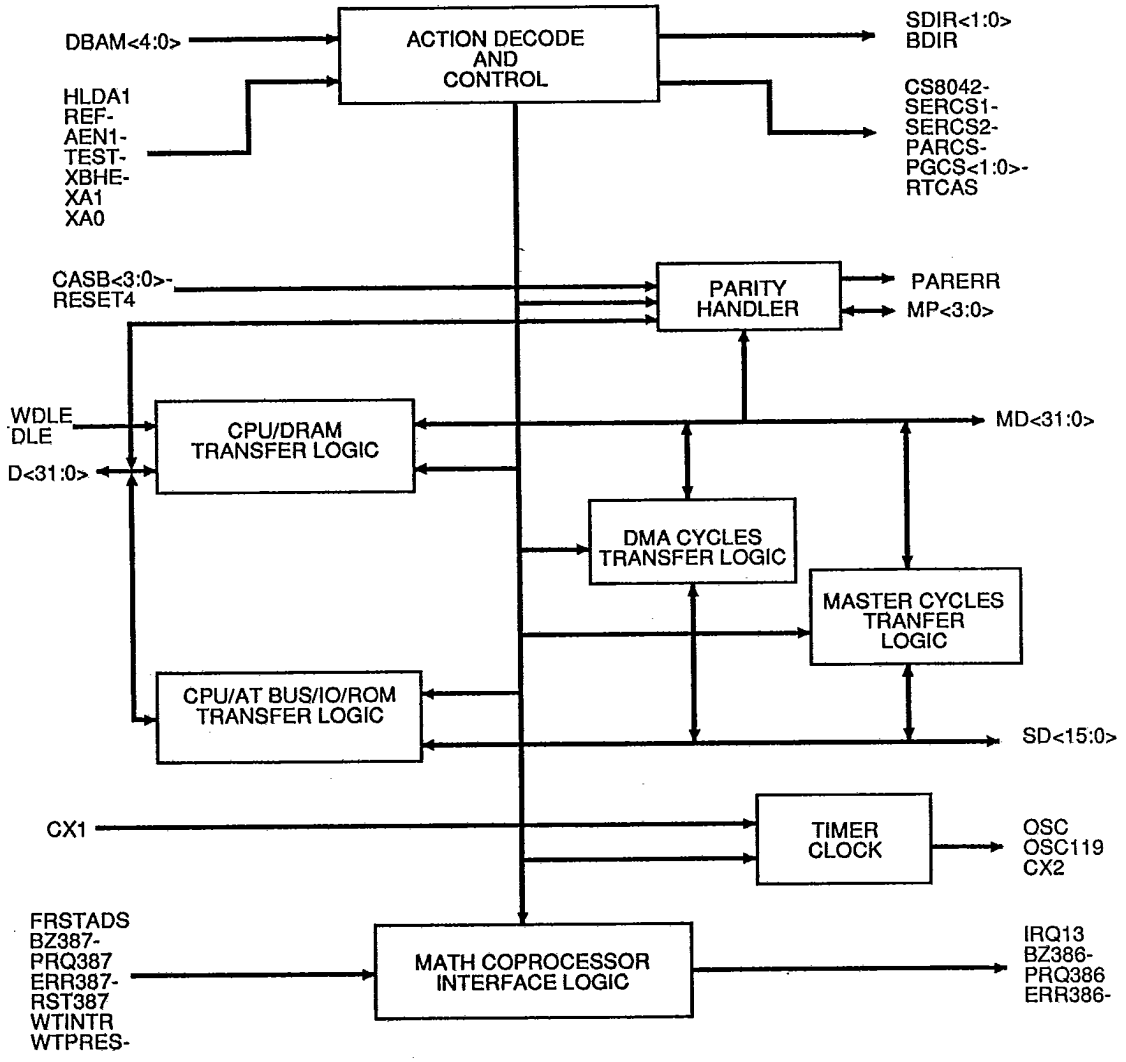


Figure 7-1. e88C312 Block Diagram

Table 7-1. Bus Cycle Definition (DBAM <4:0> in HEX format)

HLDA1	DBAM<4:0>	Bus Cycle	Source	Dest.
X	00	DEFAULT	-	-
X	02 - 03	RESERVED	-	-
0	01	CPU Read Local Memory	MD	D
0	04 - 07	CPU Read Local I/O or ROM	SD	D
0	08	CPU Write Local Memory	D	MD
		CPU Write AT	D	SD
0	09 - 0B	CPU Write AT or Local I/O	D	SD
0	0C - 0F	CPU Read AT	SD	D
1	01	Master Write Local Memory or	SD	MD
		Master Write Local I/O, AT Memory, AT I/O	-	-
1	04 - 05	Master Read Local Memory	MD	SD
1	06	Master Read Local ROM or I/O	-	-
1	07	Master Read AT Memory or AT I/O	-	-
1	08	DMA Write Local Memory or	SD	MD
		8-bit DMA Write AT Memory High Byte		
		(Byte-Swap Operation)	SD<7:0>	SD<15:8>
1	09	DMA Read Local ROM	-	-
1	0A	DMA Read AT Memory	-	-
1	0B	8-bit DMA Read AT Memory High Byte		
		(Byte-Swap Operation)	SD<15:8>	SD<7:0>
1	0C - 0F	DMA Read Local Memory	MD	SD
X	10 - 16	CPU Write Peripherals	D	SD
X	17	CPU Write, Clear 387 Busy	-	-
X	18 - 1D	CPU Read Peripherals	SD	D
X	1E	CPU Read Configuration Register 4Dh	e88C312	D & SD
X	1F	CPU Write Configuration Register 49h	D	SD

Note: (-) In the Source and Destination columns, this indicates that e88C312 does not handle the data transfer, i.e., either there is no data transfer involved, or the transfer takes place external to the e88C312.

(X) Denotes Don't Care.

Table 7-2. Action Mode Codes For CPU Cycles

HLDA1	DBAM<4:0>	CYCLE	OPERATION
0	00000	DEFAULT	
0	00001	CPU READ	LOCAL MEMORY (32-BIT)
0	00010	-	(RESERVED)
0	00011	-	(RESERVED)
0	00100	CPU READ	LOCAL ROM (16-BIT) LOW WORD LOCAL ROM (8-BIT) BYTE 0 LOCAL I/O (8-BIT) BYTE 0
0	00101	CPU READ	LOCAL ROM (8-BIT) BYTE 1 LOCAL I/O (8-BIT) BYTE 1
0	00110	CPU READ	LOCAL ROM (16-BIT) HIGH WORD LOCAL ROM (8-BIT) BYTE 2 LOCAL I/O (8-BIT) BYTE 2
0	00111	CPU READ	LOCAL ROM (8-BIT) BYTE 3 LOCAL I/O (8-BIT) BYTE 3
0	01000	CPU WRITE	32-BIT 16-BIT LOW WORD 8-BIT BYTE 0
0	01001	CPU WRITE	8-BIT BYTE 1
0	01010	CPU WRITE	16-BIT HIGH WORD 8-BIT BYTE 2
0	01011	CPU WRITE	8-BIT BYTE 3
0	01100	CPU READ	16-BIT AT BUS LOW WORD 8-BIT AT BUS BYTE 0
0	01101	CPU READ	8-BIT AT BUS BYTE 1
0	01110	CPU READ	16-BIT AT BUS HIGH WORD 8-BIT AT BUS BYTE 2
0	01111	CPU READ	8-BIT AT BUS BYTE 3

Table 7-3. Action Mode Codes For MASTER/DMA Cycles

HLDA1	DBAM<4:0>	CYCLE	OPERATION
1	00000	DEFAULT	
1	00001	MASTER WRITE	LOCAL MEMORY (16-BIT) LOCAL I/O AT BUS MEMORY (16-/8-BIT) AT BUS I/O (16-/8-BIT)
1	00010		(RESERVED)
1	00011		(RESERVED)
1	00100	MASTER READ	LOCAL MEMORY LOW WORD
1	00101	MASTER READ	LOCAL MEMORY HIGH WORD
1	00110	MASTER READ	LOCAL 16-BIT ROM (16-BIT) LOCAL 8-BIT ROM (8-BIT) LOCAL I/O (8-BIT)
1	00111	MASTER READ	16-BIT AT BUS MEMORY, I/O 8-BIT AT BUS MEMORY, I/O
1	01000	DMA WRITE	LOCAL MEMORY 16-BIT AT BUS MEMORY 8-BIT AT BUS MEMORY
1	01001	DMA READ	LOCAL 16-BIT ROM WORD LOCAL 16-BIT ROM LOW BYTE LOCAL 8-BIT ROM
1	01010	DMA READ	16-BIT AT BUS MEMORY WORD 16-BIT AT BUS MEMORY LOW BYTE 8-BIT AT BUS MEMORY
1	01011	DMA READ	16-BIT AT BUS MEMORY HIGH BYTE
1	01100	DMA READ	LOCAL MEMORY LOW WORD LOCAL MEMORY BYTE 0
1	01101	DMA READ	LOCAL MEMORY BYTE 1
1	01110	DMA READ	LOCAL MEMORY HIGH WORD LOCAL MEMORY BYTE 2
1	01111	DMA READ	LOCAL MEMORY BYTE 3

Table 7-4. Extended Action Mode Codes

HLDA1	DBAM<4:0>	CYCLE	OPERATION
X	10000	CPU WRITE	8042 CHIP SELECT
X	10001	CPU WRITE	PARALLEL PORT 1
X	10010	CPU WRITE	SERIAL PORT 1
X	10011	CPU WRITE	SERIAL PORT 2
X	10100	CPU WRITE	PROGRAMMABLE CHIP SELECT 0
X	10101	CPU WRITE	PROGRAMMABLE CHIP SELECT 1
X	10110	CPU WRITE	REAL-TIME CLOCK ADDRESS STROBE
X	10111	CPU WRITE	CLEAR 80387 BUSY
X	11000	CPU READ	8042 CHIP SELECT
X	11001	CPU READ	PARALLEL PORT 1
X	11010	CPU READ	SERIAL PORT 1
X	11011	CPU READ	SERIAL PORT 2
X	11100	CPU READ	PROGRAMMABLE CHIP SELECT 0
X	11101	CPU READ	PROGRAMMABLE CHIP SELECT 1
X	11110	CPU READ	CONFIGURATION REGISTER 4Dh
X	11111	CPU WRITE	CONFIGURATION REGISTER 49h

7.2 Data Transfer Modules

As shown in the block diagram, there are 4 data transfer modules. Each of these is controlled by the internal control signals generated by the Action Decode Control module. The description of each of these modules is given below.

7.2.1 CPU/DRAM Data Transfer Module

The CPU/DRAM Data Transfer Module controls the data flow between the CPU and the main memory. During memory write, CPU data is latched by WDLE and driven onto the MD bus. During memory read, the memory data is latched by DLE and driven onto the D bus. The data flow involved is shown in Figure 7-2.

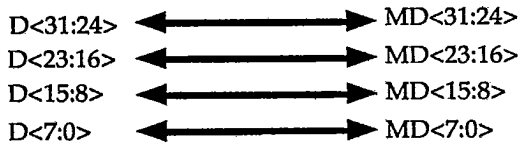


Figure 7-2. CPU/DRAM Data Transfer

7.2.2 CPU/AT/IO/ROM Data Transfer Module

The CPU/AT-BUS/IO/ROM Data Transfer Module controls data flow between the CPU and the AT-Bus, peripherals and system BIOS ROM. The CPU data is latched by WDLE during CPU write and the SD data is latched by DLE during CPU read.

The data flows for 16-bit transfers are shown in Figure 7-3.

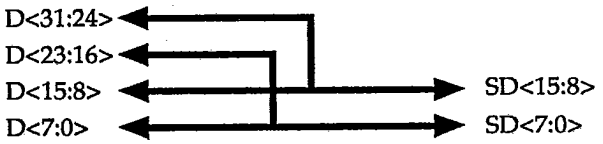


Figure 7-3. CPU/AT/IO/ROM 16-bit Data Transfer

The data flows for 8-bit transfers are shown in Figure 7-4.

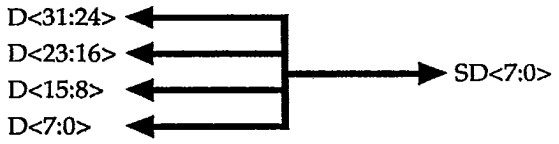


Figure 7-4. CPU/AT/IO/ROM 8-bit Data Transfer

7.2.3 DMA CYCLES Transfer Module

The DMA Cycles Transfer Module controls the data flow between the local SD bus and the main memory MD bus as well as between the local SD bus and the AT SD bus as shown in Figures 7-5A and 7-5B. During main memory read, the memory data is latched by DLE. The data transfer between an 8-bit local I/O and 16-bit AT memory is accomplished through a byte-swap mechanism as shown in Figure 7-5C.

Data flows for 16-bit DMA transfers are as follows:

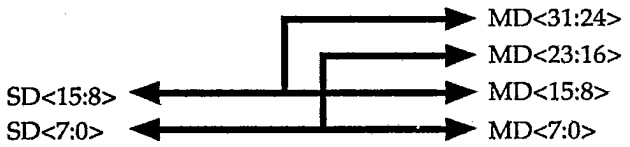


Figure 7-5A. 16-bit DMA Memory Cycles Transfer

Data flows for 8-bit DMA transfers are as follows:

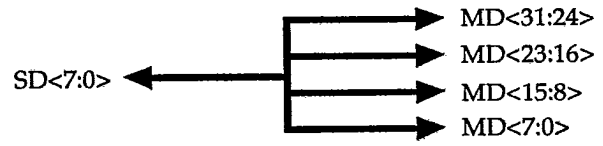


Figure 7-5B. 8-bit DMA Memory Cycles Transfer

AT memory transfer:

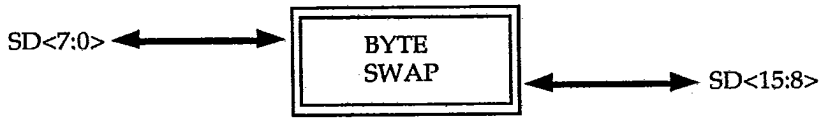


Figure 7-5C. Byte Swapping Between 8-bit local I/O and 16-bit AT Memory

7.2.4 MASTER CYCLES Transfer Module

The MASTER Cycles Transfer Module controls the data flow between the AT bus (SD) and the main memory bus (MD). During memory read, the memory data is latched by DLE. The memory write data is unlatched. The data flow involved is shown in Figure 7-6.

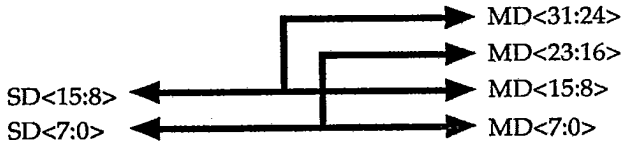


Figure 7-6 Memory Cycles Transfer

7.3 Parity Handler

In order to maintain data integrity, the e88C312 generates a parity bit for each byte of data written to local memory and also provides parity check to detect any mismatch whenever data is read from local memory.

During the local memory write cycle, source data (CPU, DMA or Master) is passed to the MD bus as well as to the parity generation logic. The parity generator generates one parity bit for each byte of write data and passes this bit to the memory parity outputs MP<3:0>. The memory write data (MD<31:0>) together with the parity bits (MP<3:0>) are written into the DRAM when the proper row address and/or column address strobes are issued by e88C311.

During the local memory read cycle, memory data MD<31:0> and memory parity bits MP<3:0> are latched into the e88C312. The MD data is redirected to the proper destinations (CPU, DMA or Master) as well as to the parity check logic. The parity check logic will regenerate new parity bits from the memory read data, one bit per byte, and compare them with the read memory parity bits. Bytes with a parity error will be latched into a 4-bit internal indexed register (4Dh). The content of this register can be read later for error diagnosis (action code DBAM<4:0> = 1Eh). Refer to Table 1.5 for the definition of register 4Dh.

The byte parity error bits are OR'ed together and latched to generate the parity error signal PARERR. When PARERR is high, it indicates a parity error has been detected. This will close the 4Dh latch and keep it closed until a reset condition has occurred or until a parity clear command (action code DBAM<4:0> = 1Fh) is issued. The e88C311 can constantly monitor the PARERR signal if the Parity Check Enable bit in register 49h is enabled. Upon detecting PARERR, it will latch the address where parity error occurred. e88C311 then generates an NMI (if it is enabled) to the CPU and executes an I/O operation to read register 4Dh in order to identify the byte(s) that have caused the error.

7.4 Timer Clock

The e88C312 also generates the AT bus color reference oscillator signal OSC. This output is a 14.31818 MHz clock signal. Another clock signal is generated by dividing the above signal by 12 to derive the OSC119 signal. This is used by the on-board Timer/Counter logic to perform the following functions under software control: timer, rate generator, pulse or square wave generators, and strobe signal. It is also used in the e88C311 to control the "RAS time-out" operation.

Table 7-5. REGISTER 4Dh Definition

NAME:	Parity Error Diagnostic Register 5 INDEX: 4Dh	Default Values: XXXXXXXX
	Functions:	
7-4	RESERVED	
3	0 = No Parity Error 1 = Parity error is caused by BYTE 3	
2	0 = No Parity Error 1 = Parity error is caused by BYTE 2	
1	0 = No Parity Error 1 = Parity error is caused by BYTE 1	
0	0 = No Parity Error 1 = Parity error is caused by BYTE 0	
	NOTE: During power up, bits 3 and 2 reflects the presence status of Intel 80387 and WTL 3167 coprocessors respectively. 0 = Coprocessor is not installed 1 = Coprocessor is installed. After the first read from this register, it resumes the normal definition.	

(The definition is also listed in e88C311 Specifications)

7.5 Math Coprocessor Interface Logic

The e88C312 supports the interface logic for the Intel 80387 as well as the WTL 3167 math coprocessor. Bus cycle generation is handled by the e88C311. Interface signals consist of input signals: FRSTADS, BZ387-, PRQ387-, ERR387-, RST387-, WINTR and WTPRES- and output signals: IRQ13, BZ386-, PRQ386 and ERR386-.

At reset, the states of the ERR387- and WTPRES- signals are sampled to detect the presence of either coprocessor. The states are latched into bits 3 and 2 of 4Dh register. The first *and only* I/O read access to 4Dh will read back these states to system BIOS (see Table 1.5). Subsequent access to 4Dh will return the parity error bits instead. The ERR387- is sampled by the trailing edge of RESET4 to generate the ERR386- output. By sampling this output during reset, the CPU (80386) is able to determine the presence of a 80387. The first ADS- signal from the CPU (FRSTADS) forces the ERR386- high thereafter. Subsequent ERR387- signals will not cause ERR386- to go low, but instead hold the busy state of the coprocessor at output BZ386- and also generate IRQ13.

The 80387 asserts ERR387- after an operation resulting in an error not masked by the coprocessor's control register. The e88C312 will use the ERR387- input to latch the BZ387- signal and generate IRQ13. As soon as BZ387- goes inactive (high), the PRQ386 is asserted. The PRQ386 is also asserted when PRQ387 becomes active. The latched BZ386- and IRQ13 will be cleared when e88C312 receives a RST387 signal from the e88C311 or when an I/O write cycle to port F0h or F1h is executed. (See action code DBAM<4:0> = 17h .)

8. e88C312 PIN DESCRIPTION

8.1 e88C312 Pin Diagram

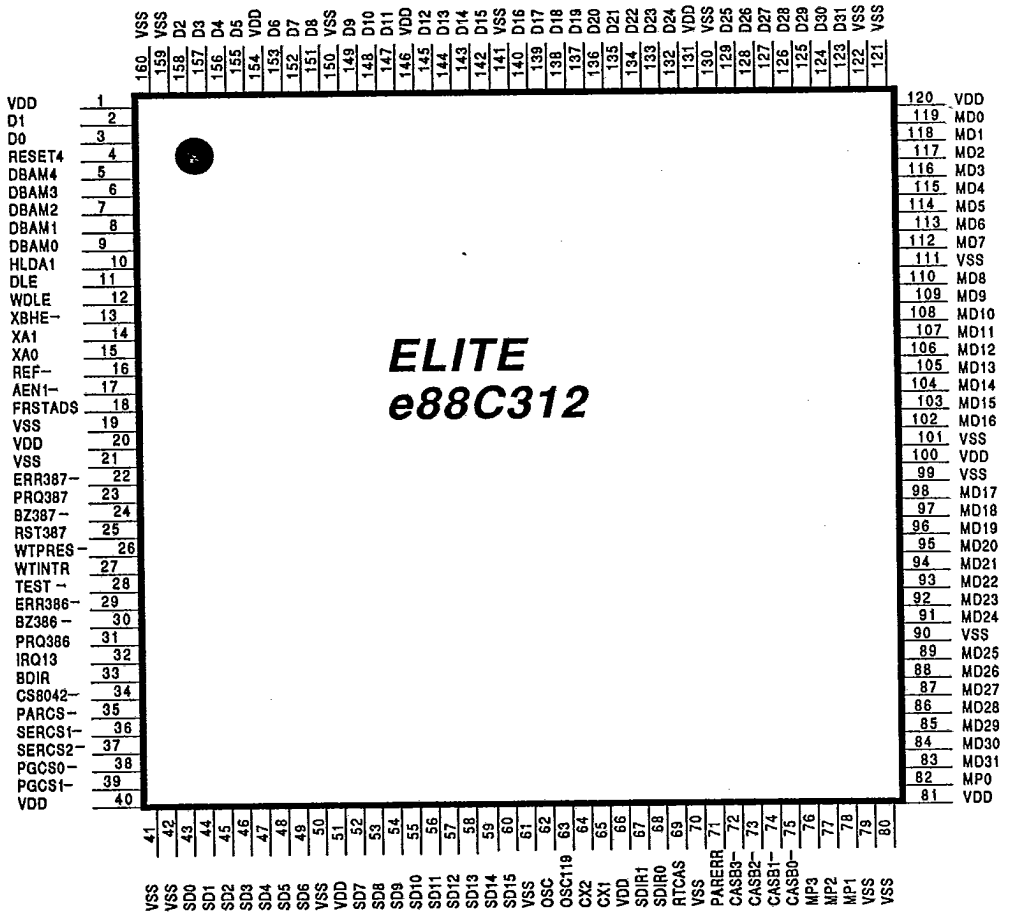


Figure 8-1. e88C312 Pin Diagram

8.2 e88C312 Pin List

PIN No.	NAME	TYPE	DESCRIPTION
123-129 132-140 142-145 147-149 151-153 155-158 2-3	**D<31:0>**	Input/Output	*Local Data* bits 0 through 31 connected to 80386 CPU.
12	**WDLE**	Input	*Write Data Latch Enable* from the e88C311. It is used to latch the CPU write data into an on-chip register for post-write operation
11	**DLE**	Input	*Data Latch Enable* from the e88C311. The high to low transition of this signal latches memory data into the e88C312.
10	**HLDA1**	Input	*Hold Acknowledge* 1 from the e88C311. It is high when the CPU relinquishes the system bus to other masters.
5-9	**DBAM<4:0>**	Input	Data controller action mode codes from the e88C311. It defines the type of current bus cycle and determines the direction of the data transfer.
17	**AEN1-**	Input	*Address Enable* of an 8 bit DMA transfer. It is used to latch the addresses for 8 bit DMA/Master cycles.
13	**XBHE-**	Input	*Byte High Enable.*
14-15	**XA<1:0>**	Input	XA address bits 1 and 0.
83-89 91-98 102-110 112-119	**MD<31:0>**	Input/Output	*Memory Data* bits 0 through 31 from memory array (DRAMs).
76-78, 82	**MP<3:0>**	Input/Output	*Memory Data Parity* bits from DRAMs.

PIN No.	NAME	TYPE	DESCRIPTION
71	**PARERR**	Output	*Latched Parity Error;* when high it indicates a parity error. The e88C311 will latch the error address upon detecting an error.
72-75	**CASB<3:0>-**	Input	*CAS Byte Enable* signals from the e88C311 latch parity error bits for each byte of data.
60-52 49-43	**SD<15:0>**	Input/Output	*System Data Bus.* SD<7:0> are tied together with the peripheral data bus signals XD<7:0>. SD<15:0> can be connected to the AT bus directly or through a pair of 245's.
67-68	**SDIR<1:0>**	Output	*SD Bus Direction Control.* These two signals are used to control the data bus direction between I/O channel data bus (SD) and local SD bus (LSD). When high, SDIR<1:0> drives the LSD bus toward the I/O Channel bus. When low, SDIR<1:0> drives the I/O Channel bus towards the LSD bus.
33	**BDIR**	Output	*Buffer Direction.* This signal is used to control the address bus direction between I/O Channel address bus (SA) and the peripheral address bus (XA). When high, BDIR drives the XA address bus toward SA address bus. When low, BDIR drives the SA address bus toward XA address bus.
16	**REF-**	Input	*AT Bus Refresh.* REF- is used to toggle the 80386 Busy signal (BZ386-) if 80387 is not present.
65	**CX1**	Input	*14.318 MHz Oscillator Input* from the crystal.
64	**CX2**	Output	*14.318 MHz Oscillator Output* to the crystal.
62	**OSC**	Output	*14.318 MHz Oscillator Output to the AT* bus.

PIN No.	NAME	TYPE	DESCRIPTION
63	**OSC119**	Output	*1.19 MHz* (14.318 MHz/12) or oscillator output. It is used by the e88C311 for RAS time-out control; it is also used as a clock input to the on-board timer/counter logic.
69	**RTCAS**	Output	*Address Strobe for the RTC.* The I/O address is conditioned with XIOW-.
34	**CS8042-**	Output	*8042 Keyboard Controller* Chip Select.
36	**SERCS1-**	Output	*Software Programmable Serial Port 1 chip select.* This feature is enabled by setting bit 0 of register 19h in the e88C311 to 1.
37	**SERCS2-**	Output	*Software Programmable Serial Port 2 Chip Select.* This feature is enabled by setting bit 1 of register 19h in the e88C311 to 1.
35	**PARCS-**	Output	*Software Programmable Parallel Port Chip select.* This feature is enabled by setting bit 2 of register 19h in the e88C311 to 1.
39-38	**PGCS<1:0>-**	Output	*Programmable Chip Select 0 and 1.* These are defined by configuration registers 13h through 18h in e88C311.
24	**BZ387-**	Input	*80387 BUSY-* signal. When active, it indicates that the coprocessor is busy executing an instruction. This input has an internal pull-up.
22	**ERR387-**	Input	*80387 ERROR-* signal. When active, it indicates that an error has been generated in a previous coprocessor cycle. This input has an internal pull-up.
23	**PRQ387**	Input	*80387 PEREQ* signal. When active, it indicates that the 80387 is requesting a data transfer cycle between the 80386 and the 80387. This input has an internal pull-down.

PIN No.	NAME	TYPE	DESCRIPTION
30	**BZ386-**	Output	*80386 BUSY-* signal. When active, it indicates that the coprocessor is still executing an instruction and is not able to accept the next instruction.
29	**ERR386-**	Output	*80386 ERROR-* signal. When active, it indicates that a previous coprocessor instruction generated an error of a type not masked by the coprocessor's control registers.
31	**PRQ386**	Output	*80386 PEREQ* signal. When active, it indicates that a coprocessor requests a data operand to be transferred to/from memory by the 80386.
26	**WTPRES-**	Input	*Weitek Coprocessor Presence.* If the Weitek coprocessor is installed, this pin will be pulled to logic 0. It should be connected to Vcc through a resistor of 10K Ohms to ensure a high logic level when the Weitek coprocessor is not installed.
27	**WTINTR**	Input	*Weitek Coprocessor Interrupt.* It is "OR'ed" with the 80387 interrupt logic to generate IRQ13. This input has an internal pull-down.
32	**IRQ13**	Output	*Interrupt Request 13.* When high, it signals an interrupt request from the coprocessor to the 80386. The service routine handles coprocessor errors.
18	**FRSTADS**	Input	*First Address Status.* An input signal from the e88C311 indicating the *first ADS- cycle.* It goes low after the first ADS- signal is issued by 80386. It is used to stop further detection of coprocessor presence after a system reset.
25	**RST387**	Input	*80387 Reset* from e88C311.
4	**RESET4**	Input	*RESET4* signal from the e88C311. It is used to reset all internal registers and to detect coprocessor presence during system reset.

PIN No.	NAME	TYPE	DESCRIPTION
28	**TEST-**	Input	*Test* signal. When low, this signal tri-states all of the e88C312 outputs. In normal operation, this signal should be tied to logic 1. This input has an internal pull-up.
1,20,40,51, 66,81,100, 120,131, 146,154	**VDD**	Input	Supply Voltage at nominal 5.0 Vdc.
19,21,41,42, 50,61,70,79, 80,90, 99,101, 111,121,122, 130,141,150, 159,160	**VSS**	Input	Ground.

9. e88C312 ELECTRICAL AND TIMING SPECIFICATION

9.1 Storage and Operating Characteristics

9.1.1 Absolute Maximum Ratings

Stresses above the conditions listed in this section may cause permanent damage to the device. This is a stress rating only. The functional operation of the device at these or any other conditions above those indicated in the Recommended Operating Conditions section is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 9-1. Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE		UNIT
		MIN	MAX	
Supply Voltage	V_{cc}	-0.3	7.0	Volts
Input Voltage	V_i	-0.3	V_{cc} + 0.3	Volts
Storage Temperature	T_{stg}	-40.0	125.0	degrees C

9.1.2 e88C312 Recommended Operating Conditions

Table 9-2. Recommended Operating Conditions

PARAMETER	SYMBOL	VALUE		UNIT
		MIN	MAX	
Supply Voltage	V_{cc}	4.75	5.25	Volts
Input Voltage	V_i	0	V_{cc}	Volts
Ambient Temperature	T_a	0	50	degrees C

9.2 e88C312 DC Characteristics

(V_{CC} = 5.0 Volts +/-5%; T_a = 0 - 50° C)

Table 9-3. e88C312 DC Characteristics

PARAMETER	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Input Low Voltage	Vil			
TTL level			0.8	Volts
Schmitt level			1.0	Volts
Input High Voltage	Vih			
TTL level		2.0		Volts
Schmitt level		4.0		Volts
Input Low Current	Iil	-10	10	µA
W/ Pull-up Resistor		-200	-10	µA
Input high current		-10	10	µA
W/ Pull-down Resistor		10	200	µA
Output low voltage	Vol		0.4	Volts
2 mA buffer, IOL = 2mA				
4 mA buffer, IOL = 4mA				
8 mA buffer, IOL = mA				
12 mA buffer, IOL = 12 mA				
Output high voltage	Voh	2.4		Volts
2 mA buffer, IOH = -2mA				
4 mA buffer, IOH = -4mA				
8 mA buffer, IOH = -8mA				
12 mA buffer, IOH = -12mA				
High Impedance Leakage	Ioz			
Current		-10	10	µA
W/ Pull-up Resistor		-200	-10	µA
W/ Pull-down Resistor		10	200	µA
Device Quiescent	Iccq		TBD	µA
Supply Current			TBD	
Supply Current	Icc		TBD	mA
Power Dissipation	Pdis		TBD	mW
Input Capacitance	Cin		7	pF
Output or I/O Capacitance	Cout		10	pF

9.3 e88C312 AC Characteristics

(Vcc = 5.0 Volts +/- 5%; Ta = 0-50° C)

NOTE: The symbol number in the following table indicates which timing diagram the symbol is associated with. The first digit of the 3-digit number following the T indicates the figure number within section 10. For example, the timing parameter T505 can be found in Figure 10-5.

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
MD<31:0> Setup Time to DLE Low	T101	7		ns
MD<31:0> Hold Time from DLE Low	T102	5		ns
D<31:0> Valid from DBAM<4:0>	T103	8	29	ns
D<31:0> Valid from MD<31:0>	T104	4	15	ns
D<31:0> Float Delay from DBAM<4:0>	T105	8	26	ns
PARERR Valid from MD<31:0>	T106	10	35	ns
D<31:0> Setup Time to WDLE Low	T107	4		ns
D<31:0> Hold Time from WDLE Low	T108	2		ns
MD<31:0> Valid from DBAM<4:0>	T109	7	26	ns
MD<31:0> Valid from D<31:0>	T110	5	18	ns
MD<31:0> Float Delay from DBAM<4:0>	T111	6	20	ns
MP<3:0> Valid from DBAM<4:0>	T112	7	26	ns
MP<3:0> Valid from D<31:0>	T113	8	30	ns
MP<3:0> Float Delay from DBAM<4:0>	T114	6	20	ns

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
SD<15:0> Valid from DBAM<4:0>	T201	10	35	ns
SD<15:0> Valid from MD<31:0>	T202	9	30	ns
SD<15:0> Float Delay from DBAM<4:0>	T203	9	33	ns
PARERR Valid from MD<31:0>	T204	10	35	ns
MD<31:0> Valid from SD<15:0>	T205	5	18	ns
MP<3:0> Valid from SD<15:0>	T206	9	33	ns
SD<15:0> Setup Time to DLE Low	T301	7	-	ns
SD<15:0> Hold Time from DLE Low	T302	5	-	ns
D<31:0> Valid from SD<15:0>	T303	6	19	ns
SD<15:0> Valid from D<31:0>	T304	8	28	ns
BDIR Active from DBAM<4:0>	T401	4	14	ns
BDIR Inactive from DBAM<4:0>	T402	5	17	ns
SDIR0 Active from DBAM<4:0>	T403	8	28	ns
SDIR0 Inactive from DBAM<4:0>	T404	8	27	ns
SD<7:0> Valid from SD<15:8>	T405	9	32	ns
SDIR1 Active from DBAM<4:0>	T406	8	28	ns
SDIR1 Inactive from DBAM<4:0>	T407	8	27	ns
SD<15:8> Valid from SD<7:0>	T408	9	32	ns

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
CS8042- Active from DLE High	T501	5	16	ns
PARCS- Active from DLE High	T502	5	16	ns
SERCS1- Active from DLE High	T503	5	16	ns
SERCS2- Active from DLE High	T504	5	16	ns
PGCS0- Active from DLE High	T505	5	16	ns
PGCS1- Active from DLE High	T506	5	16	ns
RTCAS Active from DLE High	T507	5	16	ns
CS8042- Inactive from DLE Low	T508	6	18	ns
PARCS- Inactive from DLE Low	T509	6	18	ns
SERCS1- Inactive from DLE Low	T510	6	18	ns
SERCS2- Inactive from DLE Low	T511	6	18	ns
PGCS0- Inactive from DLE Low	T512	6	18	ns
PGCS1- Inactive from DLE Low	T513	6	18	ns
RTCAS Inactive from DLE Low	T514	6	18	ns
CX2 Low from CX1 High	T601	4	12	ns
OSC Low from CX1 High	T602	11	38	ns
OSC119 High from CX1 Low	T603	11	40	ns
CX2 High from CX1 Low	T604	2	6	ns
OSC High from CX1 Low	T605	9	30	ns
OSC119 Low from CX1 Low	T606	11	40	ns

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
ERR387- Setup Time to RESET4 Low	T701	6	-	ns
ERR387- Hold Time from RESET4 Low	T702	4	-	ns
ERR386- Valid from RESET4 Low	T703	6	21	ns
ERR386- Inactive from FRSTADS Low	T704	4	13	ns
BZ387- Setup Time to ERR387- Low	T705	7	-	ns
BZ387- Hold Time from ERR387- Low	T706	4	-	ns
BZ386- Active from BZ387- Low	T707	5	16	ns
BZ386- Inactive from RST387 High	T708	6	21	ns
PRQ386 Active from BZ387- High	T709	6	20	ns
PRQ386 Inactive from RST387 High	T710	6	22	ns
IRQ13 Active from BZ387- High	T711	5	19	ns
IRQ13 Inactive from RST387 High	T712	6	21	ns
BZ386- Inactive from DLE High (DBAM<4:0> = 17 h)	T713	6	22	ns
PRQ386 Inactive from DLE High (DBAM<4:0> = 17 h)	T714	7	23	ns
IRQ13 inactive from DLE High (DBAM<4:0> = 17 h)	T715	7	23	ns
PRQ386 Active from PRQ387 High	T716	4	12	ns
PRQ386 Inactive from PRQ387 Low	T717	5	16	ns
IRQ13 Active from WTINTR High	T718	4	13	ns
IRQ13 Inactive from WTINTR Low	T719	5	17	ns

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
D<31:24> Valid from DLE High (DBAM<4:0> = 1Eh)	T801	6	21	ns
SD<7:0> Valid from DBAM<4:0>=1Eh	T802	13	43	ns
PARERR Inactive from DBAM<4:0>=1Eh	T803	7	25	ns

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
BDIR Active from REF- Low	T901	5	16	ns
BDIR Inactive from REF- High	T902	5	16	ns
BZ386- Active from REF- Low	T903	6	20	ns
BZ386- Inactive from REF- High	T904	5	16	ns
D<31:0> Tri-Stated from TEST- Low	T905	6	21	ns
MD<31:0> Tri-Stated from TEST- Low	T906	7	23	ns
MP<3:0> Tri-Stated from TEST- Low	T907	7	23	ns
SD<15:0> Tri-Stated from TEST- Low	T908	8	25	ns
PARERR Tri-stated from TEST- Low	T909	4	15	ns
OSC Tri-Stated from TEST- Low	T910	4	17	ns
All Other Outputs Tri-Stated from TEST- Low	T911	4	15	ns
D<31:0> Enabled from TEST- High	T912	6	23	ns
MD<31:0> Enabled from TEST- High	T913	7	25	ns
MP<3:0> Enabled from TEST- High	T914	7	25	ns
SD<15:0> Enabled from TEST- High	T915	8	26	ns
PARERR Enabled from TEST- High	T916	4	14	ns
OSC Enabled from TEST- High	T917	4	15	ns
All Other Outputs Enabled from TEST- High	T918	5	18	ns

10. e88C312 TIMING DIAGRAMS

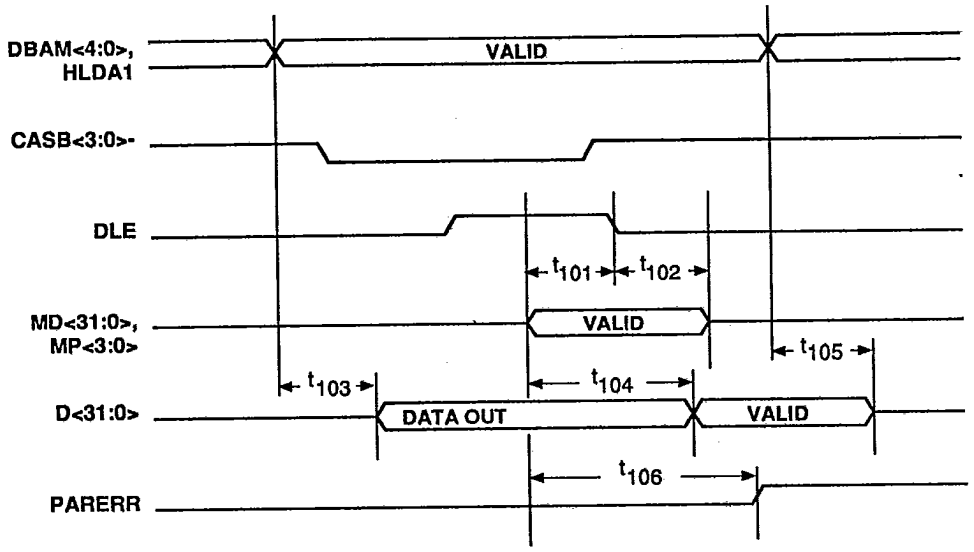


Figure 10-1A. CPU Local Memory Read

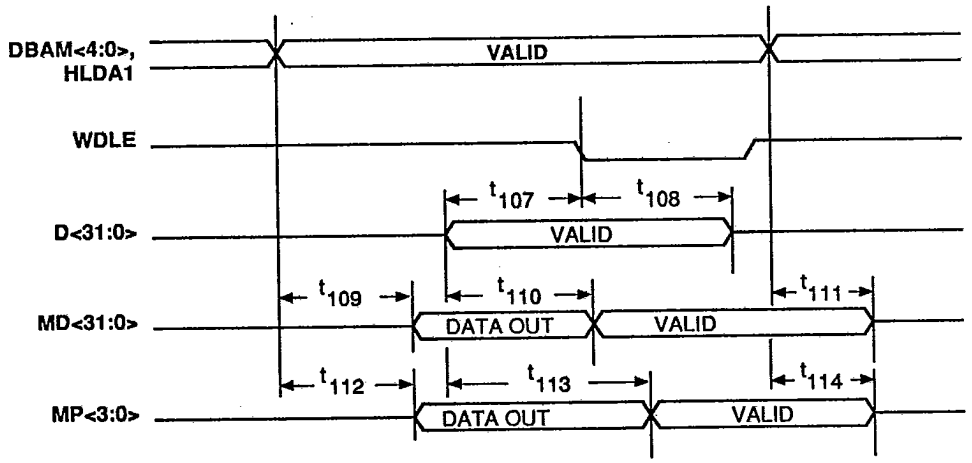
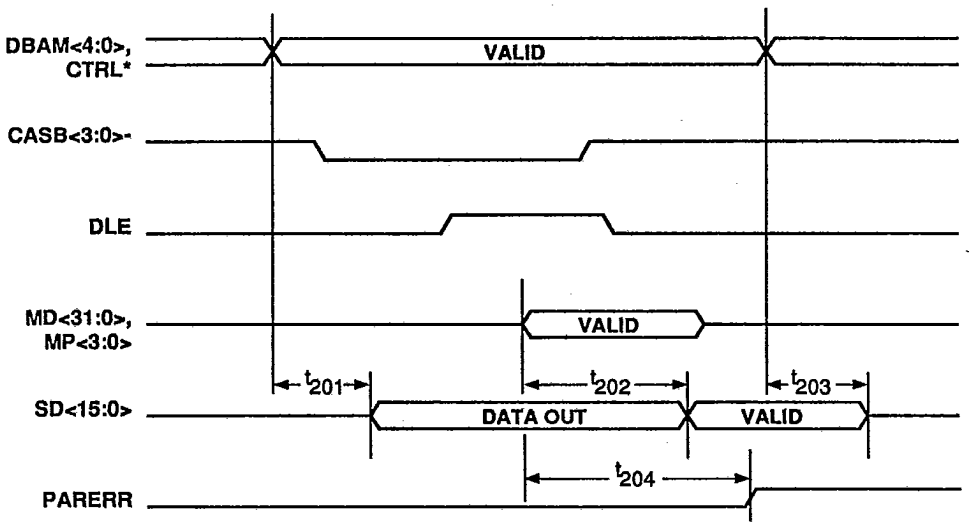
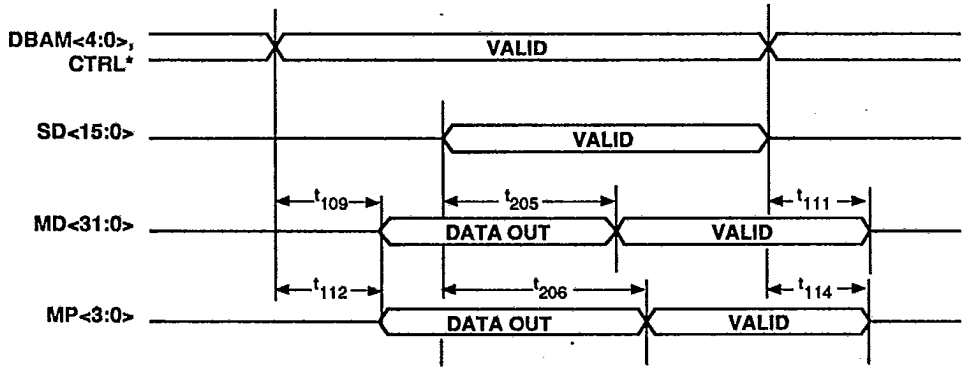


Figure 10-1B. CPU Local Memory Write



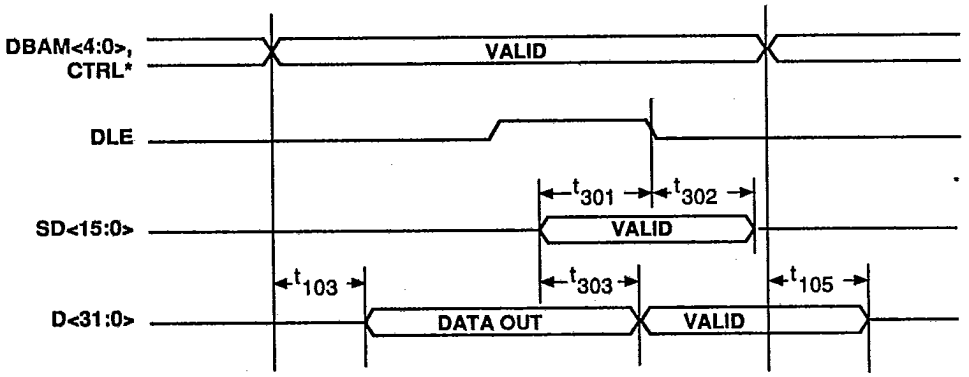
[CTRL* = HLDA1, AEN1- , XBHE-, XA1, XA0]

Figure 10-2A. Master/DMA Local Memory Read



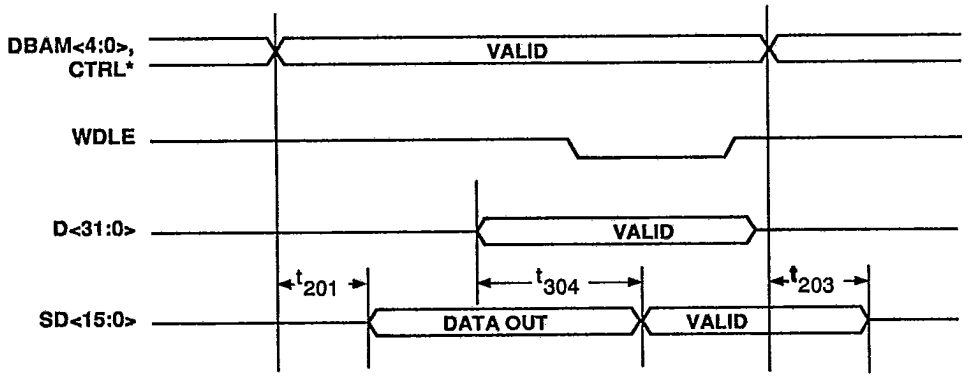
[CTRL* = HLDA1, AEN1- , XBHE-, XA1, XA0]

Figure 10-2B. Master/DMA Local Memory Write



[CTRL* = HLDA1, XBHE-, XA1, XAO]

Figure 10-3A. CPU I/O Read



[CTRL* = HLDA1, XBHE-, XA1, XAO]

Figure 10-3B. CPU I/O Write

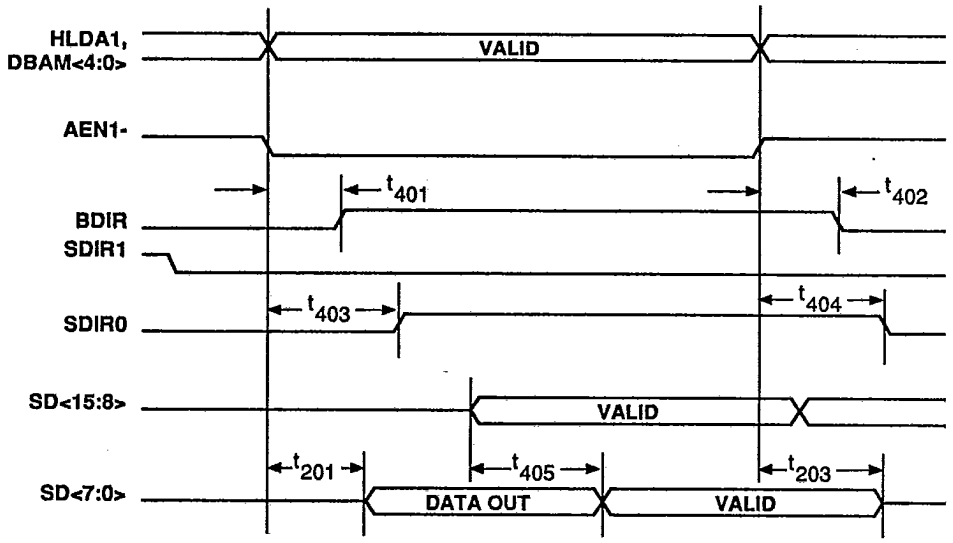


Figure 10-4A. 8-bit DMA Hi-Byte to Low-Byte Swap

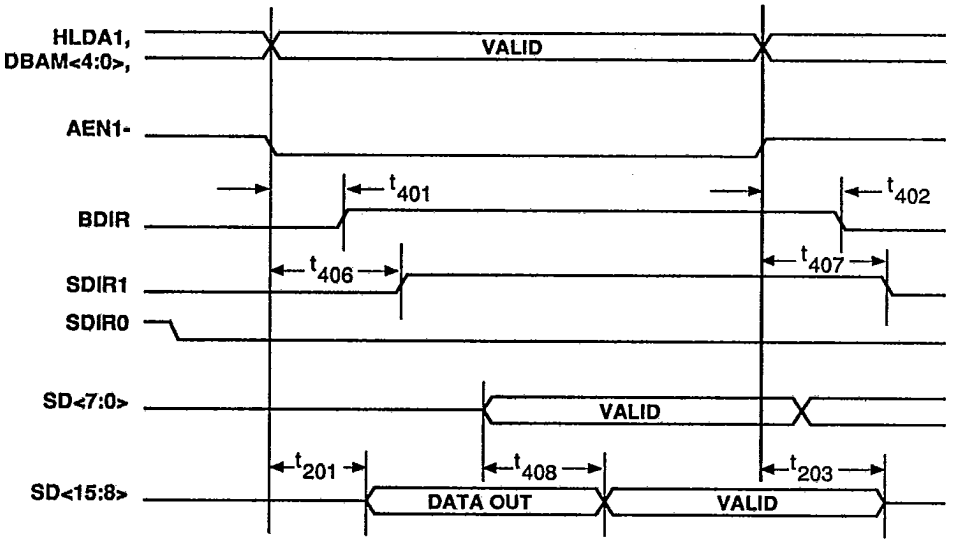


Figure 10-4B. 8-bit DMA Low-Byte to Hi-Byte Swap

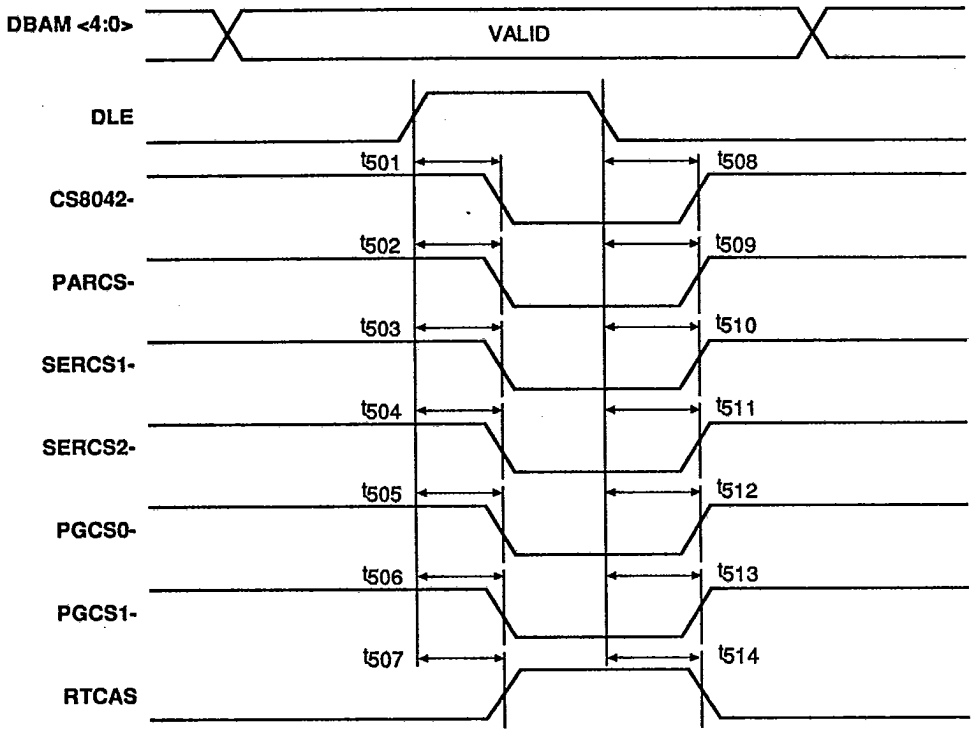


Figure 10-5. I/O Chip Selects

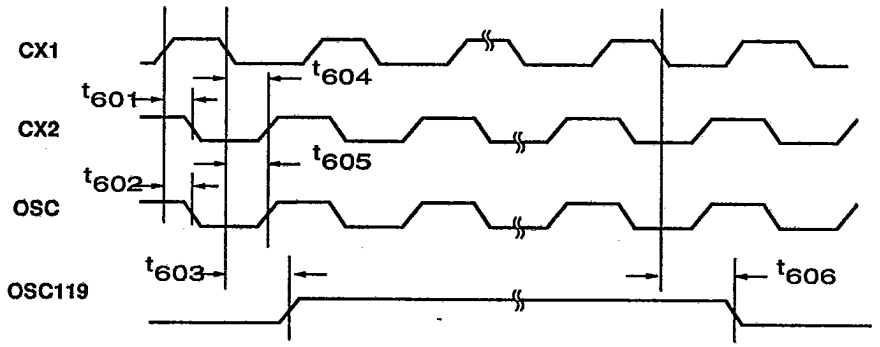


Figure 10-6. Oscillator and Timer Clock

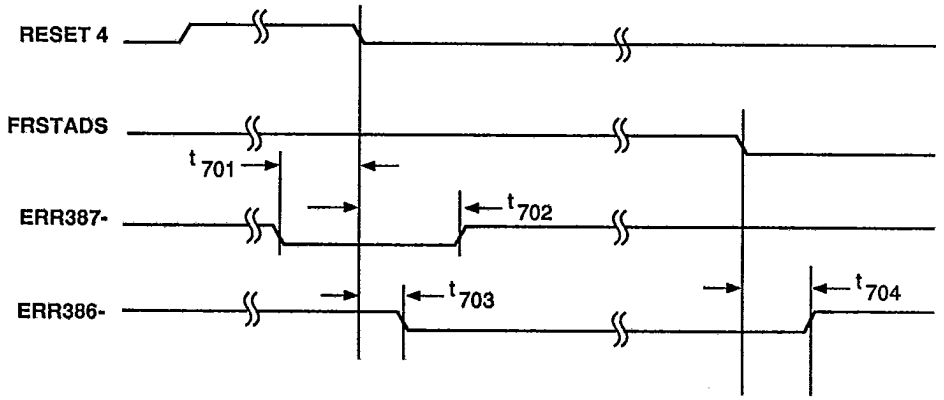


Figure 10-7A. Math Coprocessor Detection

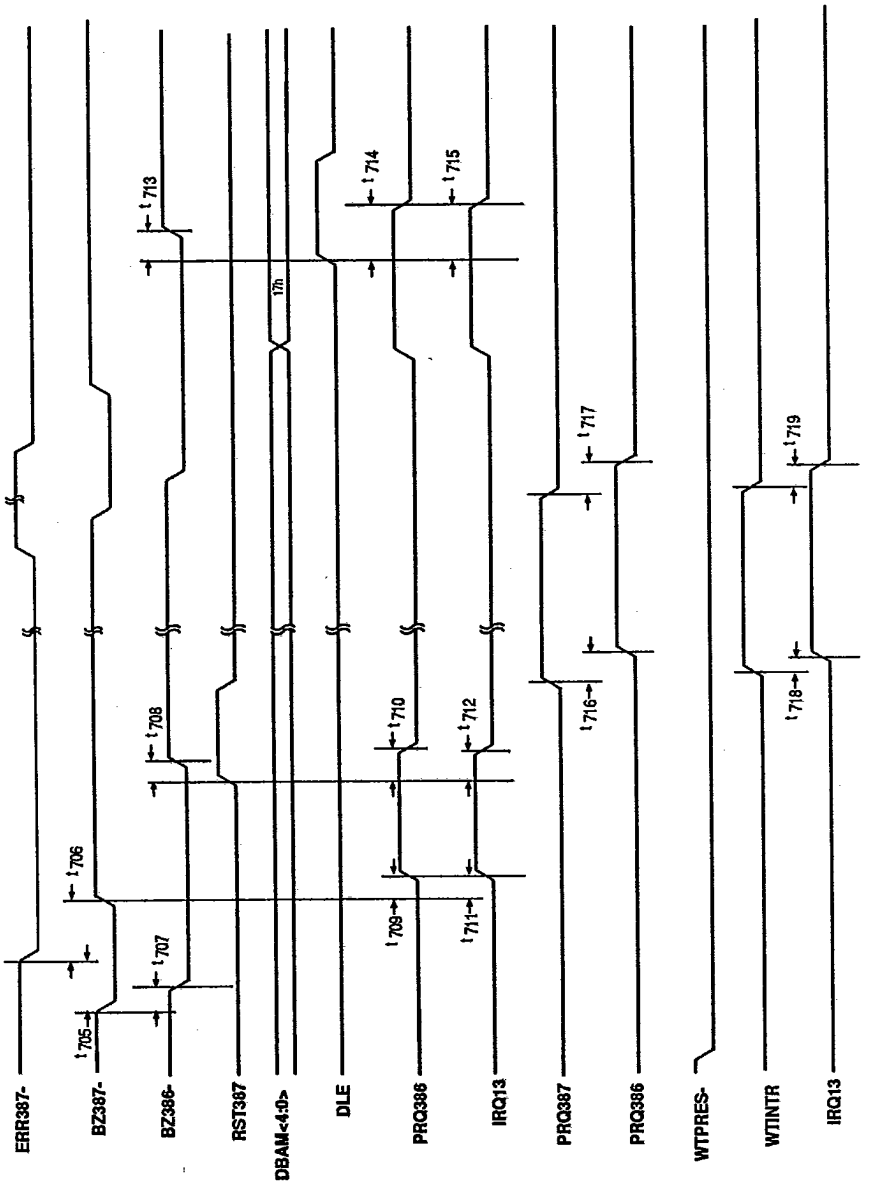


Figure 10-7B. Math Coprocessor Interface Timing

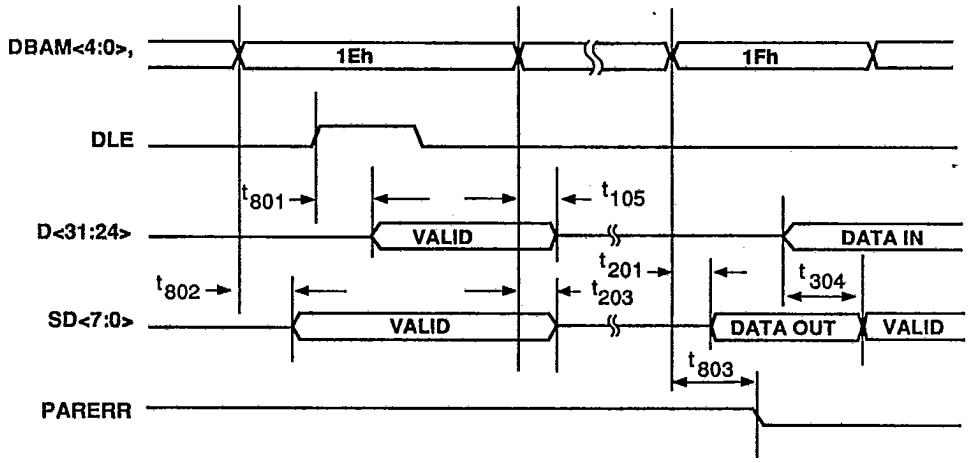


Figure 10-8. Parity Register Read and Reset

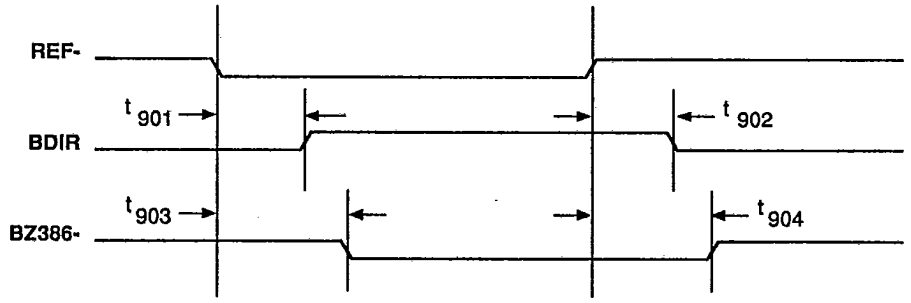


Figure 10-9A. Refresh Buffer Control and Coprocessor Busy

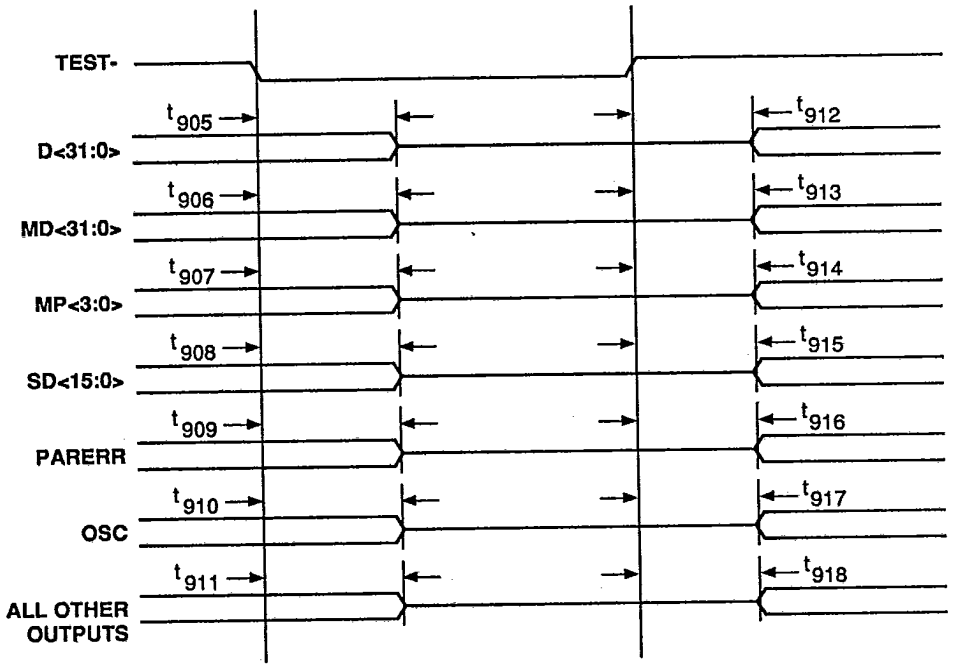


Figure 10-9B. Test Mode

11. e88C312 MECHANICAL INFORMATION

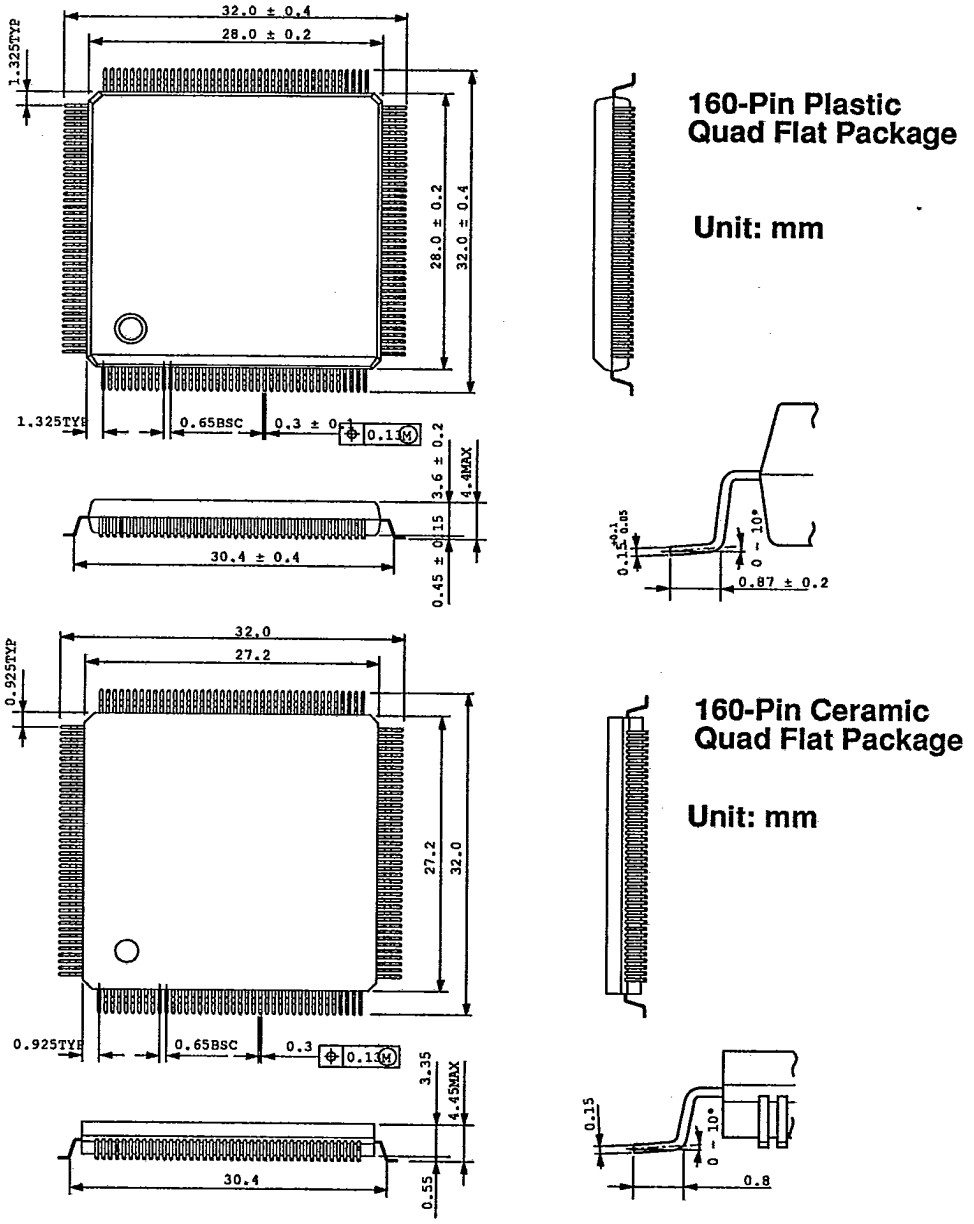


Figure 11-1. e88C312: 160-Pin Quad Flat Package

11.1 e88C312 Pin Lists

11.1.1 Numerical

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VDD	41	VSS	81	VDD	121	VSS
2	D1	42	VSS	82	MP0	122	VSS
3	D0	43	SD0	83	MD31	123	D31
4	RESET4	44	SD1	84	MD30	124	D30
5	DBAM4	45	SD2	85	MD29	125	D29
6	DBAM3	46	SD3	86	MD28	126	D28
7	DBAM2	47	SD4	87	MD27	127	D27
8	DBAM1	48	SD5	88	MD26	128	D26
9	DBAM0	49	SD6	89	MD25	129	D25
10	HLDA1	50	VSS	90	VSS	130	VSS
11	DLE	51	VDD	91	MD24	131	VDD
12	WDLE	52	SD7	92	MD23	132	D24
13	XBHE-	53	SD8	93	MD22	133	D23
14	XA1	54	SD9	94	MD21	134	D22
15	XA0	55	SD10	95	MD20	135	D21
16	REF-	56	SD11	96	MD19	136	D20
17	AEN1-	57	SD12	97	MD18	137	D19
18	FRSTADS	58	SD13	98	MD17	138	D18
19	VSS	59	SD14	99	VSS	139	D17
20	VDD	60	SD15	100	VDD	140	D16
21	VSS	61	VSS	101	VSS	141	VSS
22	ERR387-	62	OSC	102	MD16	142	D15
23	PRQ387	63	OSC119	103	MD15	143	D14
24	BZ387-	64	CX2	104	MD14	144	D13
25	RST387	65	CX1	105	MD13	145	D12
26	WTPRES-	66	VDD	106	MD12	146	VDD
27	WTINTR	67	SDIR1	107	MD11	147	D11
28	TEST-	68	SDIR0	108	MD10	148	D10
29	ERR386-	69	RTCAS	109	MD9	149	D9
30	BZ386-	70	VSS	110	MD8	150	VSS
31	PRQ386	71	PARERR	111	VSS	151	D8
32	IRQ13	72	CASB3-	112	MD7	152	D7
33	BDIR	73	CASB2-	113	MD6	153	D6
34	CS8042-	74	CASB1-	114	MD5	154	VDD
35	PARCS-	75	CASB0-	115	MD4	155	D5
36	SERCS1-	76	MP3	116	MD3	156	D4
37	SERCS2-	77	MP2	117	MD2	157	D3
38	PGCS0-	78	MP1	118	MD1	158	D2
39	PGCS1-	79	VSS	119	MD0	159	VSS
40	VDD	80	VSS	120	VDD	160	VSS

11.1.2 Alphabetical

Name	Pin	Name	Pin	Name	Pin	Name	Pin
AEN1-	17	D7	152	MD4	115	SERCS1-	36
BDIR	33	D8	151	MD5	114	SERCS2-	37
BZ386-	30	D9	149	MD6	113	TEST-	28
BZ387-	24	DBAM0	9	MD7	112	VDD	1
CASB0-	75	DBAM1	8	MD8	110	VDD	20
CASB1-	74	DBAM2	7	MD9	109	VDD	40
CASB2-	73	DBAM3	6	MP0	82	VDD	51
CASB3-	72	DBAM4	5	MP1	78	VDD	66
CS8042-	34	DLE	11	MP2	77	VDD	81
CX1	65	ERR386-	29	MP3	76	VDD	100
CX2	64	ERR387-	22	OSC	62	VDD	120
D0	3	FRSTADS	18	OSC119	63	VDD	131
D1	2	HLDA1	10	PARCS-	35	VDD	146
D10	148	IRQ13	32	PARERR	71	VDD	154
D11	147	MD0	119	PGCS0-	38	VSS	19
D12	145	MD1	118	PGCS1-	39	VSS	21
D13	144	MD10	108	PRQ386	31	VSS	41
D14	143	MD11	107	PRQ387	23	VSS	42
D15	142	MD12	106	REF-	16	VSS	50
D16	140	MD13	105	RESET4	4	VSS	61
D17	139	MD14	104	RST387	25	VSS	70
D18	138	MD15	103	RTCAS-	69	VSS	79
D19	137	MD16	102	SD0	43	VSS	80
D2	158	MD17	98	SD1	44	VSS	90
D20	136	MD18	97	SD10	55	VSS	99
D21	135	MD19	96	SD11	56	VSS	101
D22	134	MD2	117	SD12	57	VSS	111
D23	133	MD20	95	SD13	58	VSS	121
D24	132	MD21	94	SD14	59	VSS	122
D25	129	MD22	93	SD15	60	VSS	130
D26	128	MD23	92	SD2	45	VSS	141
D27	127	MD24	91	SD3	46	VSS	150
D28	126	MD25	89	SD4	47	VSS	159
D29	125	MD26	88	SD5	48	VSS	160
D3	157	MD27	87	SD6	49	WDLE	12
D30	124	MD28	86	SD7	52	WTINTR	27
D31	123	MD29	85	SD8	53	WTPRES-	26
D4	156	MD3	116	SD9	54	XA0	15
D5	155	MD30	84	SDIR0	68	XA1	14
D6	153	MD31	83	SDIR1	67	XBHE-	13