Features

- Stereo Audio DAC
  - 2.7V to 3.3V Analog Supply Operation
  - 2.4V to 3.3V Digital Supply Operation
  - 20-bit Stereo Audio DAC
  - 93 dB SNR Playback Stereo Channels
  - 32 Ohm/20 mW Stereo Headset Drivers with Master Volume and Mute Controls
  - Stereo Line Level Input with Volume Control/mute and Playback through the Headset Drivers
  - Differential Monaural Auxiliary Input, with Volume Control/mute and Playback through the Headset Drivers
  - Accepts Mixed Signals from All Signal Paths (Line Inputs, External Mono and DAC Output)
  - 8, 11.024, 16, 22.05, 24, 32, 44.1 and 48 kHz Sampling Rates
  - 256x or 384xFs Master Clock Frequency
  - I2S Serial Audio Interface
- Mono Audio Power Amplifier
  - Supply Input from Main Li-Ion Battery
  - 440mW on 8 Ohm Load
  - Low Power Mode for Earphone
  - Programmable Volume Control (-22 to +20 dB)
  - Fully Differential Structure, Input and Output
  - 8 mA Drain Current in Full Power Mode
  - Power-down mode (Consumption Less than 2 µA)
  - Minimum External Components (Direct Connection of the Loudspeaker)
- Applications: Mobile Phones, Digital Cameras, PDAs, SmartPhones, DECT Phones, Music Players

Power Management and Analog Companions (PMAAC)

AT73C213B Audio Interface for Portable Handsets

1. Description

The AT73C213B is a fully integrated, low-cost, combined stereo audio DAC and audio power amplifier circuit targeted for Li-Ion or Ni-Mh battery powered devices such as mobile phones, smartphones, PDA, DECT phones, digital still cameras, music players or any other type of handheld device where an audio interface is needed.

The stereo DAC section is a complete high performance, stereo audio digital-to-analog converter delivering a 93 dB dynamic range. It comprises a multibit sigma-delta modulator with dither, continuous time analog filters and analog output drive circuitry. This architecture provides a high insensitivity to clock jitter. The digital interpolation filter increases the sample rate by a factor of 8 using 3 linear phase half-band filters cascaded, followed by a first order SINC interpolator with a factor of 8. This filter eliminates the images of baseband audio, retaining only the image at 64x the input sample rate, which is eliminated by the analog post filter. Optionally, a dither signal can be added that reduces possible noise tones at the output. However, the use of a multibit sigma-delta modulator already provides extremely low noise tone energy.

Master clock is from 256 or 384 times the input data rate, allowing choice of input data rate up to 50 kHz, including standard audio rates of 48, 44.1, 32, 16 and 8 kHz.

The DAC section is followed by a volume and mute control and can be simultaneously played back directly through a stereo 32 Ohm headset pair of drivers.

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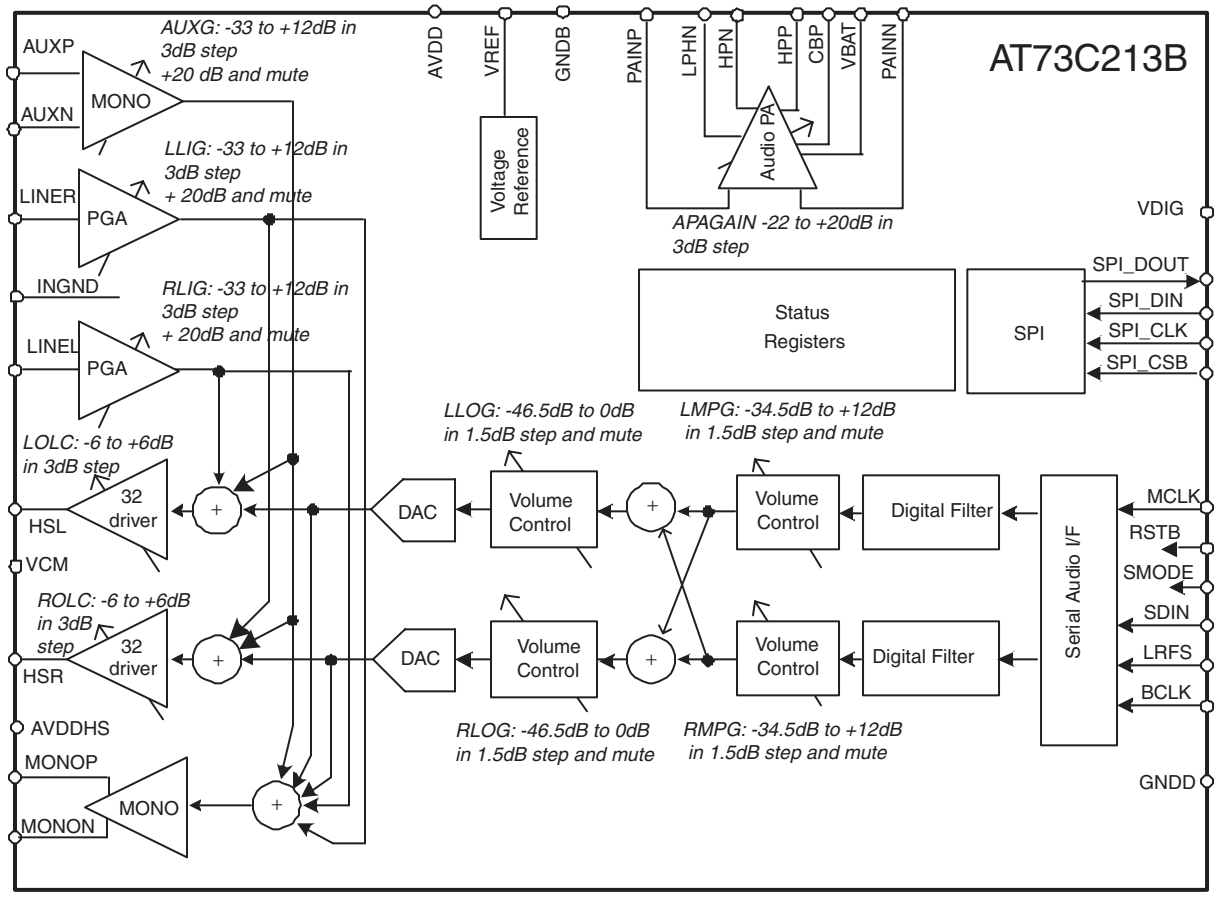
The stereo 32 Ohm headset pair of drivers also includes a mixer of a LINEL and LINER pair of stereo inputs, as well as a differential monaural auxiliary input (line level).

The DAC output can be connected through a buffer stage to the input of the audio power amplifier, using 2x coupling capacitors The mono buffer stage also includes a mixer of the LINEL and LINER inputs, as well as a differential monaural auxiliary input (line level) which can be, for example, the output of a voice Codec output driver in mobile phones.

The audio power amplifier is a dual-mode AB class amplifier with differential output and programmable volume control. In full power mode, it is capable of driving an 8-ohm loudspeaker at maximum power of 1W at 5V supply and 440 mW at 3.6V supply. In low power mode, it can drive the same loudspeaker as an earpiece, making it suitable as a handsfree speaker driver in wireless handset application. The volume, mute, power down, de-emphasis controls and 16-bit, 18-bit and 20-bit audio formats are digitally programmable via a 4-wire SPI bus and the digital audio data are provided through a multi-format I2S interface.

2. Block Diagram

Figure 2-1. AT73C213B Functional Block Diagram



3. Pin Description

Table 3-1. Pin Description

Pin Name	I/O	Pin	Type	Function
LPHN	O	10	Analog	Low power audio stage output
HPN	O	11	Analog	Negative speaker output
VBAT	I	12	Supply	Audio amplifier supply
HPP	O	13	Analog	Positive speaker output
CBP	O	14	Analog	Audio amplifier common mode voltage decoupling
PAINN	I	15	Analog	Audio amplifier negative input
PAINP	I	16	Analog	Audio amplifier positive input
SDIN	I	17	Digital	Audio interface serial data input
BCLK	I	18	Digital	Audio interface bit clock
LRFS	I	19	Digital	Audio interface left/right channel synchronization frame pulse
MCLK	I	20	Digital	Audio interface master clock input
RSTB	I	21	Digital	Master reset (active low)
SMODE	I	22	Digital	Serial interface selection (to connect to ground)
GNDD	GND	23	Ground	Digital ground
VDIG	I	24	Supply	Digital supply
SPI_DOUT	O	25	Digital	SPI data output
SPI_DIN	I/O	26	Digital	SPI data input
SPI_CLK	I	27	Digital	SPI clock
SPI_CSB	I	28	Digital	SPI chip select
MONON	O	29	Analog	Negative monaural driver output
MONOP	O	30	Analog	Positive monaural driver output
AUXP	I	31	Analog	Audio mono auxiliary positive input
AUXN	I	32	Analog	Audio mono auxiliary negative input
VREF	I	1	Analog	Voltage reference pin for decoupling
AVDD	I	2	Supply	Analog supply (DAC + Line in + Aux + Mono out)
HSL	O	3	Analog	Left channel headset driver output
HSR	O	4	Analog	Right channel headset driver output
AVDDHS	I	5	Supply	Headset driver analog supply
LINEL	I	6	Analog	Left channel line in
LINER	I	7	Analog	Right channel line in
INGND	I	8	Analog	Line signal ground pin for decoupling
VCM	I	9	Analog	Common mode reference for decoupling
GNDB	GND	33 (Bottom)	Ground	Analog ground

4. Electrical Characteristics

Table 4-1. Absolute Maximum Ratings*

Operating Temperature (Industrial)-40°C to +85°C
Storage Temperature-55°C to +150°C
Power Supply Input
on VBAT-0.3V to +5.5V
on VDIG, AVDD-0.3V to +3.6V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5. Digital IOs

All the digital IOs: SDIN, BCLK, LRFS, MCLK, RSTB, SMODE, SPI_DOUT, SPI_DIN, SPI_CLK, SPI_CSB are referred to as VDIG.

Table 5-1. Digital IOs

Symbol	Parameter	Conditions	VDIG	Min	Max	Unit
VIL	Low level input voltage	Guaranteed input low Voltage	from 2.4Vto 3.3 V	-0.3	0.2 x VDIG	V
VIH	High level input voltage	Guaranteed input high Voltage	from 2.4Vto 3.3 V	0.8 x VDIG	VDIG + 0.3	V
VOL	Low level output voltage	IOL = 2 mA	from 2.4Vto 3.3 V		0.4	V
VOH	High level output voltage	IOH = 2 mA	from 2.4Vto 3.3 V	VDIG - 0.5V		V

6. Audio Power Amplifier

6.1 Electrical Specifications

VBAT = 3.6V, T_A = 25°C unless otherwise noted. High power mode, 100 nF capacitor connected between CBP and GND Audio, load = 8 Ohms.

Table 6-1. Audio Power Amplifier Electrical Specifications (General Conditions: V_{DD} = 3.6V,T_A = 25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	Unloaded, 100 nF decoupling capacitor to GND	3	3.6	5.5	V
I_{DD}	Quiescent current	Inputs shorted, no load		6	8	mA
I_{DDstby}	Standby current				2	µA
V_{Cbp}	DC reference			VDD/2		V
VOS	Output differential offset	Full gain	-20	0	20	mV
Z_{IN}	Input impedance	Active state	12K	20k	30k	Ohm
Z_{LFP}	Output load	Full Power mode	6	8	32	Ohm
Z_{LLP}	Output load	Low-Power mode, including R1	100	150	300	Ohm
C_L	Capacitive load				100	pF
PSRR	Power supply rejection ratio	200 to 2 kHz differential output		60		dB
BW_{min}	Low Frequency Cutoff	1 kHz reference frequency 3 dB attenuation 470 nF input coupling capacitors		50		Hz
BW_{max}	High Frequency Cutoff	1 KHz reference frequency 3 dB attenuation	20			kHz
t_{UP}	Output setup time	Off to on mode Voltage already settled Input capacitors precharged			10	ms
V_N	Output noise	Max gain, A weighted		120	500	μV_{RMS}
THD_{HP}	Output distortion	High power mode, 1 kHz, Pout = 100mW, gain = 0dB		0.3		%
THD_{LP}	Output distortion	Low power mode,1KHz, V out = 100m Vpp, Max gain, load 8 ohms in series with 200 ohms		1		%
P_{max}	Maximum power	High power mode, 1 KHz, Vout = 100 mVpp, Max gain, load 8 ohms in series with 200 ohms		440		mW
G_{ACC}	Overall Gain accuracy		-2	0	2	dB
G_{STEP}	Gain Step Accuracy		-0.7	0	0.7	dB

7. Audio DAC

7.1 Electrical Specifications

AVDD, AVDDHS = 2.8 V, T_A = 25°C, typical case, unless otherwise noted.

All noise and distortion specifications are measured in the 20 Hz to 0.425xFs and A-weighted filtered.

Full-scale levels scale proportionally with the analog supply voltage.

Table 7-1. Electrical Specifications

	Min	Typ	Max	Units
Overall				
Operating Temperature (ambient)	-40	+25	+85	°C
Analog Supply Voltage (AVDD, AVDDHS)	2.7	2.8	3.3	V
Digital Supply Voltage (VDIG)	2.4	2.8	3.3	V
DIGITAL INPUTS/OUTPUTS				
Resolution		20		bits
Logic Family		CMOS		
Logic Coding		2's Complement		
Analog Performance - DAC to Line-out/Headphone Output				
Output level for full scale input (for AVDD, AVDDHS = 2.8 V)		1.65		Vpp
Output common mode voltage		0.5 x AVDDHS		V
Output load resistance (on HSL, HSR) Headphone load Line load	 16 7	 32 10		 Ohm kOhm
Output load capacitance (on HSL, HSR) Headphone load Line load		 30 30	 1000 150	 pF pF
Signal to Noise Ratio (-1dBFS @ 1kHz input and 0dB Gain) Line and Headphone loads	87	92		dB
Total Harmonic Distortion (-1dBFS @ 1kHz input and 0dB Gain) Line Load Headphone Load Headphone Load (16 Ohm)		 0.01 0.06 0.5	 0.016 0.1 1	 % % %
Dynamic Range (measured with -60 dBFS @ 1kHz input, extrapolated to full-scale) Line Load Headphone Load	 88 70	 93 74		 dB dB
Interchannel mismatch		0.1	1	dB
Left-channel to right-channel crosstalk (@ 1kHz)		-90	-80	dB
Output Headset Driver Level Control Range	-6		6	dB
Output Headset Driver Level Control Step		3		dB

Table 7-1. Electrical Specifications (Continued)

	Min	Typ	Max	Units
PSRR 1 kHz 20 kHz		 55 50		 dB dB
Maximum output slope at power up (100 to 220 µF coupling capacitor)			3	V/s
Analog Performance - Line-in/Microphone Input to Line-out/Headphone Output				
Input level for full scale output - 0dBFS Level @ AVDD, AVDDHS = 2.8 V and 0 dB gain @ AVDD, AVDDHS = 2.8 V and 20 dB gain		 1.65 583 0.165 58.3		 Vppm Vrms Vppm Vrms
Input common mode voltage		0.5 x AVDD		V
Input impedance	7	10		kOhm
Signal to Noise Ratio -1 dBFS @ 1kHz input and 0 dB gain -21 dBFS @ 1kHz input and 20 dB gain	81	 85 71		 dB
Dynamic Range (extrapolated to full scale level) -60 dBFS @ 1kHz input and 0 dB gain -60 dBFS @ 1kHz input and 20 dB gain	82	 86 72		 dB
Total Harmonic Distortion -1dBFS @ 1kHz input and 0 dB gain -1dBFS @ 1kHz input and 20 dB gain		 0.01 0.018	 0.016 0.04	 % %
Interchannel mismatch		0.1	1	dB
Left-channel to right-channel crosstalk (@ 1kHz)		-90	-80	dB
Analog Performance - Differential mono input amplifier				
Differential input level for full scale output - 0dBFS Level @ AVDD, AVDDHS = 2.8 V and 0 dB gain		 1.65 583		 Vppdif mVrms
Input common mode voltage		0.5xAVDD		V
Input impedance	7	10		kOhm
Signal to Noise Ratio (-1 dBFS @ 1kHz input and 0 dB gain)	76	80		dB
Total Harmonic Distortion (-1dBFS @ 1kHz input and 0 dB gain)		-85	-81	dB
Analog Performance - PA Driver				
Differential output level for full scale input (for AVDD, AVDDHS = 2.8 V)		3.3		Vppdif
Output common mode voltage		0.5 x AVDDHS		V
Output load		10		kOhm
			30	pF
Signal to Noise Ratio (-1dBFS @ 1kHz input and 0dB Gain)	76	80		dB

Table 7-1. Electrical Specifications (Continued)

	Min	Typ	Max	Units
Total Harmonic Distortion (-1dBFS @ 1kHz input and 0dB Gain)		-75	-71	dB
Master Clock				
Master Clock Maximum Long Term Jitter			1.5	ns_{pp}
Digital Filter Performance				
Frequency response (10 Hz to 20 kHz)		± 0.1		dB
Deviation from linear phase (10 Hz to 20 kHz)		± 0.1		deg
Passband 0.1 dB corner		0.4535		Fs
Stopband	0.5465			Fs
Stopband Attenuation	65			dB
De-emphasis Filter Performance (for 44.1kHz Fs)				
MAX deviation from ideal response	-1		1	dB
POWER PERFORMANCE				
Current consumption from Analog supply in power on		9.5		mA
Current consumption from Analog supply in power down			10	mA
Power on Settling Time From full power down to full power up (Vref and VCM decoupling capacitors charge) Line in amplifier (line in coupling capacitors charge) Driver amplifier (out driver DC blocking capacitors charge)		 500 50 500		 ms ms ms

7.2 Digital Filters Transfer Function

Figure 7-1. Channel Filter

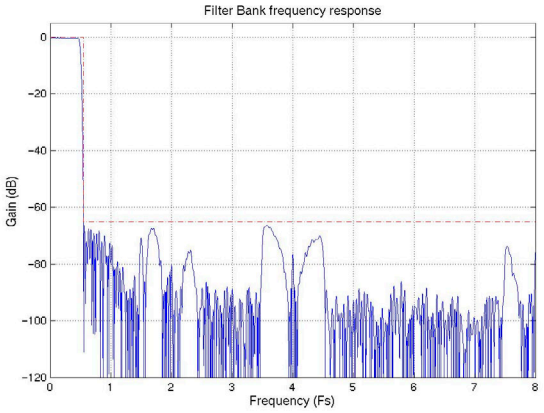


Figure 7-2. Channel Filter

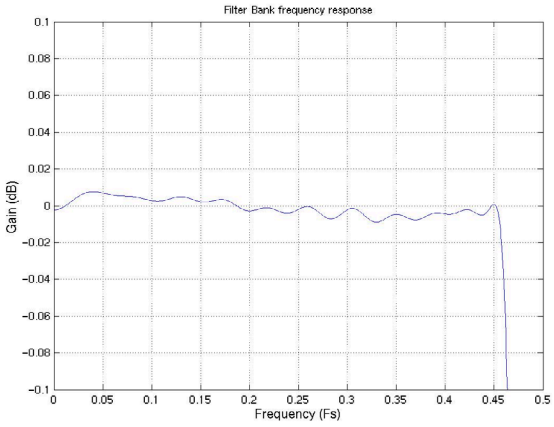
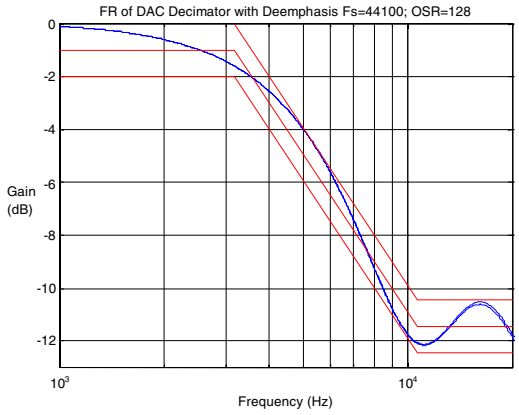


Figure 7-3. De-emphasis Filter



7.3 Data Interface

Normal operation is entered by applying correct LRFS, BCLK and SDIN waveforms to the serial interface, as illustrated in Figure 7-4, Figure 7-5 and Figure 7-6.

To avoid noise at the output, the reset state is maintained until proper synchronization is achieved in the serial interface.

The data interface allows three different data transfer modes. See Figure 7-4, Figure 7-5 and Figure 7-6.

Figure 7-4. 20-bit I2S Justified Mode

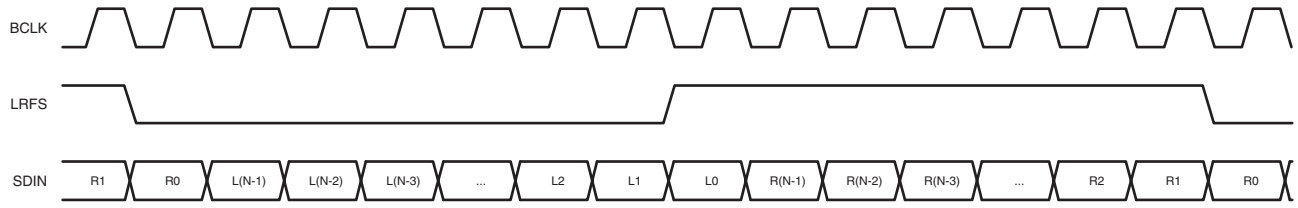


Figure 7-5. 20-bit MSB Justified Mode

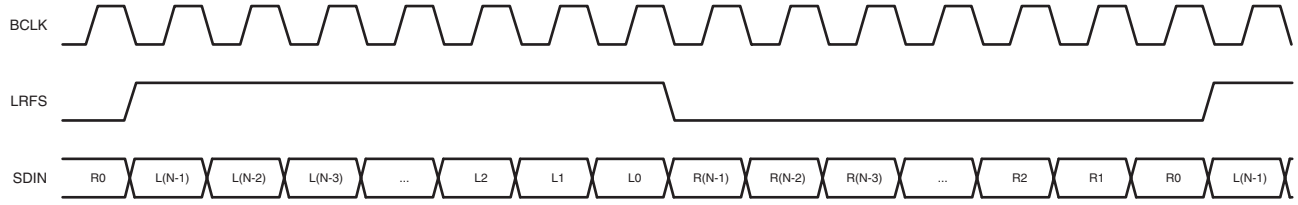
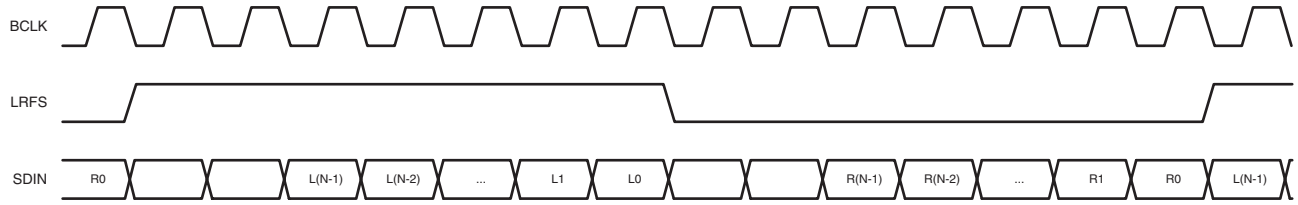


Figure 7-6. 20-bit LSB Justified Mode



The selection between modes is done using the DINTSEL<1:0> signal.

DINTSEL <1:0>	Format
00	I2S Justified
01	MSB Justified
1x	LSB Justified

The data interface always works in slave mode. This means that the LRFS and the BCLK signals are provided by the host controller. In order to achieve proper operation, the LRFS and the BCLK signals must be synchronous with the MCLK master clock signal and their frequency relationship must reflect the selected data mode. For example, if the data mode selected is the 20-bit MSB Justified, then the BCLK frequency must be 40 times higher than the LRFS frequency.

7.4 Timing Specifications

The timing constraints of the data interface are described in Figure 7-7 and Table 7-2 below.

Figure 7-7. Data Interface Timing Diagram

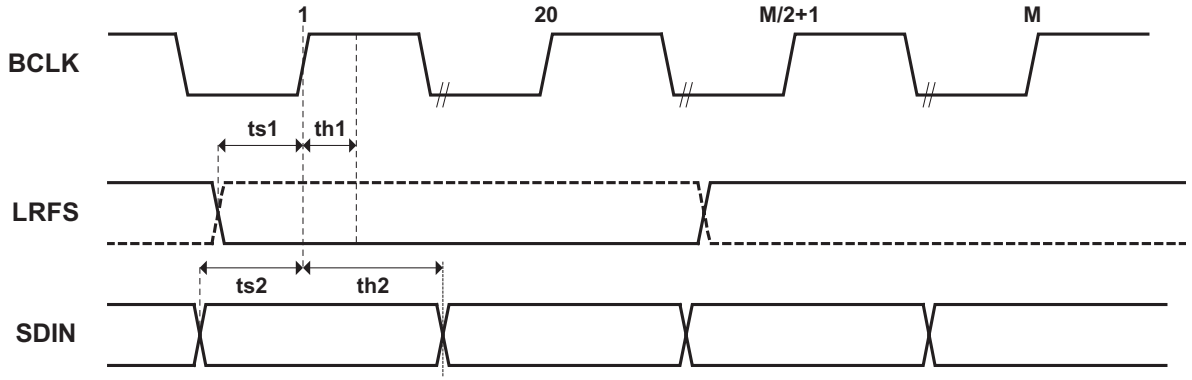


Table 7-2. Data Interface Timing Parameters

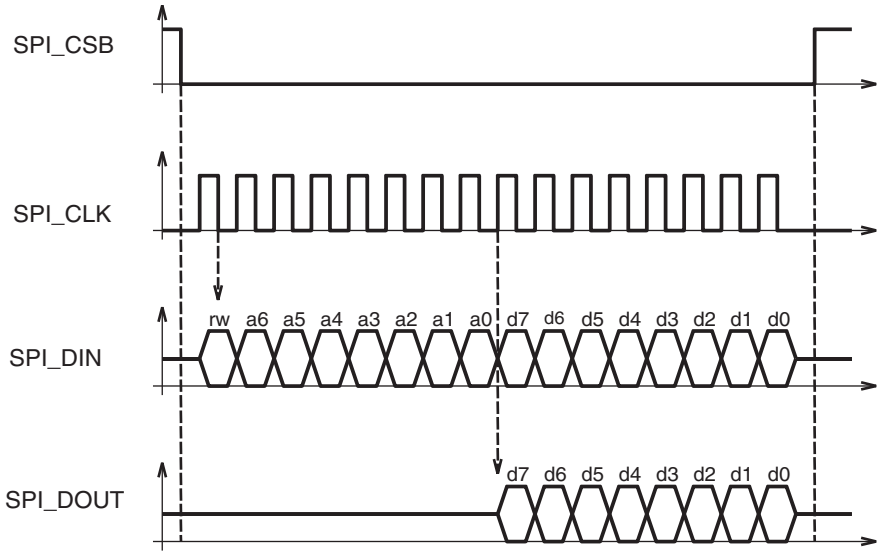
	Parameter	Min	Typ	Max	Unit
ts1	LRFS set-up time before BCLK rising edge	10			ns
th1	LRFS hold time after BCLK rising edge	10			ns
ts2	DIN set-up time before BCLK rising edge	10			ns
th2	DIN hold time after BCLK rising edge	10			ns

8. SPI Interface

8.1 Architecture

The SPI is a three-wire bi-directional asynchronous serial link. It works only in slave mode. The protocol is the following:

Figure 8-1. SPI Architecture



8.2 SPI Protocol

On SPI_DIN, the first bit is a read/write bit. 0 indicates a write operation, while 1 is for a read operation. The seven following bits are used for the register address and the eight last ones are the write data. For both address and data, the most significant bit is the first one.

In case of a read operation, SPI_DOUT provides the contents of the read register, MSB first.

The transfer is enabled by the CSB signal active low. When no operation is being carried out, SPI_DOUT is set high impedance to allow sharing of MCU serial interface with other devices. The interface is reset at every rising edge of SPI_CSB in order to come back to an idle state, even if the transfer does not succeed. The SPI is synchronized with the serial clock SPI_CLK. Falling edge latches SPI_DIN input and rising edge shifts SPI_DOUT output bits.

Note that MCLK must run during any SPI write access from address 0x00 to 0x0D.

8.3 SPI Interface Timing

Figure 8-2. SPI Timing

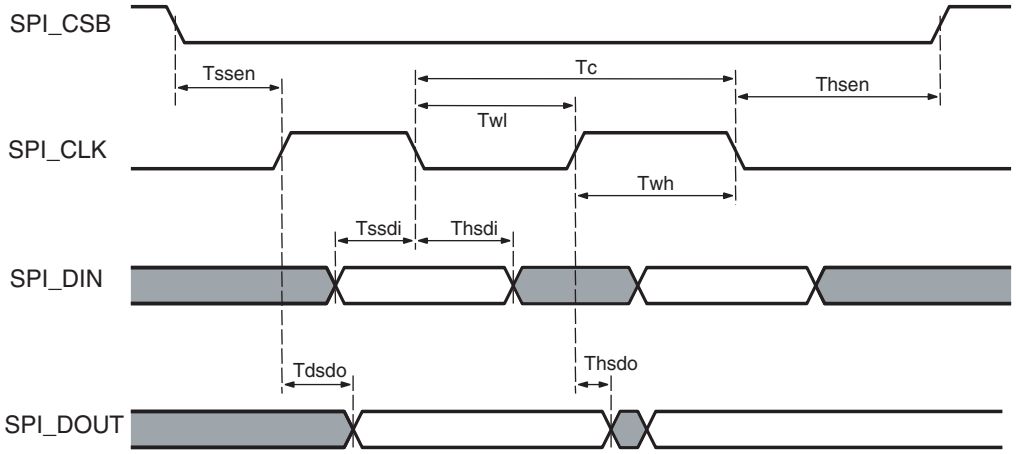


Table 8-1. SPI Timing Parameters

Parameter	Description	Min	Max
Tc	SPI_CLK min period	100 ns	-
Twl	SPI_CLK min pulse width low	50 ns	-
Twh	SPI_CLK min pulse width high	50 ns	-
Tssen	Setup time SPI_CSB falling to SPI_CLK rising	50 ns	-
Thsen	Hold time SPI_CLK falling to SPI_CSB rising	50 ns	-
Tssdi	Setup time SPI_DIN valid to SPI_CLK falling	20 ns	-
Thsdi	Hold time SPI_CLK falling to SPI_DIN not valid	20 ns	-
Tdsdo	Delay time SPI_CLK rising to SPI_DOUT valid	-	20 ns
Thsdo	Hold time SPI_CLK rising to SPI_DOUT not valid	0 ns	-

8.4 SPI User Interface

Table 8-2. SPI Register Mapping

Address	Register	Name	Access	Reset State
0x00	DAC_CTRL	DAC Control	Read/Write	0x00
0x01	DAC_LLIG	DAC Left Line In Gain	Read/Write	0x05
0x02	DAC_RLIG	DAC Right Line In Gain	Read/Write	0x05
0x03	DAC_LPMG	DAC Left Master Playback Gain	Read/Write	0x08
0x04	DAC_RPMG	DAC Right Master Playback Gain	Read/Write	0x08
0x05	DAC_LLOG	DAC Left Line Out Gain	Read/Write	0x00
0x06	DAC_RLOG	DAC Right Line Out Gain	Read/Write	0x00
0x07	DAC_OLC	DAC Output Level Control	Read/Write	0x22
0x08	DAC_MC	DAC Mixer Control	Read/Write	0x09
0x09	DAC_CSFC	DAC Clock and Sampling Frequency Control	Read/Write	0x00
0x0A	DAC_MISC	DAC Miscellaneous	Read/Write	0x00
0x0C	DAC_PRECH	DAC Precharge Control	Read/Write	0x00
0x0D	DAC_AUXG	DAC Auxiliary Input Gain Control	Read/Write	0x05
0x10	DAC_RST	DAC Reset	Read/Write	0x00
0x11	PA_CRTL	Power Amplifier Control	Read/Write	0x00

Note: MSB = Bit 7, LSB = Bit 0

8.5 DAC Control Register

Register Name: DAC_CTRL

Reset State: 0x00

Access: Read/Write

7	6	5	4	3	2	1	0
ONPADRV	ONAUXIN	ONDACR	ONDACL	ONLNOR	ONLNOL	ONLNIR	ONLNIL

- **ONLNIL**

Left channel line in amplifier (L to power down, H to power up)

- **ONLNIR**

Right channel line in amplifier (L to power down, H to power up)

- **ONLNOL**

Left channel line out driver (L to power down, H to power up)

- **ONLNOR**

Right channel line out driver (L to power down, H to power up)

- **ONDACL**

Left channel DAC (L to power down, H to power up)

- **ONDACR**

Right channel DAC (L to power down, H to power up)

- **ONAUXIN**

Differential mono auxiliary input amplifier (L to power down, H to power up)

- **ONPADRV**

Differential mono PA driver (L to power down, H to power up)

8.6 DAC Left Line In Gain Register

Register Name: DAC_LLIG

Reset State: 0x05

Access: Read/Write

7	6	5	4	3	2	1	0
0	0	0	LLIG				

- **LLIG: Left channel line in analog gain selector**

LLIG<4:0>	Gain	Unit
00000	20	dB
00001	12	dB
00010	9	dB
00011	6	dB
00100	3	dB
00101	0	dB
00110	-3	dB
00111	-6	dB
01000	-9	dB
01001	-12	dB
01010	-15	dB
01011	-18	dB
01100	-21	dB
01101	-24	dB
01110	-27	dB
01111	-30	dB
10000	-33	dB
≥10001	< -60	dB

8.7 DAC Right Line In Gain Register

Register Name: DAC_RLIG

Reset State: 0x05

Access: Read/Write

7	6	5	4	3	2	1	0
0	0	0	RLIG				

- **RLIG: Right channel line in analog gain selector**

RLIG<4:0>	Gain	Unit
00000	20	dB
00001	12	dB
00010	9	dB
00011	6	dB
00100	3	dB
00101	0	dB
00110	-3	dB
00111	-6	dB
01000	-9	dB
01001	-12	dB
01010	-15	dB
01011	-18	dB
01100	-21	dB
01101	-24	dB
01110	-27	dB
01111	-30	dB
10000	-33	dB
≥10001	< -60	dB

8.8 DAC Left Master Playback Gain Register

Register Name: DAC_LMPG

Reset State: 0x08

Access: Read/Write

7	6	5	4	3	2	1	0
0	0	LMPG					

- **LMPG: Left channel master playback digital gain selector**

LMPG<5:0>	Gain	Unit	LMPG<5:0>	Gain	Unit
000000	12.0	dB	010001	-13.5	dB
000001	10.5	dB	010010	-15.0	dB
000010	9.0	dB	010011	-16.5	dB
000011	7.5	dB	010100	-18.0	dB
000100	6.0	dB	010101	-19.5	dB
000101	4.5	dB	010110	-21.0	dB
000110	3.0	dB	010111	-22.5	dB
000111	1.5	dB	011000	-24.0	dB
001000	0.0	dB	011001	-25.5	dB
001001	-1.5	dB	011010	-27.0	dB
001010	-3.0	dB	011011	-28.5	dB
001011	-4.5	dB	011100	-30.0	dB
001100	-6.0	dB	011101	-31.5	dB
001101	-7.5	dB	011110	-33.0	dB
001110	-9.0	dB	011111	-34.5	dB
001111	-10.5	dB	≥ 100000	mute	dB
010000	-12.0	dB			

8.9 DAC Right Master Playback Gain Register

Register Name: DAC_RMPG

Reset State: 0x08

Access: Read/Write

7	6	5	4	3	2	1	0
0	0	RMPG					

- **RMPG: Right channel master playback digital gain selector**

RMPG<5:0>	Gain	Unit	RMPG<5:0>	Gain	Unit
000000	12.0	dB	010001	-13.5	dB
000001	10.5	dB	010010	-15.0	dB
000010	9.0	dB	010011	-16.5	dB
000011	7.5	dB	010100	-18.0	dB
000100	6.0	dB	010101	-19.5	dB
000101	4.5	dB	010110	-21.0	dB
000110	3.0	dB	010111	-22.5	dB
000111	1.5	dB	011000	-24.0	dB
001000	0.0	dB	011001	-25.5	dB
001001	-1.5	dB	011010	-27.0	dB
001010	-3.0	dB	011011	-28.5	dB
001011	-4.5	dB	011100	-30.0	dB
001100	-6.0	dB	011101	-31.5	dB
001101	-7.5	dB	011110	-33.0	dB
001110	-9.0	dB	011111	-34.5	dB
001111	-10.5	dB	≥ 100000	mute	dB
010000	-12.0	dB			

8.10 DAC Left Line Out Gain Register

Register Name: DAC_LLOG

Reset State: 0x00

Access: Read/Write

7	6	5	4	3	2	1	0
0	0	LLOG					

- **LLOG: Left channel line out digital gain selector**

LLOG<5:0>	Gain	Unit	LLOG<5:0>	Gain	Unit
000000	0.0	dB	010000	-24.0	dB
000001	-1.5	dB	010001	-25.5	dB
000010	-3.0	dB	010010	-27.0	dB
000011	-4.5	dB	010011	-28.5	dB
000100	-6.0	dB	010100	-30.0	dB
000101	-7.5	dB	010101	-31.5	dB
000110	-9.0	dB	010110	-33.0	dB
000111	-10.5	dB	010111	-34.5	dB
001000	-12.0	dB	011000	-36.0	dB
001001	-13.5	dB	011001	-37.5	dB
001010	-15.0	dB	011010	-39.0	dB
001011	-16.5	dB	011011	-40.5	dB
001100	-18.0	dB	011100	-42.0	dB
001101	-19.5	dB	011101	-43.5	dB
001110	-21.0	dB	011110	-45.0	dB
001111	-22.5	dB	011111	-46.5	dB
			≥ 100000	mute	dB

8.11 DAC Right Line Out Gain Register

Register Name: DAC_RLOG

Reset State: 0x00

Access: Read/Write

7	6	5	4	3	2	1	0
0	0	RLOG					

- **RLOG: Right channel line out digital gain selector**

RLOG<5:0>	Gain	Unit	RLOG<5:0>	Gain	Unit
000000	0.0	dB	010000	-24.0	dB
000001	-1.5	dB	010001	-25.5	dB
000010	-3.0	dB	010010	-27.0	dB
000011	-4.5	dB	010011	-28.5	dB
000100	-6.0	dB	010100	-30.0	dB
000101	-7.5	dB	010101	-31.5	dB
000110	-9.0	dB	010110	-33.0	dB
000111	-10.5	dB	010111	-34.5	dB
001000	-12.0	dB	011000	-36.0	dB
001001	-13.5	dB	011001	-37.5	dB
001010	-15.0	dB	011010	-39.0	dB
001011	-16.5	dB	011011	-40.5	dB
001100	-18.0	dB	011100	-42.0	dB
001101	-19.5	dB	011101	-43.5	dB
001110	-21.0	dB	011110	-45.0	dB
001111	-22.5	dB	011111	-46.5	dB
			≥ 100000	mute	dB

8.12 DAC Output Level Control Register

Register Name: DAC_OLC

Reset State: 0x22

Access: Read/Write

7	6	5	4	3	2	1	0
RSHORT	ROLC			LSHORT	LOLC		

- **LOLC: Left channel output level control selector**

LOLC	Gain	Unit
000	6	dB
001	3	dB
010	0	dB
011	-3	dB
≥ 100	-6	dB

- **LSHORT: Left channel short circuit indicator**

Persistent; after being set, bit is not cleared automatically even after the short circuit is eliminated; must be cleared by reset cycle or direct register write operation.

- **ROLC: Right channel output level control selector**

ROLC	Gain	Unit
000	6	dB
001	3	dB
010	0	dB
011	-3	dB
≥ 100	-6	dB

- **RSHORT: Right channel short circuit indicator**

Persistent; after being set, bit is not cleared automatically even after the short circuit is eliminated; must be cleared by reset cycle or direct register write operation.

8.13 DAC Mixer Control Register

Register Name: DAC_MC

Reset State: 0x09

Access: Read/Write

7	6	5	4	3	2	1	0
0	0	INVR	INVL	RMSMIN2	RMSMIN1	LMSMIN2	LMSMIN1

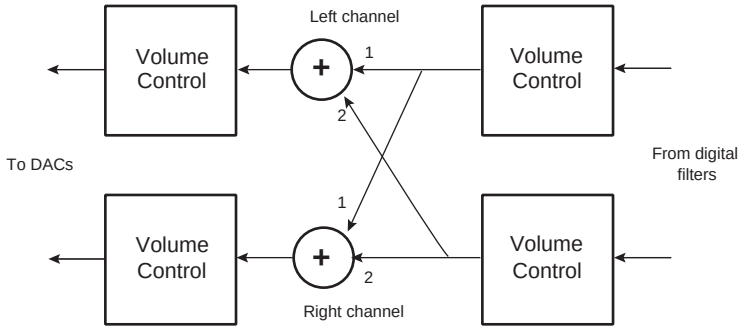
- **LMSMIN1: Left Channel Mono/Stereo Mixer Left Mixed input enable (H to enable, L to disable)**
- **LMSMIN2: Left Channel Mono/Stereo Mixer Right Mixed input enable (H to enable, L to disable)**
- **RMSMIN1: Right Channel Mono/Stereo Mixer Left Mixed input enable (H to enable, L to disable)**
- **RMSMIN2: Right Channel Mono/Stereo Mixer Right Mixed input enable (H to enable, L to disable)**
- **INVL: Left channel mixer output invert (H to enable, L to disable)**
- **INVR: Right channel mixer output invert (H to enable, L to disable)**

8.13.1 Digital Mixer Control

The Audio DAC features a digital mixer that allows the mixing and selection of multiple input sources.

The mixing/multiplexing functions are described in Figure 8-3 and Table 8-3.

Figure 8-3. Digital Mixer Functions



Note: When the two mixer inputs are selected, a -6 dB gain is applied to the output signal. When only one input is selected, no gain is applied.

Table 8-3. Digital Mixer Signal Description

Signal	Description
LMSMIN1	Left Channel Mono/Stereo Mixer Left Mixed input enable - High to enable, Low to disable
LMSMIN2	Left Channel Mono/Stereo Mixer Right Mixed input enable - High to enable, Low to disable
RMSMIN1	Right Channel Mono/Stereo Mixer Left Mixed input enable - High to enable, Low to disable
RMSMIN2	Right Channel Mono/Stereo Mixer Right Mixed input enable - High to enable, Low to disable

8.14 DAC Clock and Sampling Frequency Control Register

Register Name: DAC_CSFC

Reset State: 0x00

Access: Read/Write

7	6	5	4	3	2	1	0
0	0	0	OVRSEL	0	0	0	0

- **OVRSEL: Master clock selector**

L to 256 x Fs, H to 384 x Fs

Master clock and sampling frequency selection

Table 8-4 describes the modes available for master clock and sampling frequency selection.

Table 8-4. Master Clock Modes

OVRSEL	Master Clock
0	256 x Fs
1	384 x Fs

8.15 DAC Miscellaneous Register

Register Name: DAC_MISC

Reset State: 0x00

Access: Read/Write

7	6	5	4	3	2	1	0
VCMCAPSEL	0	DINTSEL		DITHEN	DEEMPEN	NBITS	

- **NBITS<1:0>: Data interface word length**

The selection of input sample size is done using the NBITS field.

NBITS <1:0>	Format
00	16 bits
01	18 bits
10	20 bits

- **DEEMPEN: De-emphasis enable (L to disable, H to enable)**

To enable the de-emphasis filtering the DEEMPHEN signal must be set to high.

- **DITHEN: Dither enable (L to disable, H to enable)**

The dither option (added in the playback channel) is enabled by setting the DITHEN signal to high.

- **DINTSEL<1:0>: I2S data format selector**

The selection between modes is done using the DINTSEL<1:0> signal.

DINTSEL<1:0>	Format
00	I2S Justified
01	MSB Justified
1x	LSB Justified

- **VCMCAPSEL: VCM decoupling capacitor selector**

L for 10 µF, H for 100 µF

8.16 DAC Precharge Control Register

Register Name: DAC_PRECH

Reset State: 0x00

Access: Read/Write

7	6	5	4	3	2	1	0
PRCHGPDRV	PRCHGAUX1	PRCHGLNOR	PRCHGLNOL	PRCHGLNIR	PRCHGLNIL	PRCHG	ONMSTR

- **ONMSTR: Master power on control (L to power down, H to power up)**
- **PRCHARGE: Master pre-charge (H to charge)**
- **PRCHARGELNIL: Left channel line in pre-charge (H to charge)**
- **PRCHARGELNIR: Right channel line in pre-charge (H to charge)**
- **PRCHARGELNOL: Left channel line out pre-charge (H to charge)**
- **PRCHARGELNOR: Right channel line out pre-charge (H to charge)**
- **PRCHARGEAUXIN: Differential mono auxiliary input pre-charge (H to charge)**
- **PRCHARGEPADRV: Differential mono PA driver pre-charge (H to charge)**

8.17 DAC Auxiliary Input Gain Control Register

Register Name: DAC_AUXG

Reset State: 0x05

Access: Read/Write

7	6	5	4	3	2	1	0
0	0	0	AUXG				

- **AUXG: Differential mono auxiliary input analog gain selector**

AUXG<4:0>	Gain	Unit
00000	20	dB
00001	12	dB
00010	9	dB
00011	6	dB
00100	3	dB
00101	0	dB
00110	-3	dB
00111	-6	dB
01000	-9	dB
01001	-12	dB
01010	-15	dB
01011	-18	dB
01100	-21	dB
01101	-24	dB
01110	-27	dB
01111	-30	dB
10000	-33	dB
≥ 10001	< -60	dB

8.18 DAC Reset Register

Register Name: DAC_RST

Reset State: 0x00

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	–	–	–	RESMASK	RESFILZ	RSTZ

- **RSTZ: Active low reset of the audio codec**
- **RESFILZ: Active low reset of the audio codec filter**
- **RESMASK: Active high reset mask of the audio codec**

See “Supplies and Start-up” on page 30.

8.19 PA Control Register

Register Name: PA_CTRL

Reset State: 0x00

Access: Read/Write

7	6	5	4	3	2	1	0
–	APAON	APAPRECH	APALP	APAGAIN			

- **APAGAIN<3:0>: Audio power amplifier gain**

APAGAIN<3:0>	Gain db	APAGAIN<3:0>	Gain db
0000	FORBIDDEN	1000	-1
0001	20	1001	-4
0010	17	1010	-7
0011	14	1011	-10
0100	11	1100	-13
0101	8	1101	-16
0110	5	1110	-19
0111	2	1111	-22

- **APALP: Audio power amplifier low power bit**

0: High power

1: Low power

- **APAPRECH: Audio power amplifier precharge bit**
- **APAON: Audio power amplifier on bit**

APAON	APAPRECH	Operating Mode
0	0	Stand-by
0	1	Input capacitors precharge
1	0	Active mode
1	1	Forbidden state

9. Supplies and Start-up

In operating mode, VBAT (supply of the audio power amplifier) must be between 3V and 5.5V and AVDD, AVDDHS and VDIG must be inferior or equal to VBAT.

A typical application is VBAT connected to a battery and AVDD, AVDDHS and VDIG supplied by regulators. VBAT must be present at the same time or before AVDD, AVDDHS and VDIG.

RSTB must be active (0) until the voltages are stable and reach the proper values.

To avoid noise issues, it is recommended to use ceramic decoupling capacitors for each supply close to the package. See Figure 11-1 on page 32.

The track of the supplies must be optimized to minimize the resistance, especially on VBAT where all the current from the power amplifier comes from.

HPN and HPP must be routed symmetrically and the resistance must be minimized.

9.1 Audio DAC Start-up Sequences

In order to minimize the noise during the start-up, a specific sequence should be applied.

In any audio configuration, always force Bit 2 to high level (“1”) at 0x0B address.

9.1.1 Power on Example

Path DAC to headset output

1. Write @0x10 => 0x03 (deassert the reset)
2. Write @0x0C => 0xFF (precharge + master on)
3. Write @0x00 => 0x30 (ONLNOL and ONLONOR set to 1)
4. Delay 500 ms
5. Write @0x0C => 0x01 (precharge off + master on)
6. Delay 1ms
7. Write @0x00 => 0x3C (ONLNOL, ONLNOR, ONDACR and ONDACL set to 1)

9.1.2 Power off Example

1. Write @0x00 => 0x30 (ONDACR and ONDACL set to 0)
2. Write @0x0C => 0x00 (master off)
3. Delay 1ms
4. Write @0x00 => 0x00 (all off)

9.1.3 I2S Example

In order to prevent I2S from generating noise at the output (for example a MP3 player switching from one song to another):

1. Set ONDAC to 0 ((bit 4 and 5 in register @0x00)
2. Stop I2S and MCLK

When I2S is restarted, in order to prevent noise generation at the output:

1. Start MCLK
2. Write @0x10 => 0x07 (RSTMSK=1)
3. Write @0x10 => 0x04 (RESFILZ=0, RSTZ=0)
4. Write @0x10 => 0x07 (RESFILZ=1, RSTZ=1)

5. Write @0x10 => 0x03 (RSTMSK=0)
6. Delay 5 ms
7. Set ONDAC to 1 (bit 4 and 5 in register @0x00)
8. Reprogram all DAC settings (Audio format, gains, etc.)
9. Start I2S.

9.2 Audio Power Amplifier Power on Sequence

To avoid an audible “click” at start-up, the input capacitors must be pre-charged before the power amplifier.

1. At start-up, set APAON off, APAGAIN<3:0> set to -22 dB, set APAPRECHARGE to 1.
2. Wait 50 ms minimum.
3. Then disable APAPRECH and set APAON.
4. Wait 10 ms min time.
5. Set the gain to the value chosen.

9.2.1 Audio Power Amplifier Power off Sequence

To avoid an audible “click” at power-off, the gain should be set to the minimum gain (-22 dB) before turning off the power amplifier.

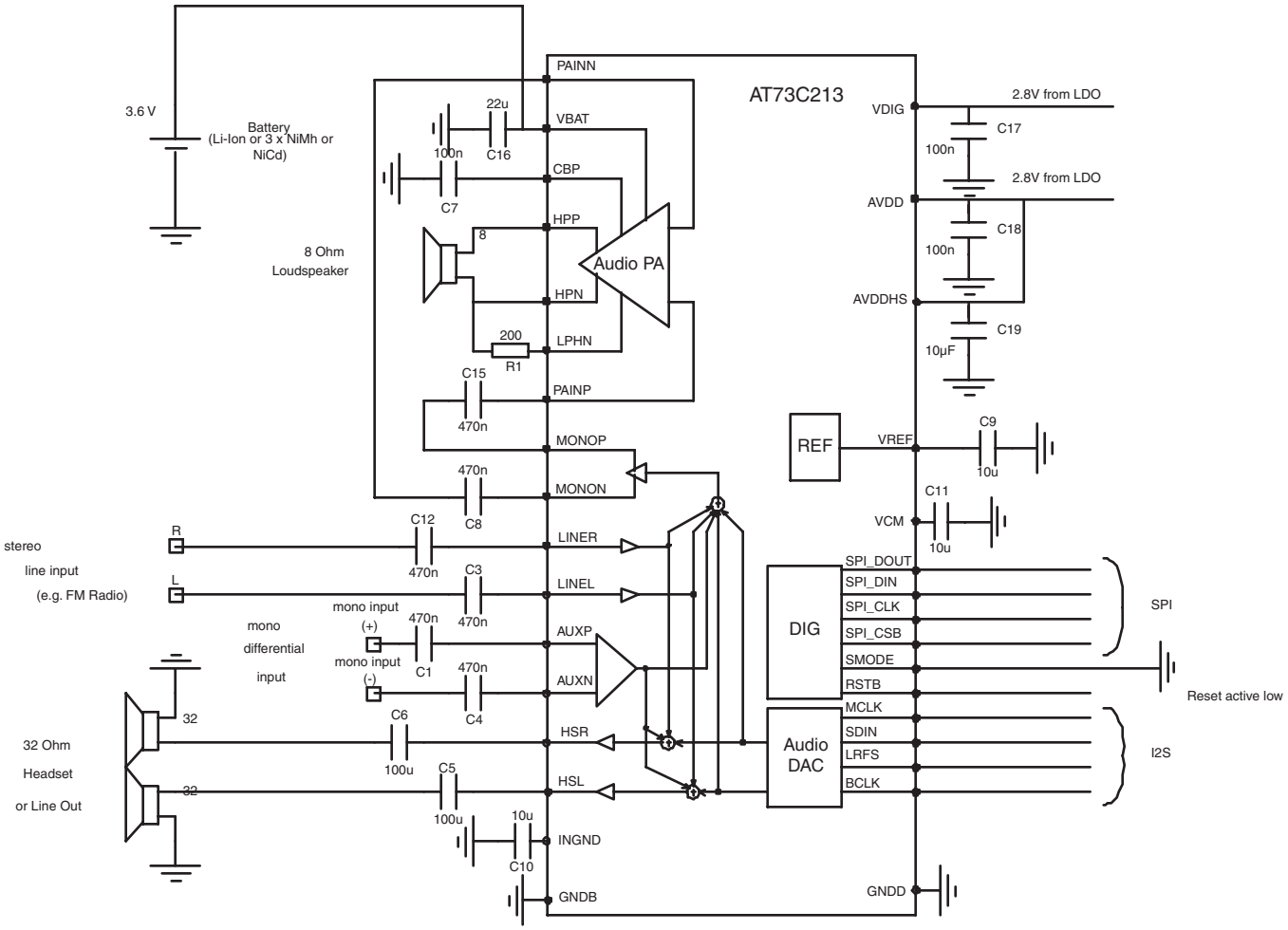
10. Current Consumption in Different Modes

Table 10-1. Current Consumption in Different Modes

Mode	Current Consumption (typ)	Current Consumption (max)	Unit
0: Off	5	12	uA
1: Standby	250	350	uA
2: DAC Playback through Stereo Headset (Current in the load not included)	5100	6700	uA
3: Stereo DAC Playback to Audio PA (Current in the load not included)	9500	13500	uA
4: Playback from Mono in to Audio PA (Current in the load not included)	6200	10500	uA
5: Playback from Stereo Line Input to Stereo Headset (Current in the load not included)	1600	3300	uA

11. Application Diagram

Figure 11-1. Application Using One Li-Ion Battery



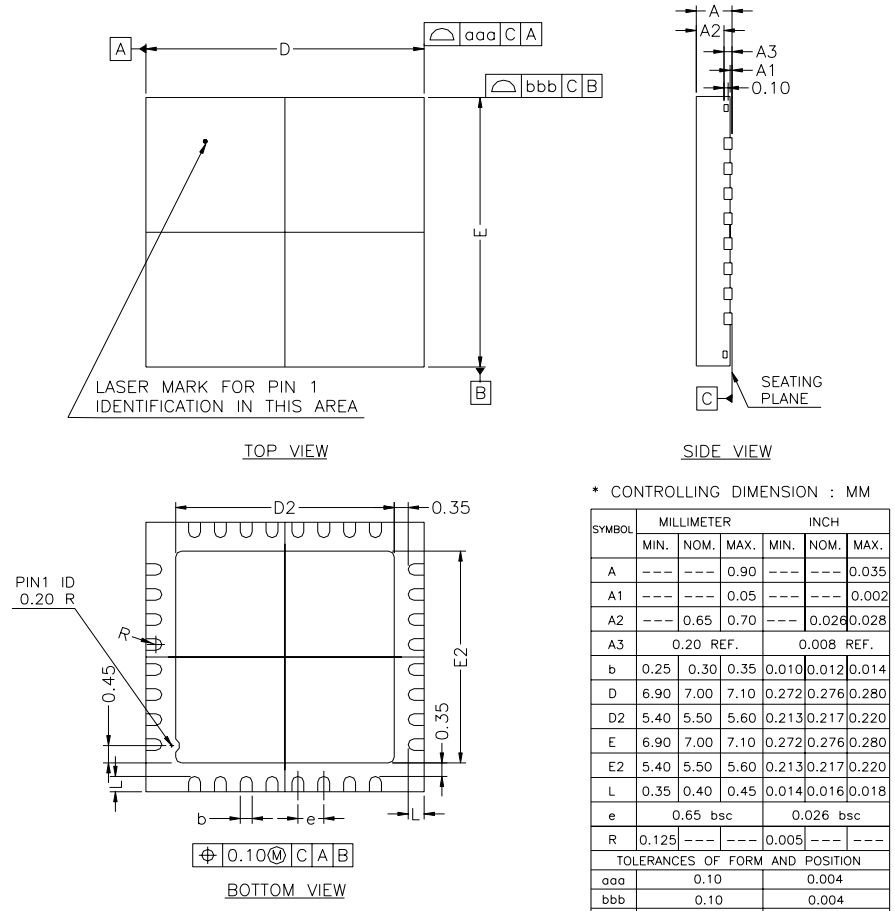
12. Components List

Table 12-1. Components List

Reference	Value	Techno	Size	Manufacturer & Reference
C1, C3, C4, C8, C12, C15	470 nF	Ceramic	0402	C1005X5R0J474K (TDK) or GRM155R60J474KE18 (Murata®)
C5, C6	100 µF	Ceramic	1210	C3225X5R0J107M (TDK) or GRM32ER60J107ME20 (Murata)
C9, C10, C11, C19	10 µF	Ceramic	0603	C1608X5R0J106MT (TDK) or GRM188R60J106ME47 (Murata)
C7, C17, C18	100 nF	Ceramic	0402	C1005X5R1C104KT (TDK) or GRM155R61A104KA01 (Murata)
C16	22 µF	Ceramic	0805	C2012X5R0J226MT (TDK) or GRM21BR60J226ME39 (Murata)
R1	200 Ohms		0603	

13. Package Drawing

Figure 13-1. Package Outline



* CONTROLLING DIMENSION : MM

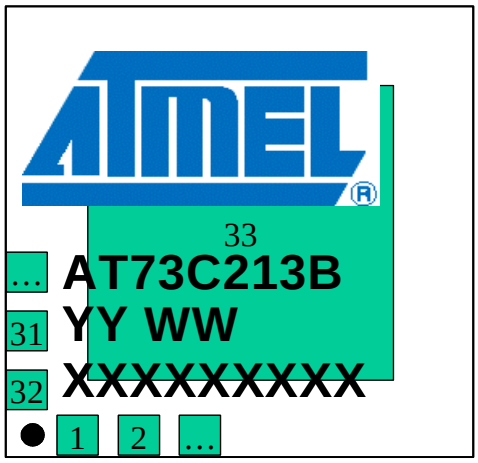
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	---	---	0.05	---	---	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	6.90	7.00	7.10	0.272	0.276	0.280
D2	5.40	5.50	5.60	0.213	0.217	0.220
E	6.90	7.00	7.10	0.272	0.276	0.280
E2	5.40	5.50	5.60	0.213	0.217	0.220
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.65 bsc			0.026 bsc		
R	0.125	---	---	0.005	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

Note: 1.All Dimensions are in mm
2 Package WARPAGE Max: 0.08 mm

Notes: 1. All dimensions are in mm.

2. Drawing is for general information only. Refer to JEDEC drawing MO-220 for additional information.

Figure 13-2. Package Drawing with Pin 1 and Marking



14. Revision History

Table 14-1. Revision History

Doc. Rev.	Comments	Change Request Ref.
6704A	First issue.	

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